SSRL Beam Position Monitor Detection Electronics*

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Abstract

As part of a program to improve its orbit stability SSRL is redesigning its detection electronics for its beam position monitors (BPMs) [1] [2]. The electronics must provide high accuracy positional information at the low bandwidth required of an orbit feedback. With available commercial technology, it is now possible to obtain high accuracy turn by turn information so that this electronic module can also be used to measure beam dynamics. The new electronics are currently being fabricated for testing and evaluation. This article discusses the design criteria used for this prototype system.

1 INTRODUCTION

SPEAR is a 3 GeV electron storage ring used for synchrotron radiation. It was originally built as an $e^- - e^+$ collider for high energy physics, and its BPM detection electronics was designed to differentiate between the signals from the two particles. All of the BPM inputs are multiplexed into one large switching matrix and processed by one set of electronics. We are redesigning the electronics to improve processor speed, dynamic range, and accuracy. In addition to providing high accuracy positional information under normal operation, the system must be able to detect low current orbits for injection studies, etc. Table 1 lists the relevant parameters used in the design and Figure 1 gives the flow of the processed signal.

Table 1: SPEAR BPM Parameters

Energy	E	3	GeV
Radio Frequency	f_{RF}	358.54	MHz
Harmonic Number	h	280	
Revolution Frequency	f_{rev}	1.2805	MHz
Nominal Beam Current	I_{nom}	20–100	mA
Number of BPMs		40	
Accuracy/ processing		10	μm
Resolution		10	μm
Channel Isolation		> 80	dB
Detector SNR @I_{nom}	SNR	> 126	dB/$\sqrt{\text{Hz}}$
Dynamic Range		40	dB

2 RF SIGNAL PROCESSING

The periodic nature of a storage ring determined our choice of a harmonic processing system that detects the power in an appropriate frequency bandwidth. Since we determine the beam position by the difference over sum technique [3] [4], we multiplex the signals as early as possible to minimize errors in the signals due to electronic variations. Our RF processing is designed to provide a high quality, narrow bandwidth signal for our IF.

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2.1 *Processing Frequency*

The periodicity of the ring means that frequency spectrum of the current will be centered on harmonics of f_{rev}. The amplitude of these harmonics will be the Fourier transform of the fill pattern, modulated by the Fourier transform of the bunch shape. For arbitrary fills, the only harmonics guaranteed to have non-zero amplitude are the harmonics of f_{RF}. The decision as to which RF harmonic to process was a tradeoff of engineering considerations. SPEAR has several BPMs near the RF cavities, where the evanescent fields from these cavities provide a strong beam-independent signal at the RF, so we rejected processing f_{RF}. Although our BPM buttons are more sensitive to the higher beam frequencies, we chose the second RF harmonic, 717.08 MHz, for two reasons. First, our signal processing electronics will be housed in the control room, typically 100 m from the buttons, and attenuation due to the cable length greatly increases with frequency. Second, the size of our beam pipes gives a typical vacuum chamber cutoff frequency of about 1.5 GHz, and in many places as low as 1 GHz. Discontinuities and structures in the vacuum chamber support higher order modes at these frequencies that contaminate the fundamental signal on the BPMs produced by the image charges of the beam.

2.2 *Signal Multiplexing*

The main purpose of the BPM system is to provide high accuracy information about the orbit of the beam. For our vacuum chamber size, resolution of 1 micron beam motion means a variation in the difference signals of about 50 ppm from the 4 buttons of each BPM. The design of the electronics attempts to minimize the potential for systematic errors that could prevent high resolution measurements. Therefore, we have multiplexed as much of the button processing as possible. The current system multiplexes all BPM buttons into a single processor. We will initially commission the new processor with this same arrangement, but then will build one processor per BPM.

The BPM signals are multiplexed at the input. Since this is the only part of the circuitry that is not common to all of the buttons, we desire the technology with the most consistent and repeatable characteristics. We chose GaAs FETs over PIN diodes because of the independence of the FET video impedance with respect to signal level. Standard isolation per switch at our processing frequency is only about 35 dB, so our design cascades three absorptive switches in series for each button. The selected signal passes through its three switches to the processor, while the other buttons see the 50Ω on chip terminator of their first switch. Based on the signal level out of the button, we do not expect to violate any voltage or power breakdown levels of the devices. During initial commissioning of the processor, the multiplexer will be in the control room, but we will study the feasibility of placing it in the ring. If it can be adequately shielded from radiation, the multiplexer will only require one high quality cable from each BPM to the control room. The only signal paths that will vary from button to button will then be a short cable to the multiplexer and the switches themselves.

2.3 *RF Conditioning*

The processor will heterodyne the RF signal down to an IF of 6.4025 MHz, where its amplitude will be measured.

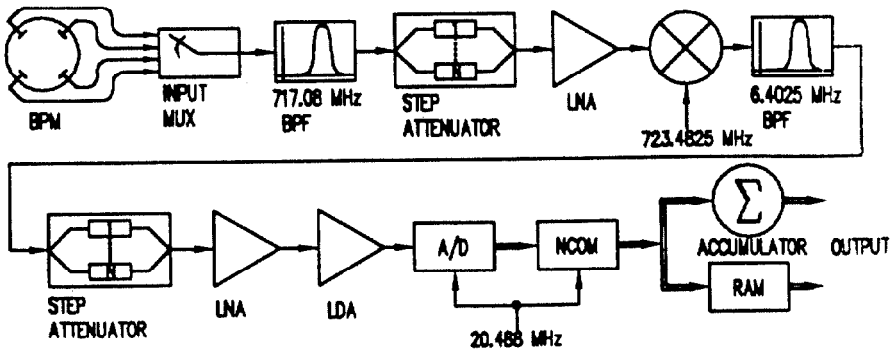

Figure 1: Processor Block Diagram

We use a dielectric resonator band pass filter, a 5 section Chebyshev filter with a 1% bandwidth and 7 dB insertion loss at 717.08 MHz, to limit the out of band input power. In order to condition this signal for a 10 dBm image reject mixer, we want to set its power level to a maximum value of -10 dBm. We use a combination of a low noise, fixed gain amplifier and a FET step attenuator to keep this level in range. Our calculations and measurements lead us to expect that for our normal operating range of currents we will always have a -10 dBm signal at the input of our mixer. We chose a fixed gain amplifier and attenuator arrangement because of its overall lower noise figure than that of a variable gain amplifier. We chose a step attenuator over an voltage controlled variable attenuator because we require the more constant attenuation provided by the digital control rather than the fine adjustment offered by variable control. The operating values of the input power were chosen to be well below the 1 dB compression point of the amplifier and the 3rd order intercept of the mixer in order to maximize linearity of the system.

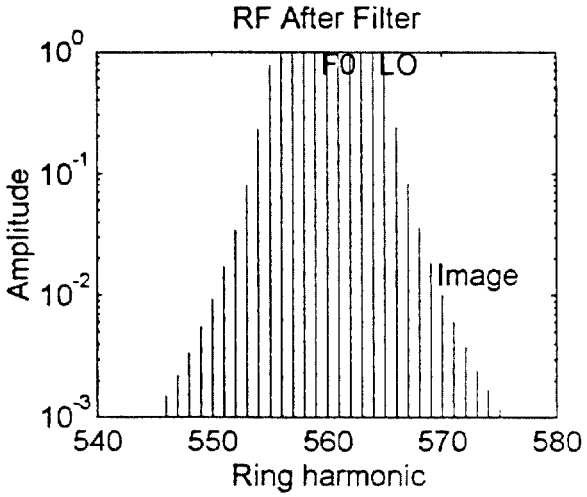

Figure 2: Input Signal After Filter

3 IF SIGNAL PROCESSING

Our IF was selected so that, using available commercial technology, we could digitize it directly without sacrificing the accuracy of our IF signal. Proper selection of frequency within this range gives us high accuracy, high bandwidth signals with a minimum of processing overhead.

3.1 *Analog Considerations*

Recent technological advances have produced monolithic 20 MHz, 12 bit A/Ds at reasonable prices. Therefore we tried to select our IF below 10 MHz, the frequency above which the A/D performance starts to roll off. The lower the IF, however, the harder it is to reject through filtering the mixer image of the desired frequency. Our RF bandpass filter rejects this image at the input by $\sim$ 40 dB (Fig 2), but by using an image-reject mixer, we reduce the IF image by another 30 dB. We chose an IF of 6.4025 MHz as a reasonable compromise where very high quality commercial video opamps and digitizers are available while good image rejection is still possible with simple circuitry.

For initial testing of the system, we will bandpass filter this IF and detect the power to determine the beam position. However this approach requires fixed hardware components to determine noise bandwidth, SNR, response time, etc., of the processor, which may vary for different processing requirements. Also, the data must still be digitized and some other intelligent controller must handle low level control of the processor. Our goal is to place all of these functions on board of one self-contained module that will interface with the rest of the control system only through the exchange of processed data and high-level messages over a standard digital bus.

3.2 *Digital Considerations*

With this processor, we want to be able to measure single turn phenomena that may be important for commissioning purposes or other machine studies, as well as the high accuracy, low bandwidth signals needed for orbit correction. Our digital signal processing will start with the digitisation of the IF. We have chosen the IF, and therefore the mixing frequency, to optimise this processing. When Fourier transforming band-limited data, one assumes that the signal that is transformed is a portion of an infinitely periodic signal. This is not the case for signals with arbitrary frequency content, and this periodic assumption 'contaminates' the transform with non-existent frequency components that are needed to make the sample periodic. To minimize this problem, one applies a 'window' to the data which de-emphasises the ends of the data sample. This windowing also contaminates the data, but hopefully less than an unwindowed sample. The signals we measure, however, are extremely periodic and we have access to the ultimate system clock, f_{RF}. By making use of this periodicity, we can choose to sample a signal that is periodic with respect to our clock, so that this signal truly is a portion of an infinitely periodic signal. With this method, we get a faithful frequency decomposition of the signal without windowing (Fig. 3). Since our signal is coherent while noise is

incoherent, N samples per revolution will increase our SNR by $\sqrt{N}$. Therefore, we chose our digitization frequency as $16f_{rev}$, or 20.488 MHz.

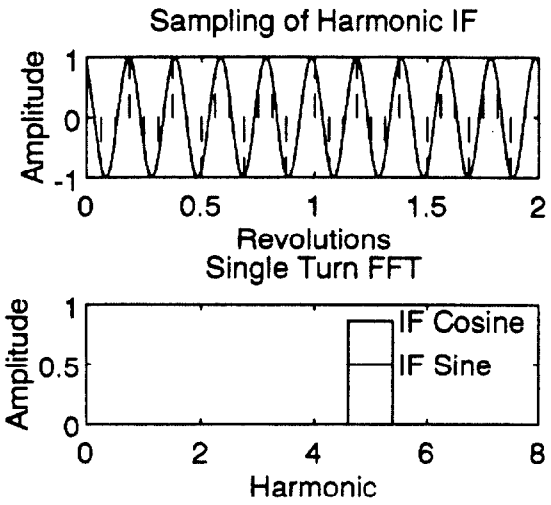

Figure 3: Harmonic IF gives faithful single turn FFT

When a perfect periodic signal is digitized, the output codes will have a periodic fixed quantization error. To minimize this error, the digitizer should sample the signal at as many values as possible. This means that the periodicity of the sampler should be as relatively prime as possible to the periodicity of the signal. Based on the criteria of image rejection, analog signal fidelity, periodicity, and digital fidelity, we chose $5f_{rev}$, 6.4025 MHz, as our IF.

3.3 IF Analog Conditioning

The remainder of the analog processing is to optimize the signal for the digitizer. We use a lumped element band pass filter at 6.4 MHz to pass the output of the mixer. This filter needs only act as an anti-aliasing filter for the digital processing that follows. Its specifications are not very strict since the nearest aliased frequency of the IF is 14.0855 MHz. We will set its bandwidth to $\sim f_{rev}$, since we want the ability to observe signals change that quickly. (In fact, we have been very conservative in all of our analog filtering specifications. Since each revolution harmonic carries the same spectral information, we are detecting synchronously with the ring RF, and the button response is essentially constant over the small bandwidths we are considering, the only contamination we would get from aliased signals is a uniform increase or decrease in the detected signals of all buttons. The major danger in this is that two signals may be exactly out of phase and cancel, but contamination on the order of ~40 dB would not affect our detection accuracy.) In the IF we again use a combination of a digital step attenuator and fixed gain amplifiers. Although there are variable gain video opamps with the same noise performance as fixed gain opamps, we are more confident in keeping the system gain constant with the step attenuators. If necessary, we will use a cascaded low noise amplifier to boost the initial IF signal and a low distortion amplifier to raise the signal up to the 1V nominal input value desired by the digitizer.

3.4 IF Digital Processing

We digitize the data at a high rate to improve the SNR of the system, but it would be very expensive to keep and process all information contained in these samples. From a beam dynamics point of view, all desired information is stored within a bandwidth of f_{rev}. Further, it is not clear what information we would ever need to investigate that happens faster than f_{rev}. We therefore use a digital mixer, the Harris HSP45116 numerically controlled oscillator/modulator (NCOM), to beat our IF frequency down to baseband once per revolution period. The NCOM takes as input the digital word representing the real signal sample and internally multiplies it with the appropriate sinusoids to output 16 bit real and imaginary values that represent the amplitudes of the quadrature components of the IF. We then both store into RAM and accumulate these values at an f_{rev} rate. The accumulated sum is the filtered value of the IF, the width of which is determined by the number of samples taken. If we want to look at dynamics of the BPM signal, or do a post- mortem on a beam loss, we then have turn by turn digital data stored in RAM that can be processed by other, more intelligent boards in the crate. The AMD29200 32 bit microcontroller is our BPM system controller, since it can acquire, accumulate, and store the 32 bit data words at the f_{rev} rate, as well as handle the low level control requirements of the processor.

4 SYSTEM TIMING

The timing generation of the system is straightforward. To generate the synchronous signals for our clocks and local oscillators, we divide down our f_{RF}. For signals not obtainable by straight division, we use direct digital synthesis (DDS) chips to generate the locked frequencies from f_{RF}. Switching of electrodes will all be done at increments of the revolution period and the processor will sample each electrode for multiples of this fundamental period. These values can, of course, be dynamically changed through software. We plan to package this controller in a format that will interface to a VME environment. Once this decision is finalized, we will use standard interface logic to connect the processor to the control system.

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6 REFERENCES

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