RAMPING CONTROLS FOR THE IUCF STORAGE RING

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ABSTRACT

When the IUCF Cooler Storage Ring operates as a synchrotron, 97 power supplies must be ramped over their entire operating range. The system described here does that by driving 16-bit isolated DACs through a 256 vector arbitrary waveform; each RAMPDAC module will store eight such waveforms and can be downloaded in a few milliseconds. High speed 16-bit ADCs can sample any DAC for analysis and graphic display. Total system cost: $45000.

INTRODUCTION

When IUCF's 200 MeV cyclotron was expanded to include a synchrotron storage ring (with, of course, electron cooling), the control system was forced into the realm of periodic phenomena. The transition was from control of an essentially DC machine to a machine involving 100-odd ramped power supplies synchronized to a master timing system. Trips were made to Fermilab, CERN, and Celsius to explore options, but the ramping system we arrived at was tailored to our own particular needs.

With 0.2% acceptance, our ring needed good DAC resolution and stability. Our power supplies required isolated control voltages. Cost was an important factor, as was manpower: we needed something easy to develop, construct, de-bug, and operate. Microprocessor controllers were considered, but were seen as an added complication that would confer no benefits in a small system with central control (more on this below). Our answer to ramping, designed and built at IUCF, has excellent performance at $300 per channel.

THE IUCF "RAMPDAC" FUNCTION GENERATOR CARD

GENERAL DESCRIPTION: Our solution was functionally similar to CERN's early GFA modules but with several improvements[1]. Each card can be programmed to generate a waveform made up of 2048 vectors. Vectors are specified by slope and endpoint. The first 2k RAM (slope) controls a rate multiplier operating from a 4.0 MHz clock (figure 1.); its output drives an up/down counter which in turn drives (through digital isolators) a 16-bit monolythic DAC. The second 2K RAM (endpoint) feeds a magnitude comparator, which is also fed by the U/D counter outputs. When the counter outputs match the current RAM endpoint, the address counter is incremented and a new slope/endpoint pair controls the DAC.

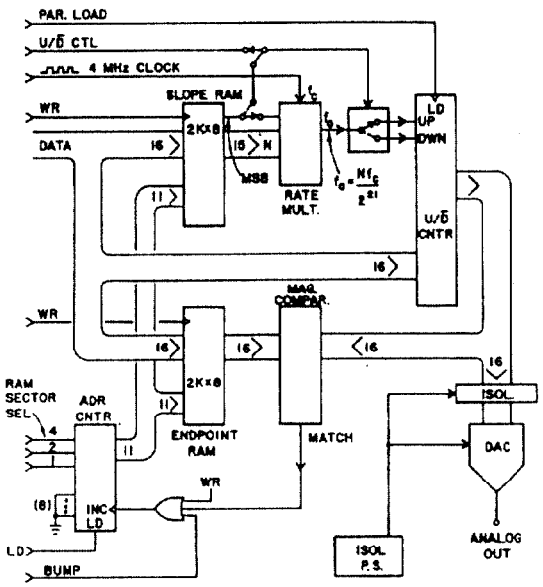

Figure 1

Because none of our ramps require 2048 vectors, we divided the RAM space into eight sectors of 256 vectors each. Hence each card will store eight separate functions, or ramps. This number can be further increased, if needed. With the rate multiplier clock turned off, each module can act as a conventional control DAC since the U/D counter can be parallel-loaded with a 16-bit word from the console.

PERFORMANCE: The pulse output to the up/down counter has a frequency equal to m*f(clock)/2**21, where N is the number presented to the rate multiplier by the slope RAM. Hence with a 4.0 MHz clock, the maxiuum frequency is 125 KHz, which will ramp the DAC from 0 to 10.0 volts in 0.52 seconds (a slope of 19.2 volts/sec). This maximum slope is more than we presently need but it could easily be increased by a factor of 20 by bypassing a divide-by-eight on the RM output and increasing the clock frequency. For 16-bit slope resolution each ramp must be monotonically increasing or decreasing, but a switch-selectable option allows the MSB of the slope RAM to become the up/down control bit. In ordinary operation the up/down bit is under system, and not card, control. See figures 2 and 3 for examples of monotonically increasing card outputs using all 256 vectors of one RAM segment. The vectors were derived from obvious analytic functions.

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Figure 2

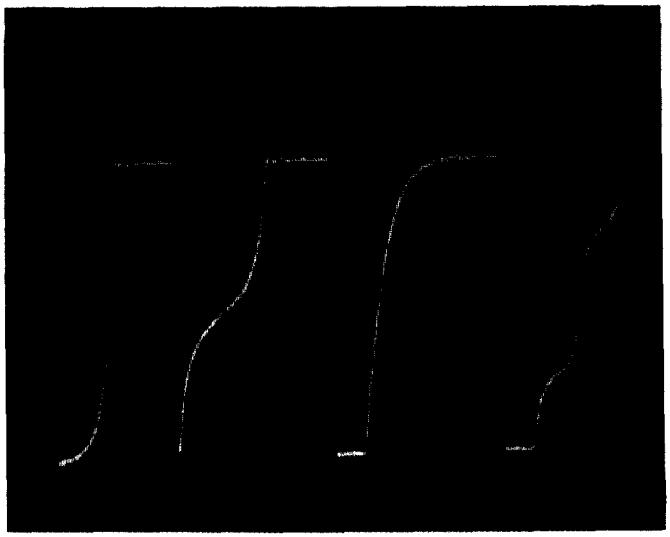

Figure 3

COMMENTS ON MICROPROCESSOR CONTROLLERS: We were told at Fermilab that one of their cards achieved 1000 writes/sec to the DAC it controlled. As mentioned above, our U/D counter can write 125,000 times/sec to the DAC it controls. We worried about "lumpy" DAC output at high slew rates as opposed to the smooth transitions of a counter. Our thought was to make the card 'dumb' and let all calculations be done by a computer that is designed to do calculations. These calculations, after all, need only be performed once for a given energy, at a cost of two minutes. However, I fear that we have, in the ramping area, fallen off the fashionable microprocessor bandwagon.

CONTROL SIGNALS: Each card receives a strobe with each transaction which it must return; if the strobe does not return, a sonalert beeps and a watchdog circuit returns the strobe. Defined card operations are PARALLEL LOAD, LOAD SLOPE RAM, LOAD ENDPOINT RAM, INCREMENT ADDRESS COUNTER. Global control signals which affect all cards are: GATED CLOCK, LOAD ADDRESS COUNTER (with 1 of 8 RAM sectors), CLEAR (rate multiplier, div-by-8), UP/DOWN, INCREMENT ADDRESS COUNTER, RAM ENABLE.

PHYSICAL LAYOUT, OPTION: The RAMPDAC card is sized for an Augat R-series wire-wrap bin. Each three-layer card is roughly 19 X 23 cm and contains 50 chips. Most chips are LS TTL; the DAC is C-MOS (Burr-Brown DAC 701). Total cost is roughly $300. A second version of the card uses a single analog isolator on the DAC output in place of the 16 digital isolators; this card has more noise and lower resolution (13-bit?) but saves a power supply. It is used mainly on steerers and hexapoles. Cards of either type have the option of unipolar (0 to +10 volt) or bipolar (-5 to +5 volt) output.

To date, we have had to build two identical 'special' cards. These cards make available the 16 bits of the up/down counter, via differential drivers, to devices that cannot use the on-card DAC. One device is the ramping RF digital frequency synthesizer; the other is the dipole power supply. This supply requires a DAC with ulta-high accuracy, stability, and linearity (Analogic MF8116) which resides in the power supply but is ramped from the special RAMPDAC card.

SYSTEM LAYOUT

At present our ring has a single PDP 11/73 controls computer. One half-size Q-bus card links this machine to the RAMPDAC control block via differential drivers. The PDP-11 can load a word into any card (memory or U/D counter) in 1.5 us. Hence slope and endpoint download could proceed at 660 KHz if the software permitted. Actual download time is slower but negligible; the entire array of 108 cards can be loaded with a new ramp set in a few seconds.

The RAMPDAC cards are in nine bins of twelve cards each; the 108 cards presently deployed take up two standard 19" racks. This includes isolation power supplies, fans, and the download control bins. Six of the bins contain a total of 72 of the higher resolution digitally-isolated cards; each of these six bins has directly undeneath a chassis with 12 small power supplies, because each card requires a supply to power the isolated DAC. The remaining three bins contain a total of 36 of the lower resolution cards which use an analog isolator (AD 289 L) on the output of the DAC; the isolator contains its own DC/DC converters and so these cards require no isolation power supply.

TESTING AND OPERATION

TESTING: The Controls hardware group at IUCF during ring construction consisted of two Engineers and four technicians. Perhaps one third of their labor went into construction and testing of the RAMPDAC array over a one-year period. (Prototype development went on for two years before that.) Each card was put through six separate tests, the final two being the generation of wildly improbable test ramps. An off-line test station was developed using a Micro-PDP 11/24+ and spare download/control boards to enable testing to go on at any time without typing up the Controls computer.

OPERATION: At present (May '88) our ring is undergoing developmental runs. The ramping hardware has successfully ramped protons from 45 to 150 MeV several times; the next goal is 45 to 287 MeV. There appears to be no serious problem with this system. Software continues to be developed and will be reported elsewhere.

RAMP VERIFICATION

Four fast (35 us) 16-bit ADCs are used to verify RAMPDAC performance. Each ADC can be multiplexed to any of 24 RAMPDAC outputs and used to generate a graphics trace of that output at the Control Console. The multiplexers are mercury-wetted relays. A test program can be run which checks the entire RAMPDAC array for dropped bits in about ten minutes. In addition, of course, the Ring power supplies which the RAMPDAC boards control have shunt-derived readouts (in amperes) at the console.

ACKNOWLEDGEMENTS

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References

(1) J. Bosser, E. Bracke, L. Burnod, J. Cadoz, E. d'Amico, G. Mugnai, J. Savioz, "The SPS Function Generators", CERN-SPS/ABM/77-, August 1977