

CONVERSION OF THE SPS TO A MULTICYCLING ACCELERATOR

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1. ABSTRACT

In order to fulfill its role as an injector for LEP and to maintain the current physics program the SPS must pre-accelerate lepton beams in parallel with the current fixed target operation mode. Preparations for multicycling of the SPS include considerable changes to the controls infrastructure of the accelerator. This paper examines in particular the design of the new timing system and general purpose function generators, and reports on initial experience with these systems.

2. INTRODUCTION

During more than a decade of operation the SPS has evolved from a high energy proton synchrotron to a storage ring colliding proton and antiproton beams at 630 GeV c.m.s. with lifetimes in the order of a day, a pulsed colliding beam facility where the energy of the beams was varied between 900 and 200 GeV c.m.s., and more recently as a source of ion beams, oxygen and sulphur having been accelerated to 200 GeV per nucleon. These various modes of operation of the SPS have been achieved by scheduling the various activities of the machine sequentially over a calendar year.

In order to satisfy the current physics program and to assume a new role as a pre-accelerator of lepton beams for LEP, it is necessary to introduce interleaved running of the SPS. The LEP machine is expected to require filling with leptons every 4 - 5 hours; this stacking will extend over a period of around 30 minutes with regular injection of batches of electrons and positrons. This pattern of operation, although incompatible with storage of hadrons in the SPS for periods of around one day, can proceed interleaved with 450 GeV proton fixed target operation as there is currently around 5 seconds of dead time in the accelerator cycle of 14.4 seconds.

Figure 1 shows how the main magnet system of the SPS is pulsed during trials for LEP filling. Superimposed on the recovery time after the descent from 450 GeV are 3 lepton acceleration cycles which correspond to the injection of these particles at 3.5 GeV and their acceleration and ejection towards LEP at 20 GeV.

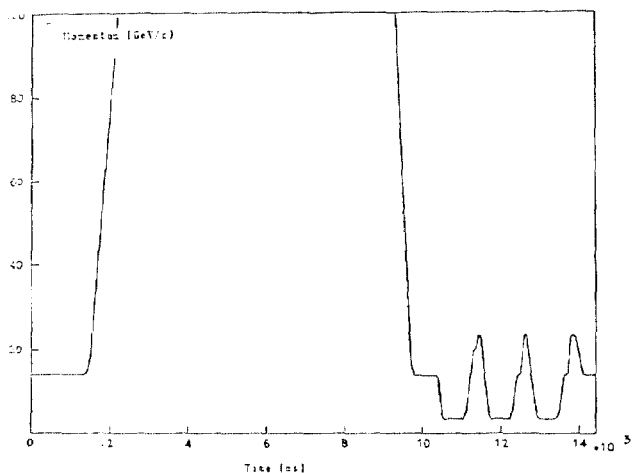


Fig. 1. Main Magnet Supercycle (truncated at 100 GeV)

3. TIMING SYSTEM

To favour a simple and coherent synchronisation of the SPS and LEP accelerators the new timing system [1] is used for both machines. The principal component is the central Master Timing Generator (MTG), which broadcasts synchronisation information to the numerous components of the accelerators. These are distributed in the surface buildings (BA's) around the 35 kilometers total circumference of the two machines. This information is encoded onto a message frame, allowing the information to be divided into several types, the most important of which are the msec clock and the timing events.

Essential to the services provided by this system are the programmable timing receiver modules which receive all the timing events and compare them with a pre-loaded subset. From a valid comparison the module may generate an interrupt to a microprocessor and/or generate a pulse to trigger external equipment. Alternatively it might delay the action for a given number of clock pulses. In both cases the requested action is referenced to the msec clock. Events decouple the settings of the receiver modules from the particular mode of operation of the accelerator; they denote operations such as injection, start acceleration and extractions.

The message frame is the principal interface between the timing system and the accelerator or equipment oriented view of this system. A major concern in the development of the timing system was that it should attach as little meaning as possible to the messages being broadcast, whereas for the user the functionality of the system depends strongly on the interpretation. The timing events are coded onto the 4 byte frame as follows:

- Message group, eg. SPS BEAM MONITORING, LEP RF.
- Event name, eg. INJECTION, TRANSITION.
- Cycle type, eg. PROTON, ELECTRON.
- Cycle type number, this serves to distinguish cycles of the same type within a supercycle.

Other information such as a supercycle count used for tagging data acquisitions and calendar time are broadcast on the same frame.

3.1 MASTER TIMING GENERATOR

The timing generator card is a single intelligent board which plugs into the IBM PC bus and drives the timing system. It consists of a motorola 6809 microprocessor controlling on-board (56 Kbytes) memory and a small number of multi-function registers. The National Semiconductor DP8342 serial transmitter integrated circuit is used to encode the message frame. The frames to be transmitted are loaded into the memory and the MC6809 loads them into the DP8342 transmitter at predetermined times. Sixteen external hardware entry points are provided which are used to trigger asynchronous timing messages such as "EMERGENCY BEAM DUMP". Duplication is provided by having two identical MTG's. The "hot" spare can be selected remotely via the control system. A similar third MTG is used for software development.

3.2 TIMING INTERFACE

The basic purpose of the interface unit is to receive the timing messages from the multidrop timing line and to pass on the treated data to the timing receivers. The treatment consists of first checking that each Manchester encoded frame received is error free and then converting and stripping the frame down to a four byte TTL binary coded message.

Two registers are accessible to the users microprocessor, a single byte error register and a three byte register containing the current supercycle count number. This number will be read each cycle by the IBM PC which generates the timing signals, thus ensuring that the broadcasting system is working correctly. For simple applications the interface card can be used by itself. Two hundred interfaces, conforming to the G64 standard have been manufactured and over 50 for the IBM PC standard.

3.3 GENERAL TIMING MODULES

The TG3 [2] range of general timing modules are based on a Motorola MC6809 microprocessor controlling an MC6840 triple 16 bit counter (hence the 3). The TG3 receives SPS/LEP timing messages via an interface unit and compares each received message with a set of pre-loaded parameters which are contained in a portion of the on-board memory labelled the event table. The parameters are similar to the transmitted timing messages which consist of 32 bit words organised as four bytes. If a comparison is valid the requested action, associated with that particular condition, is initiated. Normally the action will be to interrupt the users microprocessor and/or to transmit a trigger pulse to some external equipment. To date, over 300 G64 modules have been received and 250 VME TG3s.

3.4 SIGNAL DISTRIBUTION

In order to reduce cabling costs around the SPS and LEP, an integrated communications system is being installed [3]. This system is based on Time Division Multiplex (TDM) techniques. The links used to transport the timing messages operate at 2.048 Mbit/sec. As the timing signals are transmitted at 512 Kbit/sec, the extra capacity is used to permit correction of single bit TDM transmission errors.

The links provided specifically for the SPS/LEP timing system will normally be configured in a double ring topology, one ring for each accelerator. The links on each segment of the rings are inherently full duplex; this feature is exploited to provide two independently routed signals, following clockwise and anti-clockwise around each ring. These alternate signals will be used in the equipment interface for added reliability in case of link failure. The incoming data streams for the two channels will in general have been transmitted along different physical paths, clockwise and anti-clockwise around the two machines. A path delay compensation circuit introduces appropriate delays to the channels corresponding to the transmission times of the two paths. This ensures that, in the event of a switch to the alternate channel, the timing signals are not perturbed.

Within each building the timing messages are distributed via twisted pair cables. The signals conform to the electrical characteristics defined by CCITT Recommendations V.11 and X.27 and EIA specification RS-485. Although this standard is designed for multipoint transmission/reception on long bus lines in noisy environments, the d.c. common mode rejection has been substantially increased by the adoption of a.c. coupling on the users' receiver interface.

4. THE MUGEF SYSTEM

Many components of the accelerator must follow a continuously varying reference function. These dynamic parameters are usually computed by various mathematical models and sent over the control network to the general purpose multicycle function generators known as MUGEF's. This recent development was designed to satisfy a large variety of applications requiring an accurate, dynamic, programmable reference and to provide general control of the SPS power supplies. It has replaced a variety of monocycle function generators throughout the accelerator.

Rapid commutation between functions pertaining to the different beams interleaved in the accelerator supercycle is the major new requirement satisfied by the MUGEF system. To achieve this without provoking an excessive load on the controls network the MUGEF's supply powerful, local intelligence which is decentralised in the BA's. They are pre-loaded asynchronously and the different functions are stored locally in tables activated and synchronised within the SPS supercycle by the timing system. Labelling of the tables is done in a manner which is consistent with the conventional usage of the bytes in the timing event.

Figure 2 illustrates the function being used to pilot one of 5 chromaticity correction sextupole families during a fixed target run. The function generators are used to provide references for over 600 main ring and transfer line magnets as well as the radio frequency system. Because of the range of applications a series of conflicting requirements have had to be settled during the development. While the references for the radio frequency system only need a precision of $\approx 1 \times 10^{-2}$ the references of the orbit dipoles for lepton injection at 3.5 GeV and proton ejection at 450 GeV must be precise to a few parts in 10^5 .

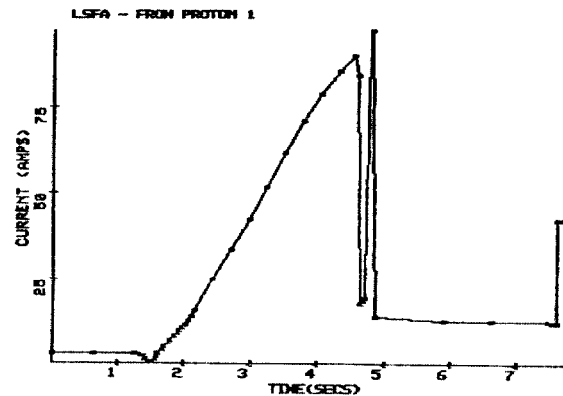


Fig. 2. Chromaticity Correction Function

The main characteristics of the function generators as presently installed are as follows: a 16 bit DAC working between $\pm 10V$ gives an amplitude resolution of $\pm 3 \times 10^{-5}$; the times of the points in the functions are specified in a 16 bit word which allows functions of up to 65 seconds total length with 1 msec resolution. If this becomes a restriction the function duration can be extended by using 2x16 bit words for this purpose. Figure 3 shows the functions and vectors definition. Notice that any two points of the grid can be linked by a vector and there is no limit on the slopes that may be specified, even discontinuities are allowed.

In addition to the function generators each MUGEF installation is also equipped with an intelligent analogue acquisition system which provides independent digitalisation of the output of the function generator and the device which is being driven. This facility is

a powerful diagnostic for localising faults to the MUGEf or the users' equipment. The MUGEf project also includes the provision of a general and intelligent control facility for switching and status acquisition of the SPS power supplies. This is already in use for the 220 closed orbit correction magnets.

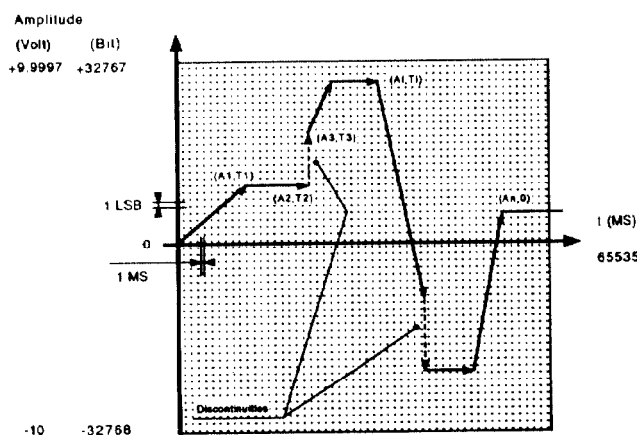


Fig. 3. Functions and Vectors Definition

5. MUGEf IMPLEMENTATION

The MUGEf approach [4] consists of a VME bus structure linked to the SPS control network through the MIL 1553-B multidrop bus. Each crate can house up to 64 independent 16 bit function generators with their ancillary equipment. Less than 20 MUGEf crates are required to control all the ring and transfer line elements associated with the current dynamic operation of the accelerator. We distinguish four sections in a MUGEf crate: the master CPU and interfaces, the ramp generation cards, the power supply control unit and the analogue acquisition system.

5.1 MASTER CPU AND INTERFACES

This section contains three VME units: a CPU card with a 68000 microprocessor and 1 Mbyte RAM, the master of the crate which controls all communications; a VME to MIL 1553-B interface linking the MUGEf to the SPS computer network and hence to the control room; and a TG3 timing module which synchronises the generation of the functions to the supercycle. Functions in user format are sent asynchronously from the main control room to the master CPU of the MUGEf crate. Here they are converted to hardware format and on a trigger from the TG3 are sent synchronously to the ramp generation (RG) card. Two timing events, the warning and the start, are associated with each of the tables employed for the current supercycle. On receipt of the warning the master CPU sends the new function to the RG.

5.2 RAMP GENERATION CARDS

This card is the heart of the MUGEf system. All the real time tasks related to the generation of the functions are carried out here. Up to 8 RG cards can be housed in a MUGEf crate. The RG module has a dedicated 68000-10 MHz microprocessor, without wait-states, and 64 of Kbytes RAM, holding the function tables. This CPU can drive up to 8 independent on-board 16 bit DAC's. By inserting 1 to 8 DAC's a user tailors his requirements compromising between ramp amplitude resolution and number of independent functions. This is currently done at the SPS, where RG cards with 1,2,4 or 8 DAC's are housed in the same crate. No booster amplifiers are required, the DAC of each function generator is able to drive at least 70m of twisted pair cable with a good margin of gain and phase stability.

Functions are generated digitally by very fast dedicated algorithms. The microprocessor computes the independent ramps in a time-sharing fashion and sends

the new amplitudes to the corresponding DAC's every 'T' microseconds. Four different algorithms, all resident in the RG's 64 Kbyte EPROM, associated with 1,2,4 or 8 DAC's per RG have been developed. The updating interval 'T' varies between 5 and 250 microseconds.

5.3 POWER SUPPLY CONTROL SECTION

The power supply commands (ON, OFF, RESET, etc) and the reading of the corresponding status bits are carried out by one single-width VME card. Up to 64 power supplies can be controlled in "daisy-chain" fashion using only one cable linking them all. There is no need for a local intelligent interface in each individual power supply. Up to 8 commands and 16 status bits per power supply are allowed with possible extensions to 32 and 64 respectively.

5.4 ANALOGUE ACQUISITION SYSTEM

The analogue acquisition section consists of three cards. The CPU card, with a 68000 microprocessor and 512 Kbytes of RAM, communicates with the master CPU of the crate and controls two analogue conversion cards. These are equipped with a 12 bit, 25 microsecond ADC converter and an analogue multiplexer with 64 differential inputs. This allows analogue acquisition of up to 64 function generator DAC outputs and the corresponding magnet currents. The system is partially installed at the SPS for the closed orbit application. It provides a complete, local and intelligent self check system of the entire MUGEf crate.

6. CONCLUSIONS

Initial experience with these systems has been very satisfactory. The timing hardware and signal transmission system have proved very reliable. The large bandwidth of the message frame has allowed detailed synchronisation problems to be tackled centrally and is being exploited to extend the timing system to a general fast message broadcast facility.

The subdivision of the extensive local memories in the function generators into tables dealing with the different interleaved cycles within the SPS supercycle follows the convention for organising the timing events providing an harmonious infrastructure for the users. The flexibility designed into the configuration of the ramp generation card has lead to a single and cost effective solution for a wide range of applications.

7. ACKNOWLEDGEMENTS

The new implementation of the timing and function generator systems is the result of over a decade of evolution at the SPS during which time many people have contributed ideas and effort.

8. REFERENCES

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