OPERATIONAL EXPERIENCE WITH THE DISTRIBUTED CONTROL SYSTEM OF THE MILAN SUPERCONDUCTING CYCLOTRON

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ABSTRACT

A two level network architecture has been implemented for the control of the Milan Superconducting Cyclotron. The first level consists of an optical Ethernet network interconnecting a set of multicomputers based stations (PCS) each one dedicated to the control of a particular accelerator subsystem. The second level consists of a serial SDLC-like bus (Bitbus) used to interconnect microcontroller based interfaces (analog and digital), fitted inside each single equipment, to the PCS related to them.

Introduction

The architecture of the control system designed for the operation of the Milan Superconducting Cyclotron (S.C.) has been extensively discussed in other papers [1,2]. For the sake of completeness, we just recall its main features.

The computer control consists of high performance, multicomputer based control units interconnected by means of a standard local area network. The functional criterion has been adopted to distribute computing power. The compact size of the S.C., in fact, makes effective to organize similar equipments, or a complete accelerating machine subset, under the control of a single computing unit. Moreover, since critical interlocks and severe real-time applications are under the control of single control station, indipendent operations can be provided in case of failure of the network.

A schematic lay-out of the Milan control system is shown in fig.1. At the floor level, the control stations perform high speed data acquisition from sensors, convert measurements to engineering units for data base updating and monitoring, and provide complex real time controls. Some rules for the hardware (h/w) have been defined in the architecture of the control stations: the card cage bus is the standard IEEE 796 (Multibus I) and the cpu are from the Intel family of 16 bit microprocessors (μP). The equipments can be controlled, directly connected to a microcomputer card-cage, or can incorporate a microcontroller (μC) board (based on Intel 8051) which communicates with the main peripheral unit on a fast serial link (Bitbus).

A particular control station is a high performance programmable logic controller which takes care of the technical plants through Serial Interface Modules for industrial I/O boards driving. At the plant supervision level, a console node provides fast access to every machine parameter, by means of interactive devices, and data display and alarm information.

A DEC μVAX II is the supervisor of the control system and is connected to the laboratory computer cluster for off-line data analysis.

The elements of the computer control system needed for magnet excitation and subsequent median plane magnetic measuremets, have been completely realized. They consists of the following stations: main coils and trim coils power supplies, cryostat and superconducting coils diagnostic, quench detection system, cryostat vacuum and, at the higher level, the console and the μVAX II. The stations have been connected to related cyclotron equipments and the control system has been running error free for more than 500 hours. In this paper we discuss the experience gained during system development and during this period of operation.

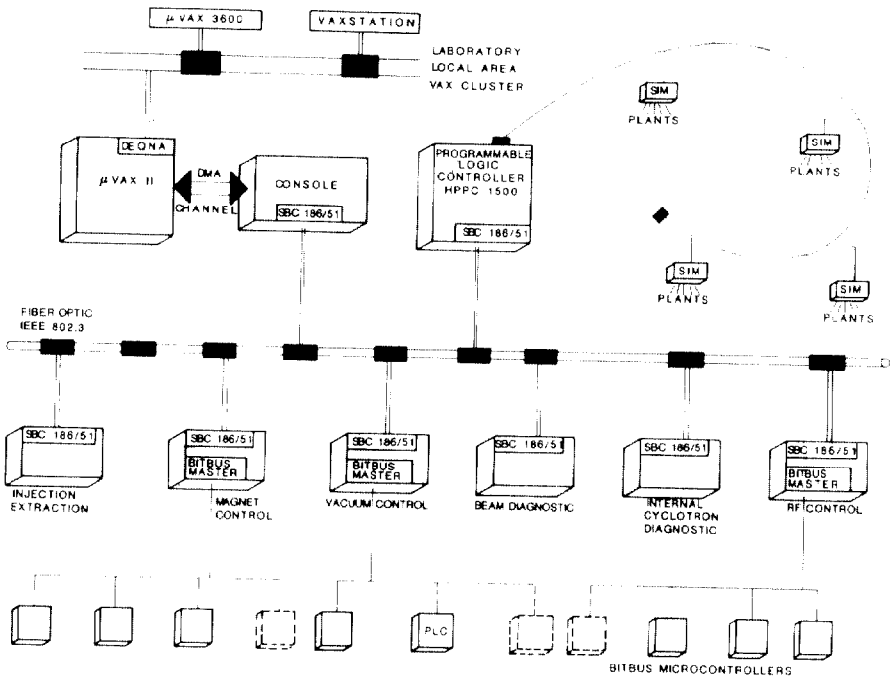

Fig. 1 The control system architecture

The Optical Network

In a distributed environment the network becomes a critical element. The choice of topology, protocol, data rate and transmission media can affect the overall performance of the control system. A good solution for our requirements has been found using the IEEE 802.3 standard communication protocol (Ethernet). An optical transmission media (graded index optical fibers and passive optical star coupler) has been preferred to the standard coaxial cable.

Doubts have been expressed about the suitability of Ethernet in a real-time control environment [3]. Non deterministic access to the network and poor short messages performance have been pointed out as the major drawbacks. For the Milan control system these limitations have not been considered significant, as the number of nodes should be lower than 15 and the most critical time controls are performed locally in the peripheral station. The standard interface between the control stations and the Ethernet network is an Intel board (iSBC 186/51). Network services are managed by application programs (burned on EPROMS), conforming to the ISO-OSI protocol up to the transport layer. Particular care has been devoted to the development of the software (s/w) implementing upper layers. Fast transmission rate, reliable data transfer and capability to reconfigure virtual circuits between the stations dinamically in case of nodes leaving or joining the network, are the main features.

Fig. 2 shows the performances (carried out with real applications running) obtained in our system for memory to memory transfer between four stations for packets of more than 1500 bytes. The cost in protocol overhead to send a short messsage, that fits in one physical packet (1500 max. bytes), is essentially independent of the message length. For these messages, which are particularly used in distributed control system to send commands or read status, it is significant to quote the messages/s figure rather than the Kbit/s one. In our system we have measured a performance of 50 messages/s.

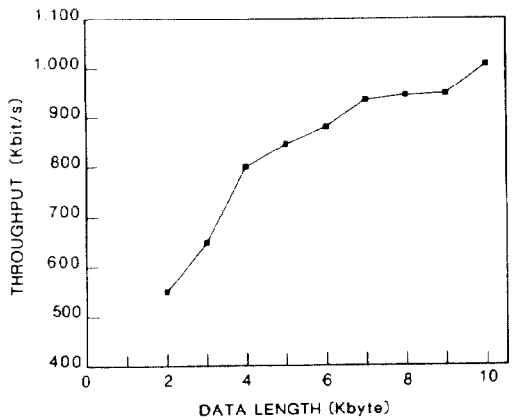

Fig. 2 Ethernet performance

Superconducting Coils and Trim Coils Power Supplies Control Station

A dedicated control station has been realized to perform the control of the currents in the superconducting coils and trim coils. Main coils power supplies, designed and realized in our laboratory, can generate currents up to 2000 A (20 V). The required stability of $\pm$ 1 Gauss for the main magnetic field demands a current stability of $1 \cdot 10^{-5}$. The stability of the power supplies has been achieved by means of a current control loop. A 18 bit DAC (DAC 1138K) supplies the reference current signal and 16 bit ADC (ICL 7104) reads the current value in the coils.

A µC has been dedicated for each section to drive both ADC and DAC allowing to respect the tight timing required for operations at variable current rates. Another one has been devoted to control start-up and shut-down sequences of the power supplies and to monitor continuosly alarm states. An 8086 based SBC has been chosen as the master element of the station.

The current control loop has been successfully tested in stationary state shorting the power supplies, in order to simulate the low resistance of the superconducting coils.

Test and maintenance of the power supplies have been guaranteed by a µP based device. It just allows to drive DACs in order to set currents at prefixed rates. The control of the 28 trim coils power supplies, delivering currents between 400 A and 500 A with voltages ranging from 36 V to 48 V, has been implemented by means of 5 dedicated µC based boards providing all the operations needed for their working.

Superconducting Coils and Cryostat Internal Diagnostic

A diagnostic system has been required to obtain a detailed knowledge of the behaviour of the superconducting coils and of the cryostat during cool-down and at the LHe temperature. Thermal stresses, due to non uniform refrigerant inlet, may cause leaks in the weldings or failures in the coils components if not well controlled, so an exauxistive map of the temperature and stresses inside the coils vessel must be known during operations of these elements. A PCS has been designed to comply with this requirements. It provides signal conditions modules for the various gauges and has to deal with 90 analog and 70 digital I/O points. An Intel 80286-8 Mhz Cpu has been choosen for local data elaboration. Performance evaluation of the acquisition and linearization s/w (along with continuosly running self-test programs) has shown that the total acquisition time (~3 sec.) for a whole temperature/stresses map is well within the requirements.

Quench Detection System

A control system has been designed and tested to protect the superconducting coils against damage due to the their revert to the normal state (quench). In the event of a quench it is mandatory to switch off the power supplies in a very short time and to waste energy (40 MJ) to a dumping system. A fast acquisition of relevant parameters will start at the same time allowing to analyze later the phenomena.

As the troubles of the control devices may produce dramatic effects, a redundant fault-tolerant architecture has been chosen. Signals, taken across the coils, are compared with different thresholds and gives to an 80286 CPU the trends of the situation. If a dangerous condition is envisaged the computer starts coils protection sequences. In case of failure of the computer, an analogic system, takes the same action. Redundancy has been also implemented taking into account the pressure in the LHe vessel as a phenomena to foresee a possible quench transition. The whole system, which is now connected to the superconducting coils, has been successfully tested.

Console

Full operation of the accelerator requires to control a lot of parameters from the control room. A large console, consisting of nine elements has been realized (fig. 3). The console has been implemented as a µP based station, whose structure, which is the same as the control stations, allows an easy expansion following future needs. The central intelligence consists of an Intel 80286-8 Mhz µP and 1 Mbyte of 0 wait-state RAM; graphic capabilities are provided by

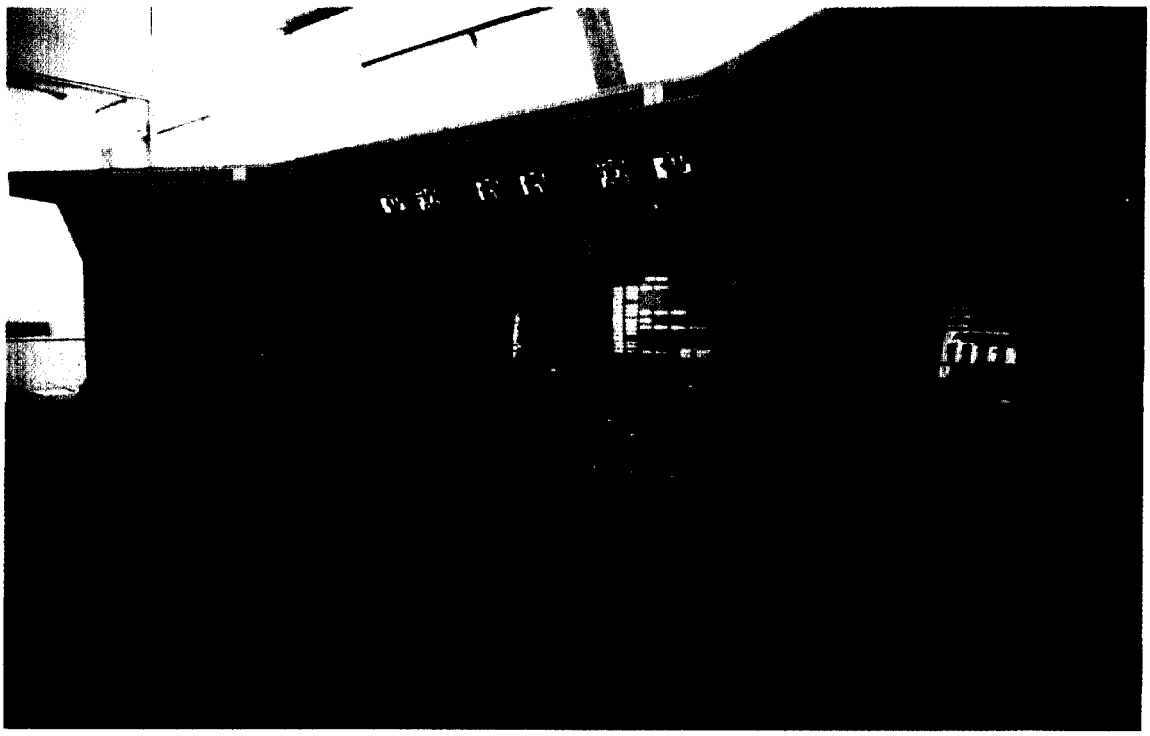

Fig. 3 View of the main console

means of a dedicated 80286 and 7220 coprocessor. Operator inputs are handled by a touch panel and a number of Intel 8051 µC based boards, interconnected on a Bitbus multidrop layout.

A µVAX II, dedicated to maintain a centralized database, to set-up the accelerator and to make correlation calculations on the machine parameters during operations, has been connected, by means of a DMA link to the console.

The s/w has been structured in modules, related to specific functions, as network managing, database access and communication with the µVAX II, operator inputs and display generation. Shared memory architecture allows an easy exchange and update of data and commands between different tasks. This architecture allows to send a 5 KBytes of data for the accelerator set-up from the µVAX II to a PCS in about 130 ms, or to make effective a knob command to the field in 30 ms. When a task reads a data location in shared memory the information is never more than 175 ms old.

Software architecture

The design of the general s/w architecture for a complete control system has a considerable cost in manpower. Although h/w has been standardized to a great extent, this does not apply to the support that is available for the implementation of the control system s/w. The lack of available, suited standard to take as a reference forces the various control groups to write their own pieces of s/w. General rules defined for the Milan control system are the installation of a real time operating system (iRMX86) on EPROM in every CPU board, the use of PL/M as programming language, the development of a support for multicomputer structure and the organization of data in a simple database structure.

iRMX86 is an event-driven operating system, which provides to the user the capability to configure it according to specific requests. We have selected a part (19.8 Kbytes of size) devoted to process interrupt and to handle memory. Real time performances have been measured on an 80286 based SBC, giving an execution time of nearly 100 µs for interrupt latency, 200 µs to send a message to a mailbox and 190 µs to receive the control of a common resource.

A protocol for interprocessor communication on the Multibus I bus has been realized and tested. Main features have been the support of up to three masters, capability to exchange data between specific processes on different boards and the indipendence of the operating system. Moreover, each board is able to test operations of the other ones in the same card-cage and to notify troubles taking the appropriate actions. Measurements, taken during real operation, have shown the capability to exchange 155 blocks of 4 Kbytes of data per second giving a throughput of 5 Mbit/s. Assuming as a figure of comparison the time needed to move one of these blocks from two memory locations on the same board, we have a 30% of performance.

The database of the whole control sytem is spread all over the network and a global copy is kept in the µVAX II memory.

Conclusions

Experience gained during first operations of the computer control system has given us a measure of the capability of the system. Main hardware and software choices have been proved satisfactory. Modifications will be carried out mainly on the console element in order to take advantage of the 16 Mbytes address space of 80286. A new version of the Intel operating system will be installed. Design and implementation of the vacuum and RF control stations are currently in progress too.

References

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