LOW LEVEL RF SYSTEM DEVELOPMENT FOR SOLEIL

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Abstract

The Low Level RF system that is used in the SOLEIL storage ring consists in fully analogue "slow" amplitude, phase and frequency loops, complemented with a direct feedback. A fast digital FPGA based I/Q feedback, currently under development, will be implemented later on. The performance of both systems has been evaluated using a Matlab-Simulink based simulation tool. The computed and first experimental results are reported.

INTRODUCTION

In the SOLEIL storage ring (SR) two cryomodules (CM), each containing a pair of 352 MHz superconducting cavities [1], will provide the maximum power of 600 kW, required at the nominal energy of 2.75 GeV with the full beam current of 500 mA and all the insertion devices. They will be supplied with liquid Helium from a single cryogenic plant [2] and each of the four cavities will be powered by a 190 kW solid state amplifier [3].

Only a single CM was implemented for the SR commissioning [4]; that will allow to store up to 300 mA in a first phase with limited number of insertion devices. The second CM, which is presently under fabrication, will be implemented by mid of 2007 for reaching the nominal performance.

The Low Level RF system (LLRF) for phase 1 consists in fully analogue "slow" amplitude, phase and frequency loops, complemented with a direct RF feedback in order to insure the Robinson stability at high beam loading. A fast digital FPGA (Field Programmable Gate Array) based I/Q feedback, presently developed in collaboration with CEA, will be implemented later on.

The computed performance and the first experimental results for both systems are reported.

SOLEIL PHASE-1 ANALOGUE LLRF

A diagram of the SOLEIL phase-1 analogue LLRF is shown in Fig. 1. The slow amplitude, phase and tuning loops are similar to that used for the SOLEIL Booster.

The amplitude loop regulates the cavity voltage by controlling the RF input power level. A sample of the cavity voltage, from a monitoring pick-up, is detected and compared to a reference value; the error signal from the amplitude comparator drives, through a PID, a variable electronic attenuator, which controls the RF input power.

The phase loop compensates for the phase changes in the amplification chain. The RF signals at the input and output of the amplification chain are compared in phase and the error signal drives, through a PID, an electronic phase shifter. Another electronic phase shifter inside the loop path is used to keep the working point close to the middle of the range of the phase comparator. A mechanical phase shifter at the entrance of each of the amplifier chains allows controlling their relative phase, while another one, located at the master oscillator (MO) output, can vary the phase of the four RF plants, simultaneously.

The frequency tuning loop adjusts the cavity resonant frequency in order to compensate for the changes in pressure or reactive beam loading. This is realised by means of a mechanism, driven by a stepping motor, which changes the cavity length and therefore its resonant frequency. The motor is controlled in closed loop with the output signal of a phase detector, which is proportional to the phase difference between the cavity incident signal (from directional coupler) and the cavity voltage (from monitoring pick-up). The phase shifter inside the loop path provides an adjustable offset.

The options for operating in open or closed loop, with local and remote control, are provided for all the three loops. Their performances are listed in Table 1.

The direct RF feedback re-injects a sample of the cavity voltage at the input of the amplifier chain with proper gain, amplitude and phase, in order to reduce the beam loading effects and so move away the Robinson instability threshold at higher current (see next section). The fundamental component is rejected by proper setting of the variable attenuator, A_o and phase shifter, φ_o.

After a few weeks of SR commissioning [4,5], current up to 85 mA could be stored with all three slow loops active; at such current level, there is no need for the feedback loop, which was therefore kept enable up to now.

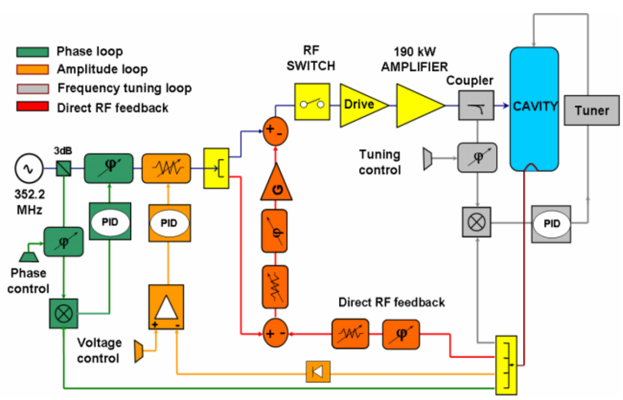

Figure 1: Block diagram of the phase-1 analogue LLRF

Table 1: Main performance of the SR "slow" LLRF loops

	Amplitude	Phase	Frequency
Accuracy	0.25 %	± 0.4°	± 10 Hz
3 dB bandwidth	350 Hz	1 kHz	0.15 Hz
Dynamic range	40 dB	± 80°	± 10 kHz

MODELLING AND SIMULATION

The nominal SOLEIL SR parameters for phase-2 (two cryomodules) are listed in Table 2. With superconducting cavities and heavy beam loading, SOLEIL operates close to the limit of Robinson instability at full beam current of 500 mA.

Table 2: Phase-2 SR parameters (with two CM)

RF frequency (MHz)	352.202
Harmonic number	416
Nominal energy (GeV)	2.75
Energy loss per turn (keV)	944 + 184 (ID) +22 (HOM)
Momentum compaction factor	$4.38\ 10^{-4}$
Energy damping factor, D	$6.88\ 10^{-4}$
Cavity loaded quality factor	10^5
R/Q per cavity (Ohm)	45
Beam current (mA)	500
Total cavity voltage (MV)	4
Synchronous phase (°)	73.6
Tuning angle (°)	-77.8

Microphonic disturbances have been measured on the SOLEIL cavities. An example of the cavity detuning signal spectrum is shown in Fig. 2 and the spectrogram of the major disturbance (around 460 Hz), which is likely related to a mechanical eigenmode of the cavity, is plotted in Fig. 3. The eigenfrequency associated to this mode may change according to the helium pressure.

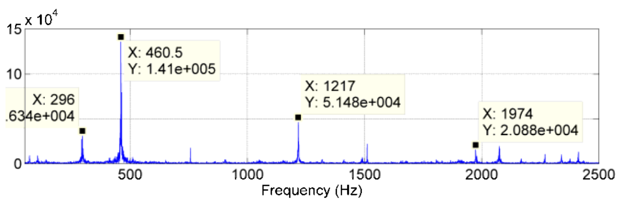

Figure 2: Cavity detuning signal spectrum

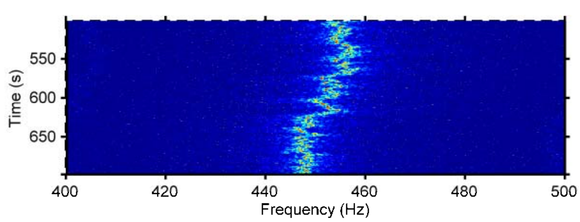

Figure 3: Spectrogram of a microphonic disturbance

A Matlab-Simulink based simulation tool has been developed in order to better understand the beam-cavity interferences in presence of disturbances or injection errors. In the model, real and imaginary parts of cavity and generator voltage, and their derivative are coupled :

$$\dot V_{cr} = \frac{V_{gr} - V_{cr} - V_{ci}\tan\psi}{\tau} \quad , \quad \dot V_{ci} = \frac{V_{gi} - V_{ci} + V_{cr}\tan\psi}{\tau}$$

where ψ is the detuning angle and τ the cavity filling time. The instantaneous single bunch beam loading gives:

$$V_{cr}^{\ +} = V_{cr} + \omega_{RF}\left(R/Q\right) q\cos\phi_b \quad , \quad V_{ci}^{\ +} = V_{ci} + \omega_{RF}\left(R/Q\right) q\sin\phi_b$$

where q is the bunch charge, ϕ_b the synchronous phase.

The synchrotron motion leads to:

$$\Delta E_i^{n+1} = \Delta E_i^n - V_c\cos\left[\phi_{b0} + (\delta\phi_b)_i^n - \phi_c\right] - \left(U_0 + D\,\Delta E_i^n\right)$$

$$(\delta\phi_b)_i^{n+1} = (\delta\phi_b)_i^n - \frac{2\pi f_{RF}\,\alpha}{f_0\,E_0}\left\{\Delta E_i^n - V_c\cos\left[\phi_{b0} + (\delta\phi_b)_i^n - \phi_c\right] - \frac{U_0 + D\,\Delta E_i^n}{2}\right\}$$

where U_0 is the energy loss per turn, D the energy damping factor, i and n defines respectively the index for bunches and turns. The feedback equations write according to the type of the feedback:

$$\tilde V_g = \tilde V_{g0} + G\left(V_{c0} - \hat D\,\tilde V_c\right) \quad , \quad \tilde V_g = \tilde V_{g0} + G_I\left(V_{c0} - \hat D\,V_{cr}\right) - jG_Q\hat D\,V_{ci}\ ;$$

the first expression is used for a direct feedback, while the second for an I/Q feedback, where D is a signal transport delay operator, G, G_I and G_Q the gains.

Without any feedback loop, the 'natural' stability margins are insufficient to cope with injection errors of 5° in phase and 0.1 % in energy (Fig. 4). Instabilities grow exponentially 600 µs after injection.

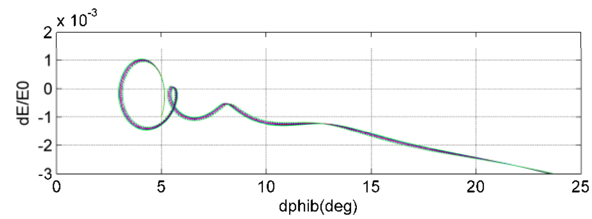

Figure 4: Disturbed beam without feedback

To maintain the beam stability, a direct RF feedback loop is simulated with a gain of 10 and delay of 1 µs. The initial perturbation is damped within 6 ms, and the stability is insured even in the presence of 'real' microphonic disturbances (~ 200 Hz pk-pk detuning) as they are measured in one cavity. The beam behaviour in the energy-phase diagram is shown in Fig. 5. In the steady state, where the only disturbance comes from the microphonics, a residual error of 0.08 % in accelerating voltage and 0.6° pk-pk in phase is observed.

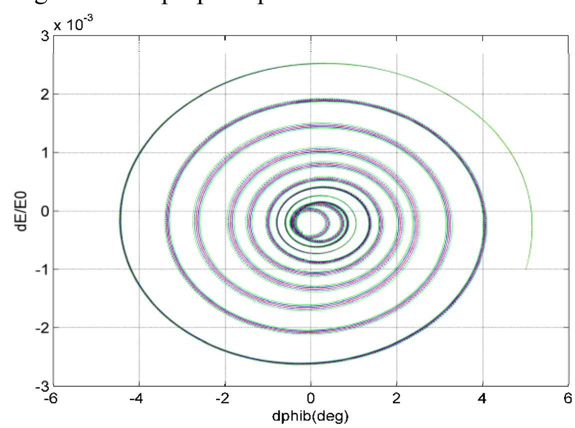

Figure 5: Disturbance damping with a direct feedback

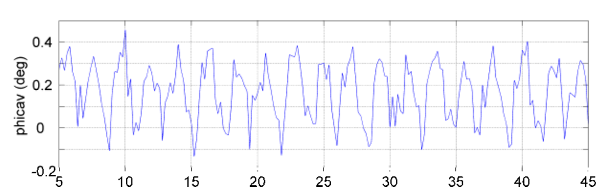

Figure 6: Residual cavity phase error in steady state

Similar results are obtained with an I/Q feedback loop with both gains equal to 10. The extra-power needed by the LLRF in this simulation is only 6 kW to cope with the microphonic disturbances. In a further step, the feedback gains will be optimized accounting for the feedback loop delay, power budget limitation and the amplitude of the disturbances in order to reduce the residual errors and the damping time.

SOLEIL PHASE-2 DIGITAL LLRF

For the digital LLRF system, an architecture based on a FPGA, with ADC's, DAC's, analogue IQ modulator and IF frequency conversion has been chosen (Fig. 7).

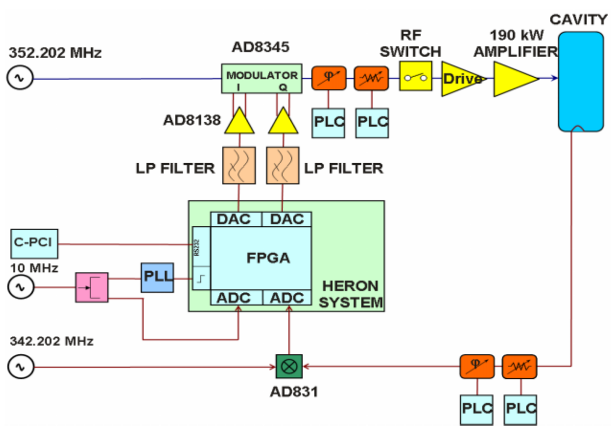

Figure 7: Block diagram of the digital LLRF

The HERON IO2 module has been selected for the digital signal processing because of the short latency between the input interface (ADC) and output interface (DAC) through the Xilinx Virtex II FPGA. The architecture of this commercial board, which can operate in a stand-alone mode, is sketched in Fig. 8.

In order to study the behavior of the program with time constraints, ISE (Integrated Software Environment) and ModelSim tools are used to simulate the applications. The loading of the FPGA boot program into the PROM is fast and easy.

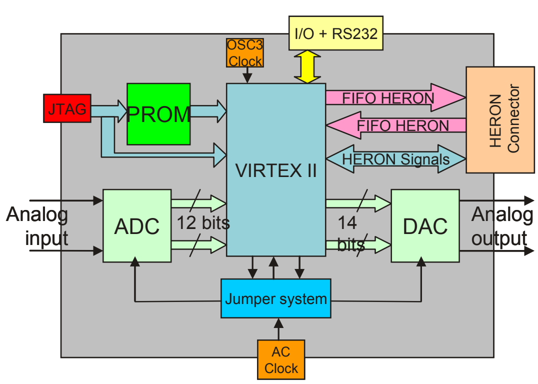

Figure 8: IO2V2 HERON module architecture

For a LLRF application, the building blocs in the FPGA are composed of a digital IQ demodulator, some FIR filters, and clock and data managers, which are detailed in Figure 9.

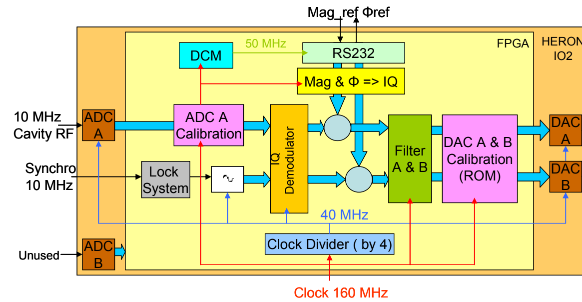

Figure 9: Digital LLRF building blocks

Most of these building blocks have been already implemented and experimentally validated. As an example, the latency of a 34 taps FIR filter implemented on the Heron board is less than 750 ns. For the signal processing, the 352 MHz RF signal is downconverted to a 10 MHz IF signal. The digital IQ demodulator works with this IF signal as an input and a look-up-table (LUT) generates a reference bit-stream synchronized with the machine 10 MHz master oscillator. The Heron board provides a basic RS232 interface with the FPGA, which makes debugging and calibration rather easy. The digital PID controller will be implemented similarly to the FIR filters. As DAC's and ADC's have coding errors, a correction table is stored in the ROMs, created inside the FPGA.

LLRF STATUS AND SCHEDULE

In the commissioning phase of the SOLEIL SR, the analogue LLRF, composed of the amplitude, phase and frequency feedback loops has provided expected performances at low beam current. The fast direct RF feedback loop needed at the nominal 500 mA beam current is ready for commissioning.

The design of the new digital LLRF system is now finalised. All the analogue and digital components have been individually validated and they are being assembled for testing the functionality of the complete system.

Meanwhile, a deeper analysis of the disturbances on the SOLEIL cavities should provide an accurate modelling and simulation of the LLRF system performance. For instance, it is important to make sure that the operation of the frequency tuning loop with a stepping motor will not excite significantly any mechanical resonance of the cavity.

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