

ALL DIGITAL IQ SERVO-SYSTEM FOR CERN LINACS

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Abstract

A VME based control system has been developed and built at CERN for the servo loops regulating the field in linac accelerating structures. It is an all-digital system built on a single VME card, providing digital detection, processing, and modulation. It is foreseen to be used, in different versions, for the needs of both present and future CERN hadron linacs. The first application will be in the energy ramping RF chain of the CERN Heavy Ion Linac (linac 3). Design principle and the experimental results are described.

INTRODUCTION

The CERN Linac RF Servo Control (LRFSC) card (formerly known as the LLCC card) is an all digital accelerator cavity control system built on a single VME standard card [1]. It has three RF inputs and one RF output. All signal processing on the card is done on a single FPGA (Xilinx XC2V2000) which also controls the diagnostic outputs and houses the VME interface. The use of an all digital system provides great flexibility in the testing and modification of the control algorithms as well as other features such as variable set-points and feed-forward. Figure 1 shows an easy to use graphical user interface that has been developed in Java for the LRFSC. It provides for the quick modification of the control filter constants and calibration parameters as well as the loading of external set-point and feed-forward files. It also shows numerous signal level readouts at different locations in the process and allows the user to choose which of these will be sent to the four diagnostic DACs.

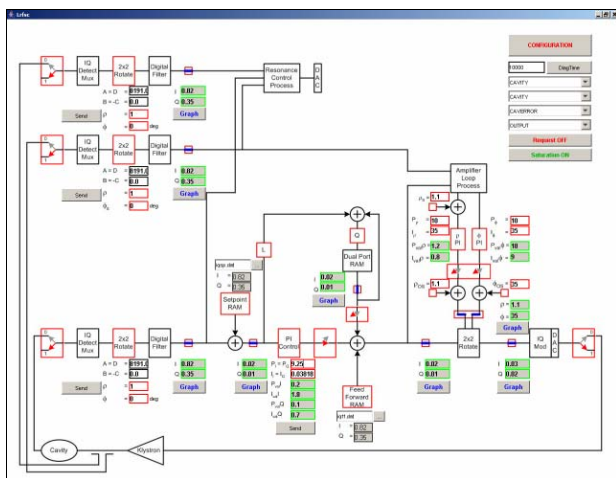


Figure 1: LRFSC control screen.

The LRFSC card has undergone a series of functional tests using a 400 W pulsed power amplifier and a copper test cavity with a 202.56 MHz centre frequency and a

bandwidth of 44.3 kHz ($Q=4450$). The frequency response in both pulsed and CW mode has been measured and an anti-windup algorithm for the integrator has been implemented and tested. This paper will describe the set-up and show the experimental results for these tests.

CW MEASUREMENTS

Since the LRFSC will be used in a pulsed system with a heavily beam loaded cavity its frequency response is of primary interest. Figure 2 shows the traditional diagram for evaluating the transfer function of the controller-cavity system.

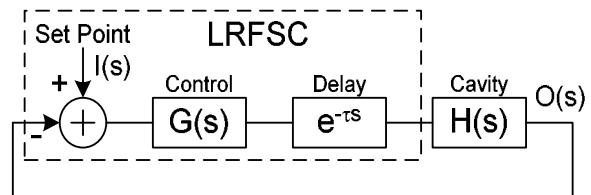


Figure 2: Simplified controller-cavity system.

The transfer function,

$$T(S) = \frac{O(s)}{I(s)} = \frac{G(s)H(s)e^{-\tau s}}{1 + G(s)H(s)e^{-\tau s}}, \quad (1)$$

has the best response when the cavity pole is cancelled by the zero of the “Proportional/Integrator” (PI) controller which occurs when $K_i = K_p \cdot \omega_c$, where K_i and K_p are the integrator and proportional gain constants respectively and ω_c is the half bandwidth of the cavity.

For the needs of RF measurements, the card was modified to operate in continuous mode (CW). A network analyzer was used to measure the frequency response of the controller-cavity system. Figure 3 shows the experimental setup used for this measurement.

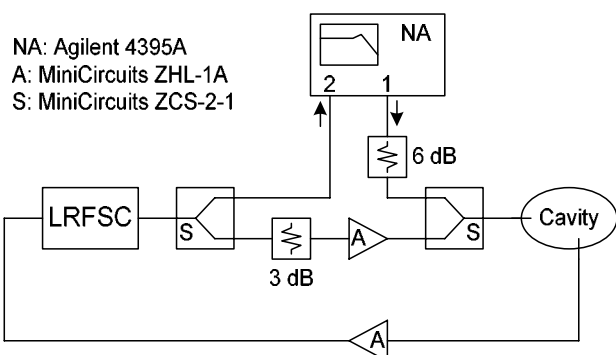


Figure 3: Experimental setup for CW frequency response.

The transfer function between the excitation port, 1, and the receiver port, 2, (S_{21}) is identical to that of Equation (1). The isolation of the splitters is 25 dB and

the amplifiers have minimal delay and a directivity of 15 dB.

Figure 4 shows the magnitude response of the controller-cavity system in closed-loop for several values of K_p (with $K_i = K_p \cdot \omega_c$), with the network analyzer excitation 26 dB below the steady state value imposed by the controller. With the cavity on resonance, the measured transfer function response is symmetric around the operating RF frequency (202.56 MHz). Table 1 shows the relevant data for each trace.

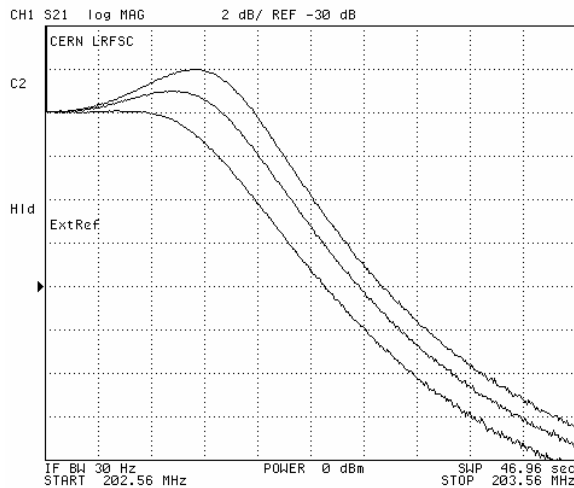


Figure 4: Closed-loop magnitude response of the LRFSC controller-cavity system.

Table 1: Data for magnitude response traces.

Trace	K_p	K_i	f_{-3dB} (kHz)	f_{0dB} (kHz)
1 (top)	10.25	.0353	472	390
2 (middle)	9.25	.0318	425	322
3 (bottom)	8.0	.0275	359	200

The open-loop frequency response of the LRFSC card was also measured but with the integrator disabled ($K_i = 0$). It has a -3 dB bandwidth of 7.5 MHz with $K_p = 10$. From the open-loop phase, the delay τ , of the LRFSC was measured to be 540 ns. This is higher than the 408 ns reported in Reference [1] because the processing in the FPGA now includes a matrix rotation for phase and gain calibration, the PI controller, and feed-forward.

STEP RESPONSE RESULTS

Figure 5 shows the small signal step response of the controller-cavity system. The step shown was caused by changing the I set-point from 40% to 44% of full power after steady state had been reached. The K_p and K_i values used were those of the middle trace in Figure 4. The 10% to 90% rise time is measured to be 1 μ s.

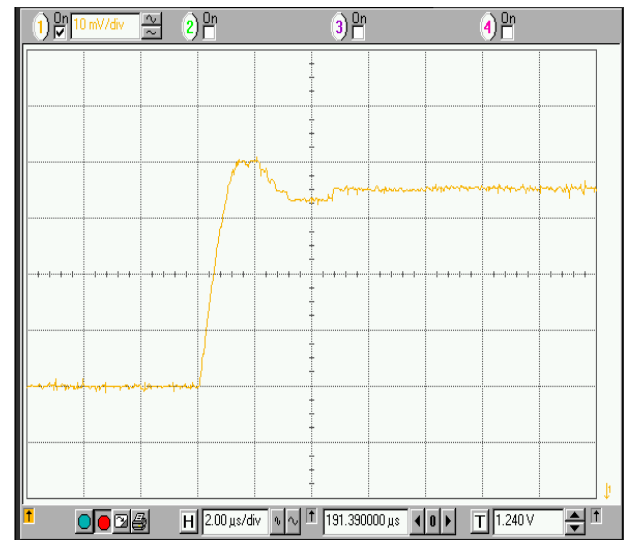


Figure 5: Small signal step response of LRFSC cavity-controller system.

ANTI-WINDUP MECHANISM

The first version of the PI controller allowed the 27-bit digital integrator to continue integrating beyond the 14-bit positive or negative limits of the output. This resulted in no extra information sent to the output during the initial overshoot, since it was already completely saturated. However, since the value of the integrator was becoming very large, the recovery of the output inside its 14 bit range was significantly delayed. Therefore an anti-windup mechanism has been designed that selectively disables the integrator when the integral product goes above 8191 or below -8192. In the first case, the integrator starts ignoring any positive errors fed to it, while in the second case it ignores negative numbers and only starts accumulating again when a positive error is received.

Figure 6 shows the improvement brought by the anti-windup mechanism with gains set to better illustrate the phenomena. The figure depicts the cavity signal step response from 0 to 40% of full power with anti-windup enabled (lower curve) and anti-windup disabled (upper curve). The rise-time is roughly 10 μ s in both cases, but the settling time is reduced by approximately 90 μ s with the anti-windup scheme.

Figure 7 shows the output signal sent to the cavity as computed by the PI controller, again for a step input. At the beginning, and for some 15 μ s, the output is saturated because the error is very large. After a while the error changes sign and the proportional branch of the controller reacts immediately, resulting in the negative drop. From then on the integrator with anti-windup starts to work and gives meaningful changes to the output (lower curve), while the integrator without the anti-windup system is still “discharging” and giving no meaningful contribution. The discharging takes some 90 μ s, after which we see a negative drop and the integrator goes back to normal operation.

REFERENCES

- [1] A. Rohlev, J. Serrano, and R. Garoby, 'All Digital IQ Servo-System for CERN Linacs', PAC'03, 2003

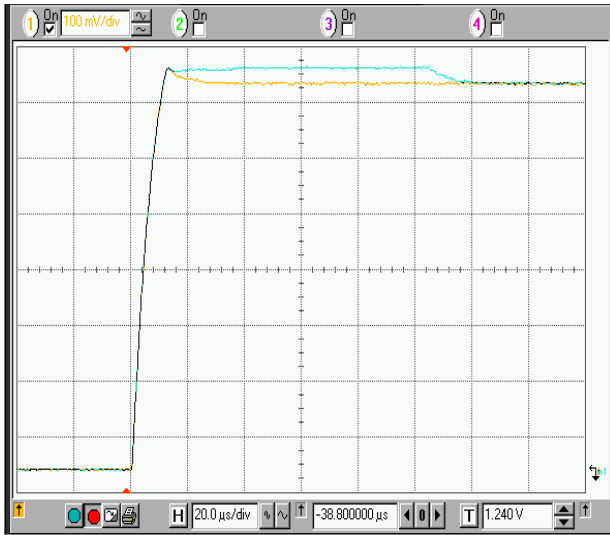


Figure 6: Step response of cavity signal with (bottom) and without (top) integrator anti-windup.



Figure 7: Step response of output signal with (bottom) and without (top) integrator anti-windup.

CONCLUSION

The frequency response of the LRFSC card has been measured in both CW and pulsed mode when driving a cavity with a centre frequency of 202.56 MHz and a bandwidth of 44.3 kHz. A closed-loop -3 dB frequency of twice 359 kHz was measured with a maximally flat response, and a -3 dB frequency of 425 kHz was reached with a 1 dB overshoot. An anti-windup mechanism has been added to the integrator and a highly functional graphical user interface has been developed in Java. The LRFSC card will be used in the energy ramping RF chain of the CERN Heavy Ion Linac (linac 3).