DESIGN AND INTEGRATION OF A LOW COST NODE FOR A DISTRIBUTED DAQ/CONTROL SYSTEM

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Abstract

Many fieldbus protocols exist for control and networking purposes in medium and large scale facilities. Among these protocols, WorldFIP initially developed for the rail transport and reactor plant applications, appears as a new European standard which presents many attractive features in different aspects. This paper presents on the one hand, the design of a DAQ/Control node based on Alstom FipWare and an Analog Device Microconverter® associated with other digital and analog I/O extensions, and on the other hand, the integration issues related to system and user level programming with a possible connection to a LabView based control system. The final product has been successfully tested as an interface for the low level RF driver of the CRYHOLAB facility dedicated to the superconducting cavities and devices R&D.

1 INTRODUCTION

Remote control of an accelerator facility or in a lesser extent, a specific test bench based on smart equipments, including actuators and sensors, involves the choice of a fieldbus protocol. Among the profusion of protocols, opened or proprietary, two candidates turn out to be particularly interesting : CAN and WORLDFIP fieldbus, for their transmission rate, versatility and openness. While the CAN bus has become a widespread industrial standard with many chip vendors and product offers, WORLDFIP still appears as an emerging European standard offering however a longer transmission distance at a higher rate (up to 3 km @ 2.5Mbit/s), a higher connectivity (256 nodes instead of 127), and above all a deterministic operation which is essential for real-time applications.

For small scale applications, WORLDFIP protocol offers low cost implementation solutions using MICROFIP [1] chips. The paper presents such a solution in the case of a phase locked RF system for a superconducting cavity test bench (CRYHOLAB). Any part of a facility or experimental area can be managed as a node in a WORLDFIP network.

2 HARDWARE ARCHITECTURE

The WORLDFIP components consist mainly in three chips : MICROFIP, FIELDRIVE and FIELDTR supplied by ALSTOM on a CC131 board. For prototyping, this later is used as a daughter board connected to a 3U board supporting an Analog Device ADuC812 Microconverter® [2] and different peripheral extensions (DAC, logic I/O expanders, VCO, timers, RS232 transceiver and RAMs). The Intel 8051 core integrated in ADuC812 operates MICROFIP in the microcontrolled mode. A synoptic of the hardware arrangement is given in Figure 1.

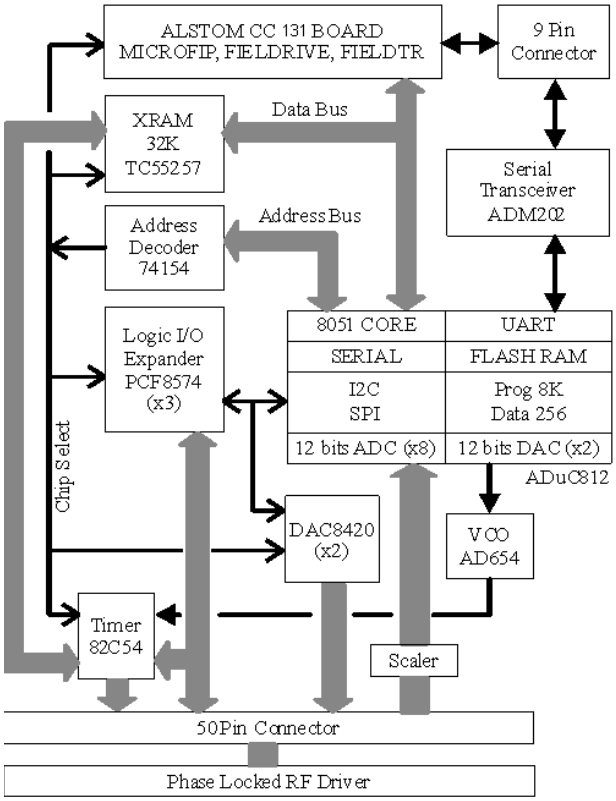

Figure 1 : Synoptic of a microcontrolled WORLDFIP node using a low cost MICROFIP chip.

Figure 2 : Physical view of the WorldFIP node showing the ALSTOM's CC131 module.

The choice of ADuC812 is motivated by its high level of integration. The 8 kBytes of program flash RAM associated with an UART interface allow in site

programming which makes developing and debugging much easier. The integration of I_2C and SPI interface offers a capability to manage multiple peripheral expansion (PCF8574, DAC8420, Timer 82C54). The subroutines required for their operation can be easily written in C language and compiled using for example Keil® development tools. Finally, the high accuracy on chip 8 multiplexed channels ADC are used efficiently to acquire ±10 V signals through a scaling network.

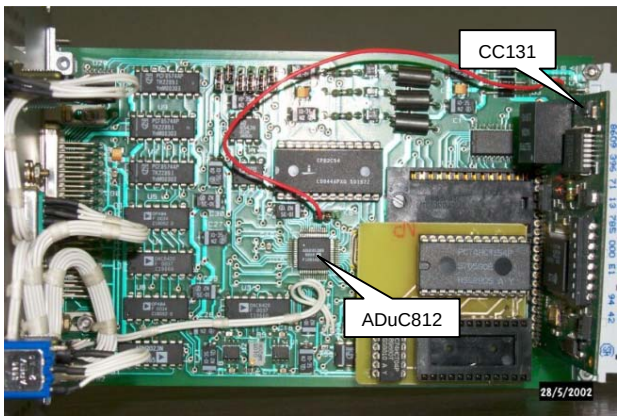

Figure 3 : View of the electronic board with ADuC812 and the peripheral devices.

As a summary, the WORLDFIP node I/Os include 8 analog inputs, 8 digital outputs, 8 logic inputs, 8 logic outputs, and 3 signal timers/oscillators. In the RF driver application, the ADC reads the phase error and the RF powers, the DAC controls the limiting amplifiers, phase shifter and frequency tune, the logic outputs drive the different RF switches while the logic inputs are dedicated to the status read back. One output of the timer modulates the RF power by means of a PIN diode.

3 SOFTWARE ARCHITECTURE

Two kinds of software were developed to control the RF driver :

- An embedded program which is loaded in the internal program memory of the ADuC812 ;
- A Human-Machine Interface to provide access to the equipment.

3.1 The embedded program

The embedded program is a real time one which ensures the FIP dialogue and controls the peripheral equipments (ADC, DACs, I/Os, timer) on each request of the WorldFIP bus arbitrator (ID_DAT). It was written in C language using the KEIL C51® environment.

The equipment produces 4 variables :

- Presence (8 bytes)
- Identification (8 bytes)
- Infos (8 bytes),
- Acquisition (40 bytes),

and consumes 2 variables :

- Timers control (8 bytes).
- Logic and DAC control (40 bytes),

The variable for timers control is structured as follows :

0	1	2	3	4	5	6	7
N	**MODE**	**RATE**		**WIDTH**		**N.U.**	**N.U.**

Where N is the timer's number (1 to 3),
MODE allows the selection between
Continuous '0' (0)
Continuous '1' (1)
Pulse (2)
RATE is the repetition rate of the pulse,
WIDTH is the duration of the pulse.

The variables for outputs control and acquisition are built on the same schedule :
Byte 0 : I/O direction
Byte 1 : I/O1 value
Byte 2 : I/O2 value
Byte 3 : I/O3 value
followed by 8 analog values (floats).

The program is based upon a modified version of ALSTOM's MICROFIP Handler® [3]. A hardware interrupt is raised on each request (ID_DAT) of the Bus Arbitrator. Upon receipt of a consumed variable, the program treats the information and controls either the timers or the analog or digital outputs. It then produces its own variables after acquisition of the inputs.

The total size of the program is 4876 bytes in CODE memory and 431 bytes in XDATA memory (196 overlayable).

3.2 The Human-Machine Interface

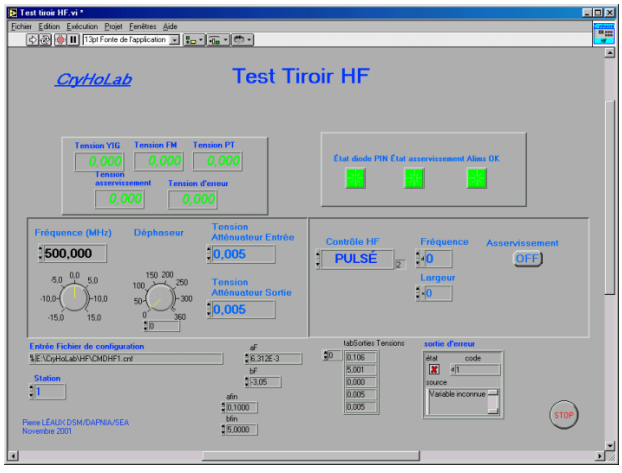

Figure 4. The Human-Machine Interface for testing the RF driver.

A Human-Machine Interface for the test of the RF driver was developed under LabView®. It allows the control of the oscillator's frequency and phase, the input and output attenuation and the operation mode (continuous or pulsed). It also periodically (100 ms) reads 5 voltage values and 3 digital inputs (status of the driver). The FIP communication is ensured via the WorldFIP DLLs developed by HLP Technologies [4], encapsulated in LabView VIs. A second set of VIs translates the controls on the interface into WorldFIP parameters.

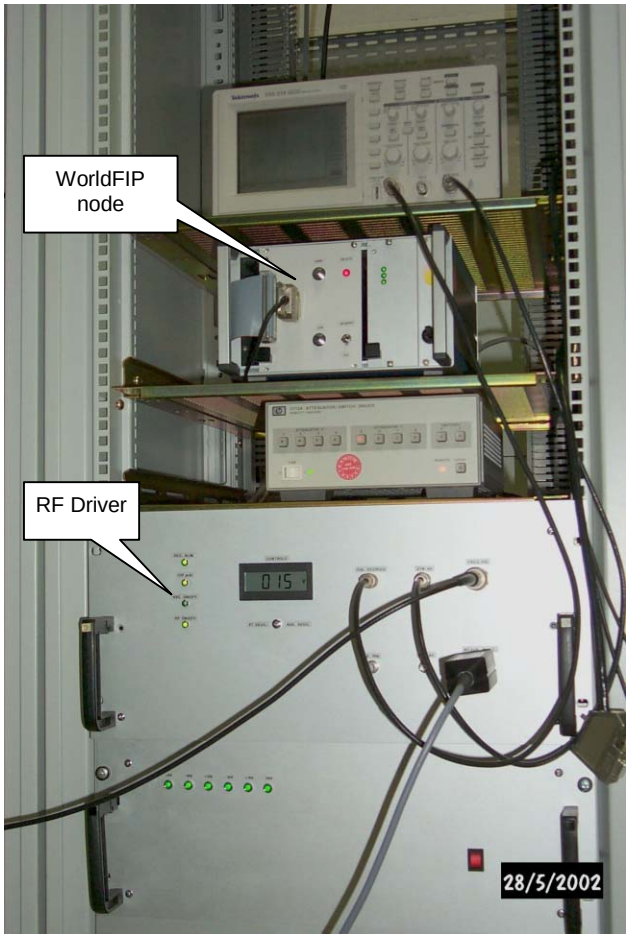

Figure 5 : Global view of the RF driver enclosure on the CRYHOLAB site.

4 CONCLUSION

The use of low-cost fieldbus components associated with intelligent data acquisition chips (ADuC812) opens a way to remote real time control for many devices in the accelerator domain. The development time was about one year, including learning of C51 and MicroFIP Handler, and writing of subroutines. After this step, the development of the HMI is very fast and straightforward using Labview.

All the components could easily be integrated on a single 3U board which can be plugged into the RF driver crate in order to obtain a system which can be directly connected on the WorldFIP network. The cost of such a WorldFIP node can be expected less than 1000 euros.

5 REFERENCES

[1] MicroFIP User Reference Manual ALS 50280 b-en ALSTOM 10-99.

[2] ADUC812 MicroConverter™, Multichannel 12-Bit ADC with Embedded FLASH MCU, Analog Devices, 1999

[3] MicroFIP Handler Software Release 1 User Reference Manual ALS 50202 d-en ALSTOM 04-2000.

[4] WorldFIP Tools, Solutions for WorldFIP HLP Technologies 07-2000. http://www.hlp.fr/