ARCHITECTURE OF LONGITUDINAL FEEDBACK SOFTWARE SYSTEM IN TLS

C. H. Kuo, W. K. Lau, M. S. Yeh, C. J. Wang, K. H. Hu, K. T. Hsu Synchrotron Radiation Research Center

No. 1 R&D Road VI, Hsinchu Science-Based Industrial Park, Hsinchu 30077, Taiwan, R.O.C.

Abstract

The longitudinal multi-bunch feedback system using new DSPs structure is being developed in TLS. Many elements of the system are remotely programmed in various operation modes to be applied in diagnostic and feedback request. The components of feedback system are consists of feedback control rules and data acquisition in DSPs, system resources management at VME host, signal analysis and simulation in console. The integrated software environments and developments status will be presented in this report.

1 INTRODUCTION

The storage ring of SRRC is a 3rd generation synchrotron light source, designed to store the beam current 200 mA at 1.5 GeV. Stable longitudinal dynamics are the most important performance issues of the storage ring. Longitudinal instabilities are prominent when the machine not optimize its operating conditions. However, to maintain optimized condition is not an easy job. Source of the longitudinal instabilities is mainly due to high order mode (HOM) of the RF cavities. Active longitudinal feedback system (LFB) was proposed to fight the instabilities. The system is in commissioning now.

The DSP technology are advanced drastically since fist bunch-by-bunch feedback system deploy by PEP-II/DA Φ NE/ALS collaboration, number of DSPs can be reduced drastically for the newly design. Experiences accumulated from these laboratories made us design a new system easily than before. A new implementation was adopted for the SRRC.

Longitudinal feedback system was planed to combat with the longitudinal instabilities [4,5]. The project to replace two existing DORIS cavities by a single cell Cornell superconductivity RF (SRF) cavity at the storage ring is underway that is a long-term solution. Nearly HOM free properties are promising of SRF cavity. This project is also accompanied with 500 mA upgrade goals. However, longitudinal feedback system is used to damp residues longitudinal instabilities are still necessary. Powerful diagnostics of LFS are still useful to study the beam properties under conventional RF as well as SRF environments.

2 SOFTWARE ENVIRONMENT

2.1 Development system



Figure 1: Software system block.

The software structure of longitudinal multi-bunch feedback system (LFB) consists of a digital signal processor array to execute feedback algorithm and to provide raw data for diagnostic purposes. In such environment, major software components includes, (1) feedback control algorithm on DSP, (2) DSP developing environment is on PC, (3) diagnostics toolkits is on PC and VME host, (4) user interface on PC and workstation. The system block is shown in figure 1. The feedback control loop combine functions including data input/output, filtering and housekeeping. DSP developing environment consists code composer running on PC via remote Ethernet based JTAG interface to debug program. The system equips diagnostic toolkits to acquire and analyse data. The associated hardware and software are commercial products that may help to reduce the system development time. The data transportation is by the 'C40 compatible communication ports. There are eight input ports and eight output ports in this system. Major module on LFB VME crates is consists of VME hosts, DSP modules and JTAG emulator.

This development system is an Ethernet based JTAG emulator. It is able to remote control by local computer with window user interface in windows95/NT operation system. It supports to multi-processor download and develops DSP program in the same time. The code composer is a system development tool that supports an integrated development environment (IDE) for 'C6x. This environment allows DSP code designer to edit, build, manage products, debug and profile from a single application. In addition, the IDE lets user compile in the background as well as analyse signals graphically (including Eye Diagnostic, Constellation diagnostic, FFT Waterfall, Image display etc.), perform file I/O, debug multiprocessors, and customise a C-interpretative scripting language in the IDE.



Figure 2: Schematic diagram of development system.

The debugger and development of VME host is to provide a simple, interrupt driven, inter-device communication protocol for distributed Digital Signal Processing applications. The protocol is based on highlevel geographic addressing, in which each device is referred to by a user assigned name rather than as a range of addresses. The hardware involved in these distributed applications may utilise various interconnect schemes, such as shared memory on the VME bus, Ethernet, etc. The debug tool provides a variety of capabilities. First, starting, stopping or resetting the DSP. Second, loading code or data into DSP, examining the registers or memory of DSP. Third, hardware instruction or datadependent breakpoints. Fourth, a variety of counting capabilities including cycle-accurate profiling. Last, realtime data exchange (RTDX) between the host and the DSP. The schematic diagram of system is shown in Figure 2.

2.2 Data I/O in Software control

All tasks of feedback software are optimal for communication and filtering. This task can't be swapped when processor is accessing from COMM port memory. The phase shift, and band-pass filter tasks are embedded in DSP module. In the meantime, it receive filter control and feedback status control from host. The DSP modules include of multiprocessors to process input data, to kick system. To keep from COMM port communication with MUX and DEMUX module in the same time. There is a synchronised signal between MUX module and DSP that is separated to input and output (I/O) COMM port communication timing. The feedback procedures are housekeeping, idle and wait next working period after data I/O and signal filtering. This synchronised signal is defined to MUX module data preparation and COMM port communication status. The DSP data I/O hardware structure is shown in figure 3.



Figure 3: DSP hardware I/O port.

2.3 Housekeeping

The housekeeping in DSP is to receive command from VME host to control filter coefficients update and various operation modes. There are three modes in the system for diagnostic request. First mode is normal mode, second mode is pre-trigger mode and the last mode is post-trigger mode. The normal mode is a default mode that is to confirm system reliable. The DSP dual port memory is always refreshed. The pre-trigger and post-trigger modes are to record some transient effects in longitudinal phase error. These control task are embedded in VME host, are connected with console computer to support to feedback remote control, filter coefficient update, status reports and data analysis. The relationship tasks are shown in Figure 4. The setting service handles filtering and status control. General reading handles raw data store.

2.4 Host tasks distributions

There are many tasks in host that is necessary managed. For example, diagnostic request includes of setting service and DDB upload. The dynamic database handles all I/O data control and server. The task of setting service receives command from console. The global data spool includes of DSP dual port and global memory. The raw data is saved in the dual port memory. The filter coefficients, operation mode and control on/off statuses are saved in global memory. The general reading program is to access global data spool that includes of global memory and dual port memory in DSP, and then sends to DDB. Upload task access data from DDB when receive network event. These tasks priority aren't same. For example, feedback is necessary to be stopped when host is updating filter coefficient and then turn on feedback again. Status control task has lower priority than filter control.



Figure 4: Host tasks distribution block.

2.5 COTS software

The VME host supports feedback loop control, filter update, data acquisition. It consists of a microprocessor of PowerPC 604e, 32 megabytes on-board memory, RS-232, PMC sites and Ethernet ports. Although data exchange interface can be established by DSP debugger and development environment, feedback will be stopped when data is transferring, it is not a good solution. Dual port memory on DSP boards is a best candidate for data exchange to satisfy analysis and access request. There are several tools in console except for development tool, such as, filter simulation and raw data on line display. An integrated MATLAB simulation tool and LABVIEW are supported in console to satisfy various conditions in commissioning, to adjust phase and centre frequency of band pass filter on online.

There is 256 KB dual port memory on each DSP site. Every DSP is in charge of 25 bunches, the longest record length of sampled data is 10 KB per bunch. The record program can be commanded to change feedback loop parameters during record scenario. For growth and damp experiment, it is necessary to turn off and on the feedback loop sequentially. After the end of record cycle, dual port memory will release by DSPs, VME host can access transient data without effect the operation of DSP. The diagnostic data is saved on this area on demand. The VME host is transparent to DSP boards and doesn't influence feedback loop of LFB.

Acquired data by the data acquisition mechanism are stored in disk. The console computer retrieve these data file via network file system (NFS). Various MATLAB script files are developed for data analyses in on-line or off-line manner. These analysis include unstable eigenmodes identification, growth/damping rates, beam pseudo-spectrum, bunch-by-bunch current monitor, synchrotron tune vs. bunch number – gap transients, tune spread, Landau damping, Longitudinal impedance vs. frequency from bunch synchronous phases, eigenstructures of uneven fills, phase space tracking. Transverse motion is also possible by alias sampling by LFB system and record that is very helpful to investigate transverse dynamics.

3 SUMMARY

The longitudinal instabilities at the storage ring of SRRC are a tricky question. Various measures were adopted to mitigate the effect of instabilities. The operational experience from six LFB installation which is the fruitful results of SLAC/DA Φ NE/ALS collaboration [1] reveal that LFB system is an effective tool to fight longitudinal instabilities. The schedule of LFB system in SRRC is slightly delay for various reasons. Most of the difficulties were solved recently. Commissioning is in progress now. The system is expected very helpful to cure longitudinal instabilities at the storage ring of SRRC. Even after HOM free superconductivity RF cavity installs, the LFB system is still useful to damp residual longitudinal instabilities. Powerful of transient domain diagnostic are very useful to investigate various instabilities issues in pre and post SRF era. Adopt alias sampling techniques made the LFB system possible as a tools for the transient domain transverse instabilities observation, it is promising for the studies of transverse instabilities and ion effect.

REFERENCES

- [1] J. D. Fox, "Programmable DSP-Based multi-bunch feedback - Operational Experience from Six Installations", these proceedings.
- [2] S. Prabhakar, J. D. Fox, D. Teytelman, and SA. Young, "Phase space tracking of coupled-bunch instabilities", Phy. Rev. Special Topics – Accel. and Beams, PRST-AB 2, 084401 (1999) and reference therin.
- [3] M. Tobiyama, and E. Kikutani, "Development of a high-speed digital signal process system for bunchby-bunch feedback systems", Phy. Rev. Special Topics – Accel. and Beams, PRST-AB 3, 012801 (2000) and reference therin.
- [4] W. K. Lau, S. J. Lin, M. S. Yeh, L. H. Chang, T. T. Yang, K. T. Hsu, M. H. Wang, C. C. Kuo: Development Of A Digital Longitudinal Damper For The TLS Storage Ring, Proceedings of 1997 IEEE Particle Accelerator Conference, Vancouver, 1997.
- [5] W. K. Lau, L. H. Chang, K. T. Hsu, C. H. Kuo, J. A. Li, M. S. J. Lin, T. T. Yang. M. S. Yeh: Progress of the TLS Longitudinal Feedback System and Associated Beam Longitudinal-Dynamics Studies, Proceedings of 1999 IEEE Particle Accelerator Conference, New York, 1999.