BEAM POSITION AND PHASE MEASUREMENTS USING A FPGA FOR THE PROCESSING OF THE PICK-UPS SIGNALS

G. Naylor, E. Plouviez, G. F. Penacoba
European Synchrotron Radiation Facility (ESRF), Grenoble, France

Abstract

We have implemented the signal processing needed to derive the transverse beam position and the beam phase from the signals of a four electrode BPM block on a FPGA (field programmable gate array). The high processing rate of a FPGA allows taking the full benefit of the high data acquisition rate of the more recent ADC. In addition, it is possible to implement on a FPGA a processing algorithm exactly tailored to the measurement of the beam parameters. The efficiency of the signal processing has also been improved by a careful choice of the frequencies of the sampling clock and of the RF front-end local oscillator, which are derived from the storage ring RF frequency. This paper describes the BPM, the RF front-end electronics and the FPGA algorithm. It presents some of the applications of this BPM at the ESRF and gives measurement results.

INTRODUCTION

ADC with resolution and sampling rate adequate for the acquisition of storage ring beam signals have been available for several years. The sampling rate of these ADCs is in the 20Msps to 100Msps. Such a high data rate cannot be efficiently processed by a regular DSP. A solution to this problem is to pre process the data in order to decimate the data flow using a specialized circuit called a Digital Down Converter (DDC)[1]. This solution gives good results but does not take full advantage of the periodicity of a beam signal. Therefore, a FPGA was used with a processing algorithm tailored to the time structure of our SR beam. The main features of this processing are:

Synchronous I/Q demodulation

Computation of the amplitude and phase modulation

The useful frequency range of the BPM pick-up signals usually starts well above the maximum frequency that an ADC can handle. In our case we selected a 10 MHz bandwidth around 352.2 MHz in the pick-up signals, and the maximum input frequency of the ADC that we use (AD9225) is only 100 MHz. So a RF front-end circuit must be implemented to down convert the frequency of the pick up signals in the input frequency range of the ADC. The efficiency of the digital signal processing will depend on the wise choice of the frequency shift applied to the pick-up signals. In our case, we wanted to be able to measure the bunches position and phase in case of so-called time structure mode filling of the storage ring: The ring is then filled with 1 or 16 high intensity bunches equally spaced. So we needed a sampling frequency equal to one quarter of the bunch spacing in the 16 bunch filling mode.

RF FREQUENCY DOWN CONVERTION

General Layout

The layout of the RF front-end is shown in figure 1.

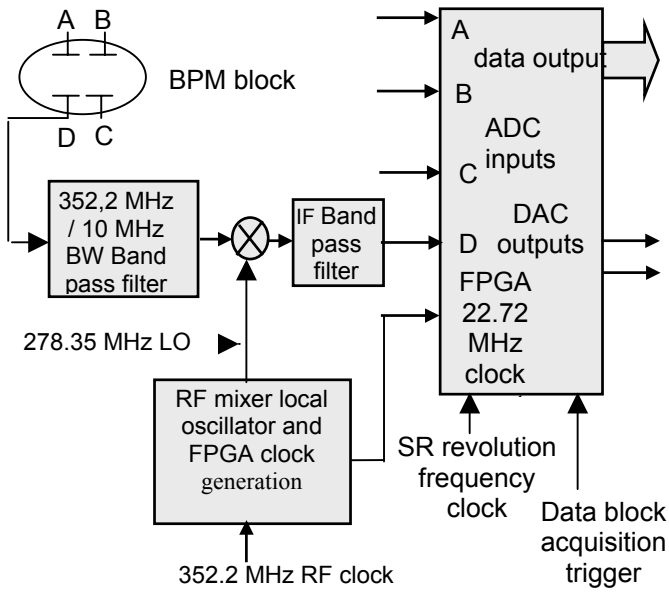

Figure 1: Layout of the BPM

The ESRF RF frequency is 352.2 MHz, the ring harmonic number is 992=32*31 and the revolution frequency is f_{rev}=355KHz. The choice of the clock and local oscillator frequency has been done following this line

ADC sampling clock frequency

The maximum sampling frequency of the 12-bit ADC AD9225 is 40MHz (definitely not the ultimate fast ADC available today…). The T delay between 2 bunches with a 16 bunch filling pattern of our storage ring is 88.018 ns; 1/T= 352.2MHz/ 62= 5.68 MHz. We have chosen 22.72 MHz for the ADC sampling clock frequency f_s, 2X 352.2 MHz / 31. Using such a clock, a synchronous in phase and in quadrature acquisition (I/Q) of all the harmonics of f_{rev} up to 11.36 MHz can be performed

Local oscillator frequency

The intermediate frequency IF can be higher than $f_s/2$ providing the IF signal bandwidth is lower than $f_s/2$

(under sampling); but the intermediate frequency IF must be such that the phase of the IF signal shifts by $\pi/4$ over one period of the f_s signal n order to produce an I/Q detection. We have chosen IF=13*fs/4 ie IF=73.848MHz; therefore the local oscillator frequency f_{LO} is $f_{RF}=f_{IF}$ =278.352 MHz. These frequencies have been synthesized using oscillators synchronized by PLLs on the right harmonics of f_{rev}.

Selectivity of the RF and IF filters

The digital filtering of the ADC data will give correct results on condition that the image frequency signals in the RF spectrum and in the IF spectrum have been removed by analog filters. In the case of a beam signal, with a periodic spectrum of N X f_{rev} lines with symmetrical sidebands created by the transverse and longitudinal oscillations, this aliasing is not harmful provided the sampling is synchronous with the beam revolution. So the requirement for the RF and IF band pass selectivity is much less stringent than with a non-synchronous scheme for the RF frequency down conversion and ADC sampling.

DIGITAL SIGNAL PROCESSING

FPGA compact PCI board

A compact PCI general-purpose mother board has been developed at the ESRF in the Digital Electronics Group, to offer a quick answer to internal developments requiring fast and reasonably complex processing with a flexible I/O interface. Application specific mezzanines are added to this board. The FPGA circuit used on this board is a *Xilinx VIRTEX 600E*.

ADC/DAC mezzanine

The input signals of the board are converted at a rate of 22.72 MHz by four AD9225 12 bits AD converters housed on a mezzanine. This mezzanine is also used to input the sampling clock signal as well as other synchronisation signals (storage ring revolution frequency and injection timing). In addition two 12 bits DAC have been implemented on the mezzanine to output the results of the processing.

ALGORITHM PROGRAMMING ENVIRONMENT

The VHDL language used for the programming of the *Xilinx* FPGA cannot be really mastered by occasional users. However, high-level programming tools are available to write down and test signal-processing algorithms, which can be compiled in VHDL afterwards. We have used such a tool: *System Generator*, available from *Xilinx*. *System Generator* compiles in VHDL a processing model described by a *Simulink* block diagram [2]. So the only VHDL programming needed then is the allocation of the input /output resources.

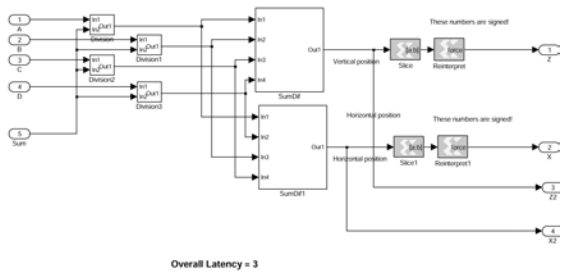

Figure 2: Part of the graphical *Simulink* algorithm layout

PROCESSING ALGORITHM

Beam position

The FPGA uses the A_n, B_n, C_n, D_n and A_{n+1}, B_{n+1}, C_{n+1}, D_{n+1} IF signals coming from the 4 pick-ups of the BPM and sampled by the four ADCs over to successive clock periods; it computes the following values:

- $A=(A_n^2+ A_{n+1}^2)^{1/2}$, B, C and D
- Σ=A+B+C+D
- Δz= ((A+B)-(C+D)) / Σ vertical position signal
- Δx=((A+D)-(B+C)) / Σ horizontal position signal

It averages Σ, Δx, Δz, over one revolution period to generate a turn-by-turn position measurement.
It calculates the beam position:

$$x = f_x(\Delta x, \Delta z) \text{ and } z = f_z(\Delta x, \Delta z)$$

$f_x(\Delta x,\Delta z)$ and $z = f_z(\Delta x,\Delta z)$ are look-up tables representing the non-linear field law in the cross section of the BPM pick-up.

Beam phase

The FPGA computes the following values

- $I=(A_n+ B_n +C_n+ D_n)$, in phase signal
- $Q = (A_{n+1}+ B_{n+1} +C_{n+1}+ D_{n+1})$, quadrature signal

(phase and quadrature with respect to a $f_{clock}/4$ reference signal) .

- $\Sigma= (I^2+Q^2)^{1/2}$: amplitude signal

It output ϕ, phase signal, with $\cos \phi = I/\Sigma$ and $\sin \phi = Q/\Sigma$

Averaging and filtering

A signal synchronous with the revolution frequency allows the selective acquisition and processing of data over a fraction of the revolution period as shown on figure 1; the position and phase signals can also be averaged inside a revolution period or over several turns in order to ease the detection of the various signals observed on a SR beam: synchrotron and betatron oscillations, low frequency beam motion due to the ground vibrations, etc. Space is still available on the FPGA for further processing like FIP filtering or digital frequency down conversion.

STATUS AND TEST RESULTS

System tested

A test system is working. A device server allows it to transmit four blocks of 2048 processed data on the compact PCI bus. The acquisition of the data blocks is triggered using the storage ring revolution frequency signal and a low repetition rate data block acquisition trigger as shown on figure 1.

Resolution of the pic- up signal detection

For a beam signal with an amplitude half of the full ADC input range (+/-1024LSB) and a uniform storage ring bunch filling (22Msps flow of valid data), the following signal to noise ratio would be expected, providing the front end electronics noise is negligible:

A,B,C,D signals: 130dBc/Hz

Σ signals: 136dBc/Hz

I/ Σ and I/ Σ signals: 130dBc/Hz

This would result in a phase resolution of 3.10^{-7} rd/$(Hz)^{1/2}$ and a position resolution of 2.5nm/$(Hz)^{1/2}$ or 1μm turn-by-turn for our 35 mm gap vacuum chamber.

Resolution of the pick-up signal detection

However it is not realistic to neglect the noise contribution of the RF front end, especially for the phase detection. For the phase detection, the frequency range of interest is around the synchrotron frequency f_s; On the ESRF storage ring, f_s about 1.5 KHz. A 278.35MHz local oscillator to be used in our RF front-end would have to exhibit a phase noise of less than 130dBc/Hz at 1.5 KHz from the carrier to have a negligible effect on the resolution of our system. On our prototype system, the phase resolution at 1.5KHz was limited to 6.10^{-3}rd/$(Hz)^{1/2}$ as shown on figure 3 since our prototype local oscillator uses a 20% tuning span VCO.

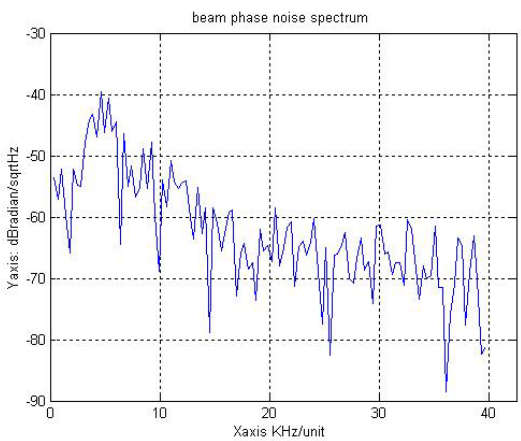

Figure 3: Plot of the spectrum of the phase signal, showing the detrimental effect of the local oscillator phase noise on the resolution.

On the final design, using a custom-made VCXO with a –97dBc/Hz phase noise at 1.5KHz from the carrier, we expect a 2.10^{-5}rad/$(Hz)^{1/2}$ resolution, which is about the resolution required to monitor the random phase jitter of our beam at the synchrotron frequency.

Resolution of the beam position detection

The beam position detection relies on an amplitude detection of the IF signals coming from the RF front-end. The amplitude detection should be almost insensitive to the local oscillator phase noise. We actually found a position detection resolution of 10nm/$(Hz)^{1/2}$, or 4μm turn-by-turn.

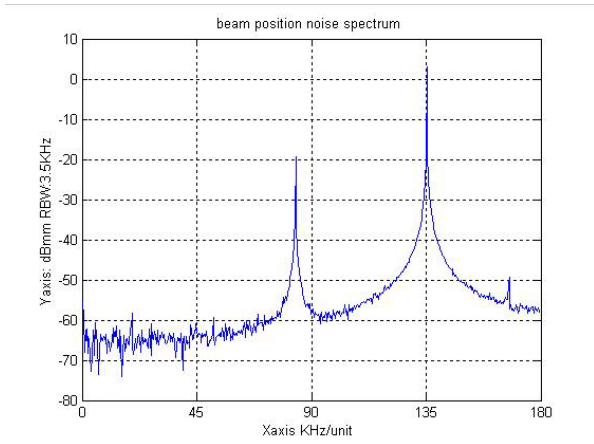

Figure 4: Plot of the spectrum of the position signal (oscillation amplitude: 2mm/ vertical scale: dBmm)

CONCLUSION

The use of a FPGA board together with a high level algorithm development environment allowed the design of a relatively sophisticated BPM/beam phase monitor using mostly standard components. However, the clocks and the oscillator of the RF front-end must be designed carefully in order to avoid spoiling the potential performance of such a design.

AKNOWLEDGMENT

This work is based on the "CUB" FPGA board and ADC mezzanine developed by J. Cerrai and G. Goujon from the Digital Electronics Group of the ESRF. The RF front-end circuits and the RF synchronous clocks were developed by P. Arnoux of the Diagnostics Group.

REFERENCE

[1] R. Ursic, "Digital receivers offer new solutions for beam instrumentation,"PAC'99, New York, April 1999.

[2] http://www.xilinx.com/products/software/sysgen/product_details.htm