FAST DSP USING FPGAs AND DSOs FOR MACHINE DIAGNOSTICS

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Abstract

Digital signal processing using digital signal processors is now a mature field for machine diagnostics, giving significant benefits, in particular when used to analyse BPM signals for tune measurement and fast feedback systems. We discuss here digital signal processing using Field Programmable Gate arrays (FPGAs) with large gate counts and intelligent oscilloscopes. These offer great potential for the analysis of very fast signals to maximize the information extracted from high bandwidth sensors.

i) FPGAs allow data to be filtered numerically and treated at the speed of data collection of A/D converters in the 100MHz range. Parallel, fast and continuous treatment of BPM and FCT signals is possible. Examples are given of injection efficiency, turn-by-turn injection efficiency, turn-by-turn beam position, amplitude and phase calculation with averaging over each turn or many turns.

ii) Modern oscilloscopes include much computational power. In-built DSPs can perform correlations on the traces allowing the application of FIR filters. Some oscilloscopes incorporate a PC and allow on-board manipulation of the data using MATLAB. An example is given using an FIR applied to a 5GHz oscilloscope to extend its time response to measure electron bunch lengths less than 100ps with 1ps resolution.

PLATFORMS FOR PERFORMING DIGITAL SIGNAL PROCESSING

- Digital Signal Processor boards
- Digital Storage Oscilloscopes with processing capabilities (in-built maths operations and or PC with Matlab)
- Field Programmable Gate Arrays (FPGA)

The use of DSP boards for treating signals from diagnostic sensors is now well established (eg for feedback systems). The increase in acquisition speed of Analogue to Digital converters coupled with the large memory capacity of recent generation oscilloscopes puts a heavy demand on the network bandwidth and on post-processing. At such speeds pre-treatment of the signal with a view to extracting the useful information and reducing the bandwidth of the data to be exported becomes all the more important. The latest generation of fast intelligent oscilloscopes offer interesting possibilities for the pre-treatment of fast signals. For the ultimate in pre-treatment data bandwidth, FPGA boards may also be used.

DIGITAL STORAGE OSCILLOSCOPES

Figure 2 shows the layout for a system using a 12GHz photo receiver [1] and a high bandwidth digital storage oscilloscope [2]. Modern digital storage oscilloscopes provide means for exporting waveform data to on board software running on the internal PC. Pre-processing of the waveform data may also be performed using standard maths library functions on the Oscilloscope DSP. Further processing on the PC part of the oscilloscope may be performed using analysis packages such as Matlab. By

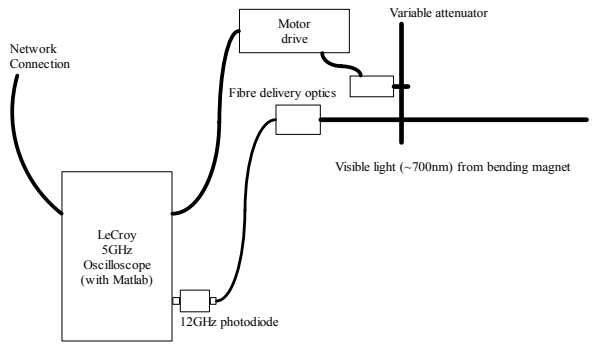

Figure 1 Optical Layout of bunch length measurement

programming custom functions using Matlab it is possible to perform tasks such as:

i) bunch length measurement by deconvolution of the instrument response

ii) beam phase monitoring (both fast and slow drift).

In order to perform deconvolution of the instrument response (to extend the effective bandwidth) it is important to process very clean, noise free, waveforms of high precision (10-12bits). Such waveforms should be recorded by averaging many repetitions of the waveform. A very stable trigger is required in order to maintain resolution when averaging. Using this technique, we have been able to measure pulses as short as about 95ps, see figure 2. A trend of the bunch length is shown in figure 3 during operation in a high bunch charge filling-mode, which suffers charge dependent bunch lengthening. This technique provides means of permanent monitoring of the bunch length without the continuous operation of a streak camera [3].

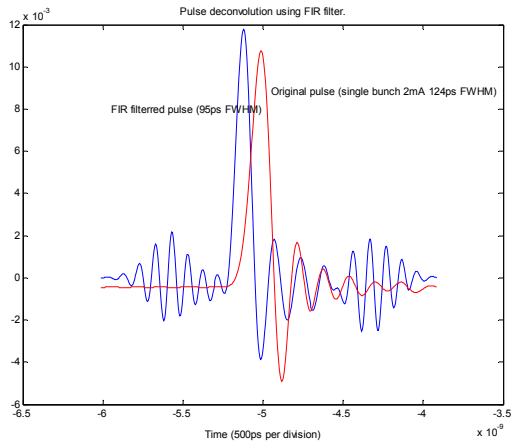

Figure 2 Reduction of pulse width by deconvolution of the instrument response

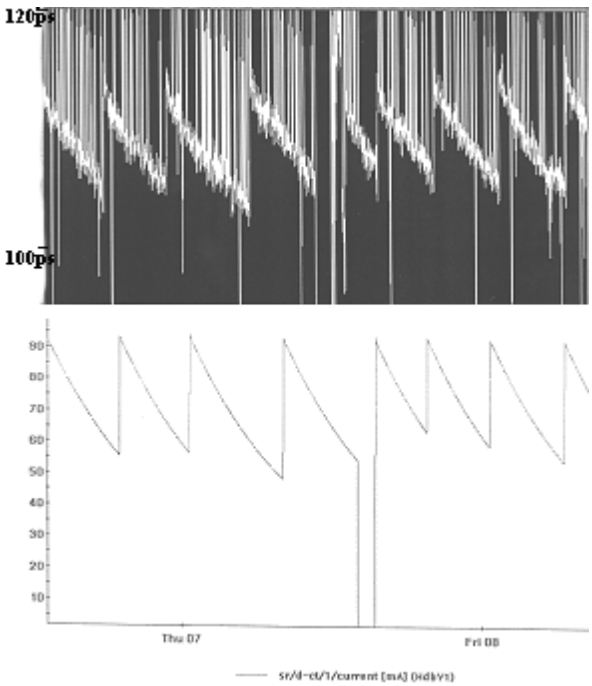

Figure 3 Monitored pulse length (upper trace) and beam current (lower trace)

Other applications of pre-processing of oscilloscope waveforms are:

i) Turn by turn beam current determination from fast current transformer signals.

ii) Bunch purity measurement using single photon counting of synchrotron radiation.

FIELD PROGRAMMABLE GATE ARRAYS (FPGA)

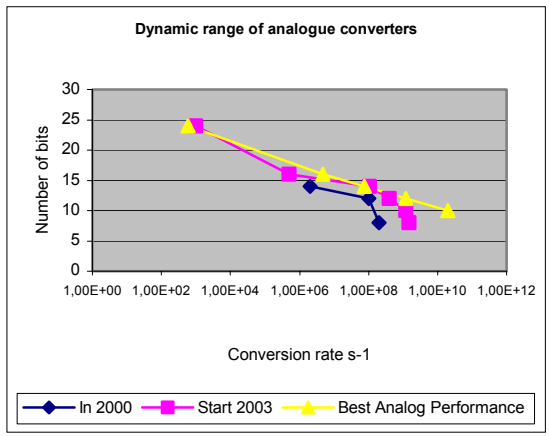

Figure 4 performance of A/D converters

The current performance of analogue converters is shown in figure 4. The data rate produced by modern high speed A/D converters exceeds the capacity of even the fastest of DSPs. As can be seen from the table below however, these high data rates can be processed using modern FPGA chips.

Function	Industry's Fastest DSP Processor Core	Xilinx Virtex-II Pro Platform
8x8 Multiply Accumulate (MAC)	4.8 Billion MAC/s fclk = 600 MHz	1 Trillion MACs/s fclk = 300 MHz
FIR Filter* 256 Taps, Linear phase* 16-bit data/coefficients	9.3 MSPS fclk = 600 MHz	300 MSPS* fclk = 300 MHz
Complex FFT* 1024 point, 16-bit data	10 µs fclk = 600 MHz	1 µs* fclk = 150 MHz
Viterbi Decoding Throughput	Five hundred channels at 7.95 Kbps for a total of 3.9 Mbps*	155 Mbps (OC-3 rates)
Reed-Solomon Decoding Throughput	4.1 Mbps fclk = 600 MHz	10 Gbps** (OC-192 rates) fclk = 85 MHz
Turbo Convolutional Decoder Throughput	Six 2 Mbps data streams* (6 iterations)	5.4 Mbps** (6 iterations)

Table 1 Comparison of DSP and FPGA performance. Courtesy Xilinx

Though the programming of FPGAs has in the past been quite difficult, the recent development of high level programming tools combined with the ability to simulate the target application has made the process much easier.

Figure 5 shows a graphical programming environment for FPGAs using toolbox System Generator from Xilinx [5], which runs under Simulink (Mathworks).

Injection Efficiency

The current signal from fast current transformers installed on the transfer line into the storage ring and on the storage ring itself are converted using 12 bit ADCs at 22.7MHz. This sampling frequency represents 64 measurements per turn (see fig 6). The signals from the two current transformers can be compared using a cross-

correlation technique, summing the product of corresponding signal values over 1 turn.

$$Injeff_n = \frac{\sum_{1}^{64} I_{TL2} \times (I_{SRafter-n} - I_{SRbefore})}{\sum_{1}^{64} I_{TL2} \times I_{TL2}} \qquad (1)$$

Equation 1 is used to calculate the percentage of the charge added to the storage ring after turn n. This calculation may be performed over several turns in order to monitor the injection efficiency during the capture process as shown in the graphical application (figure 7).

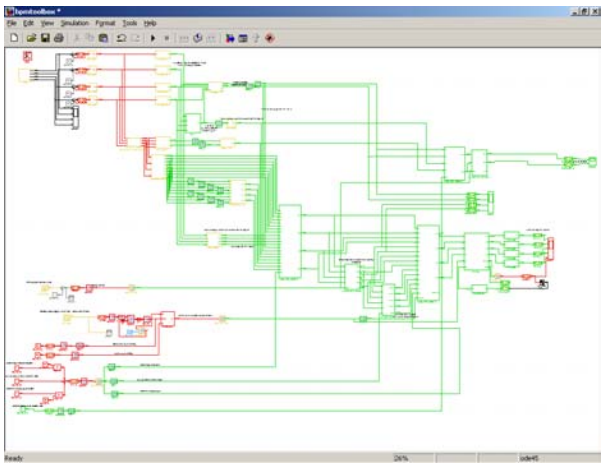

Figure 5 Development of processing algorithm using Simulink

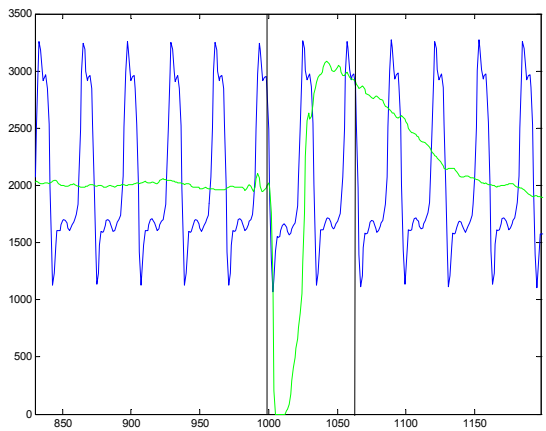

Figure 6 Data converted from 2 Fast Current Transformers

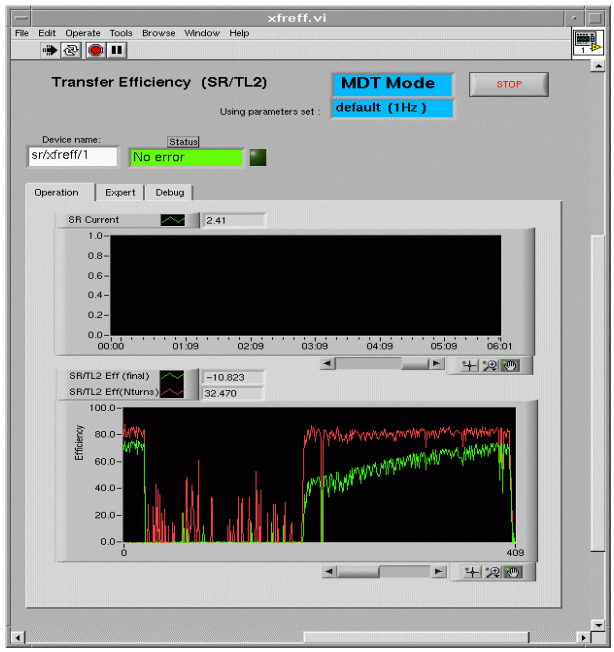

Figure 7 Injection efficiency after 10 turns (upper trace) and after 2000 turns (lower trace)

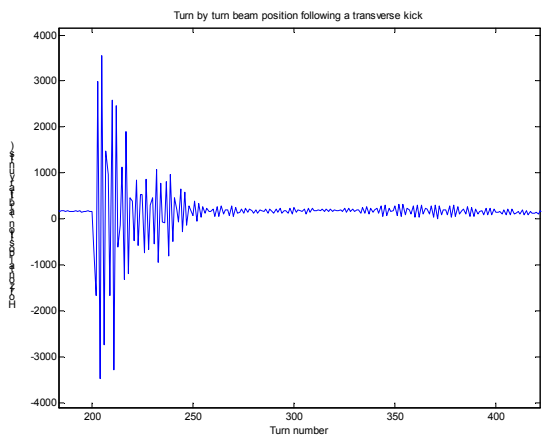

Figure 8 Turn by turn measurement of beam position using an FPGA

ACKNOWLEDGEMENTS

This work was made possible by the following:
Christian Herve, Jacques Cerrai, Gerard Goujon, Gonzalo Penacoba, Jean-Marc Koch, Eric Plouviez, Francis Epaud and Pascal Verdier

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