STATUS OF RF DRIVER AND PHASING SYSTEM FOR PLS 2.0 GEV LINAC

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Abstract

The RF system of PLS linac contributes to effectively get the capability of producing an electron beams with an energy of 2.0 GeV. It is essential to provide the optimum condition of the RF drive signal for 11 klystrons, and make the phase synchronization between the electron bunches and the accelerating waves, which would result in electron beam energy spectrum broadening. For this purpose, the RF drive and phasing system is established. In this paper, the status of the RF system for the PLS 2 GeV electron linac is presented, which includes the system design and the operation status of each subsystem, such as an RF booster drive system, IPA unit and phase control system.

1 INTRODUCTION

There are 12 high-power klystrons including injector station and modulators, and 10 SLED-type pulse compressors to provide pulsed RF accelerating fields at 2856 MHz in the PLS linac^[1]. These klystrons are presently being operated at the output power of 50 to 65 MW for 4 μ s width, 30 Hz repetition rate, and 240 W drive signal. The overall schematic integration diagram of the RF driver and phasing system for PLS 2.0 GeV linac is shown in Fig.1.

The electron bunches in the accelerator must ride on the RF crests for a maximum energy gain. There are several reasons why this condition may not be fulfilled, such as incorrect initial phasing requirement, asynchronism of the RF wave with electrons caused by incorrect frequency or incorrect temperature control, and poor bunching. The change of any parameter in RF frequency, phase, and power gives influences on the electron beam energy gain and the energy spread. The magnitude variation of these factors depends on various conditions such as the drive signal of klystrons, a modulator beam voltage, and environmental conditions. The beam voltage of a modulator is stabilized less than \pm 0.5% fluctuation level by the SCR DC feedback control system^[2]. The temperature of accelerating sections is accurately controlled within $45\pm0.2^{\circ}C^{[3]}$. The phase stability of 145-m long main drive line is less than $\pm 3.5^{\circ}$ during 72 hours^[4]. On the basis of these conditions of the related subsystem, the phasing accuracy between the traveling RF wave crests and the electron bunches in the accelerator must be within $\pm 5^{\circ}(\theta=0.1 \text{ rad})^{[5]}$. This can be reached to 99.5 % beam energy gain of its maximum value. In the current machine operation of the PLS linac, the beam energy maximization technique is being used as the phasing procedure. This method is to individually optimize the phase condition of each klystron by the

maximizing energy gain and minimizing spectrum width one by one. The IPA system is only operated in the present state of the phasing method. Involving additionally a PAD system, which is at the last stage of field test can make the automatic RF amplitude and phase control. In the following paper, each of these related subsystems is described in detail.



Fig. 1. Schematic diagram of 2.0 GeV PLS linac RF system

2 RF DRIVE SYSTEM

There are three parts in the drive system: RF booster signal source to drive the preinjector klystron, the main drive line to transmit the drive power coupled out from the preinjector klystron for driving 11 klystrons remained, and IPA units to adjust the power level and the phase of the drive power.

2.1 Booster Signal Source

The booster signal source consists of a master oscillator, low-level signal conditioning unit, and a solid-state amplifier. The high precision synthesized signal oscillator(HP 8665A) is used to generate the 2,856 MHz master frequency. The frequency stability is 5×10^{-10} /day, and the phase noise is -137 dBc/Hz at 10 kHz offset. The low-level signal-conditioning unit, designed and fabricated by PAL, is contained with a preamplifier, CW phase reference signal amplifier, isolator, and PSK module. The PSK unit can be operated to 2-W CW and its typical switching time is shorter than 50 ns. The solidstate amplifier(Nihon Koshuha PRFA-S801A) adopts Cclass pulse type, multi-cascade method and the power combination circuit, and amplifies the PSK module output to 800 W for driving the preinjector klystron. The output power of this amplifier is adjustable from 400 W to 720 W and pulse width from $2 \mu s$ to $7 \mu s$. It's rise and fall times are about 0.2 μ s and 0.1 μ s, respectively.

2.2 Main Drive Line

The main drive line of 1-5/8" air dielectric rigid coaxial cable transmits the 2856 MHz, 120 kW pulsed drive power coupled out from a waveguide cross coupler(26.5 dB) located in the preinjector waveguide network to the end of the accelerator. It consists of 45 straight pieces, 2 right angle elbows, 2 expansion sections, 11 couplers, and a dummy load, and its total length is 154 meters. The expansion sections are for compensation of the longitudinal thermal expansion due to the temperature variation in the drive line. The nitrogen gas facility and the cooling control requirement are also prepared to enhance a phase stability, not activated at the present state of operations because there is little affect due to these provisions. There are 4 kinds of coupling coefficients in 10 couplers to extract the klystron drive power from the main drive line. Approximately 120 kW power is supplied to the main drive line. The output power at each directional coupler is 2~3 kW ranges.

2.3 Isolator-Phase Shifter-Attenuator (IPA)^[6-7]

The IPA system provides the isolation of the main drive signal from the reflected drive signal at each klystron as well as the control of the phase and amplitude of the drive power for each klystron. An IPA system consists of two units of a RF unit and an electrical control unit. There are two controllable components in the RF unit: a phase shifter and an attenuator. The phase shifter is a rotary-field type and is digitally controlled from 0° to 360° by a current driver. The attenuator is a strip-line variable type and its attenuation is varied from 0 to 20 dB by a DC motor control. One-chip microprocessor circuit developed at PAL can control them locally or remotely.

2.4 RF Power Monitoring System

The RF power monitoring system is to measure each klystron output status, and monitor the amplitude modulation effect on the RF output pulse. Major units are a RF detection and distribution board, and an electronic process board, which is equipped in a unit case of 19" EIA standard panel. The RF detection/distribution board includes an amplitude detector with a low pass filter and two 70-dB monitor ports for both the forward and reflected power circuits, and provides a DC voltage signal to the process board. The amplitude detector that rectifies the peak of the RF voltage has the linearity over a 20-dB range with ± 5 % accuracy and has the excellent long-term stability. By the process board, various data display circuits are considered such as output power level, VSWR protection, and temperature indication. Those informations can be monitored in the control room via RS-232 interface provision. This control and monitoring circuits are also developed at PAL.

3 RF PHASE AND AMPLITUDE CONTROL SYSTEM

The RF phase and amplitude control system is under development for a PLS 2.0 GeV linac, which consists of a phase reference line, a phase and amplitude detection unit,

and a 2856 MHz reference source. This control system is automatically operated to stabilize the energy of electron beams. The phase reference line, 7/8 inches of diameter, 50Ω phase compensated semi-rigid coaxial cable, is used to feed the phase reference signal of 10 mW into each phase detector unit. The IPA unit now in operation is a low-level acting device to control the RF phase and amplitude of the klystron drive power. The phase and amplitude detector unit measures the amplitude of a pulsed power of klystron output used to provide accelerating fields, and phase difference between the klystron output pulse and a distributed CW phase reference signal at the same frequency. The prototype of the RF phase and amplitude control system is assembled with a new type controller for the IPA unit, and the field test is under preparation.

3.1 Phase and Amplitude Detection Unit^[8-10]

The phase and amplitude detection system is to measure and stabilize the pulsed RF power of klystrons, and then contributes for phase feedback control and for amplitude and phase jitter detection. This system consists of an RF front-end board and an electronic controller, and has the following functions: provide a measurement of amplitude and phase of microwave pulses in the watt to kilowatt peak power range at 2856 MHz with pulse widths of 1 to 4 μ s; produce video outputs of the pulse measurement; take a sample of amplitude and phase at a sampling time and digitize these values; provide instrument control and calibration functions.



Fig. 2. PAD unit block diagram of RF front-end board

The RF front-end board is designed to provide a detected amplitude and phase signal for the RF pulse with a power level of up to 3 kW. This board combines the following circuits or components as shown in Fig. 2: a large signal amplitude detector unit, a double balanced mixer as nulling phase detector, a 180° electronic phase shifter, a $\pm 90^{\circ}$ wobbler and directional couplers. The phase reference signal enters at a power level of 10 mW. To handle the large difference between power levels and avoid crosstalk, the RF front-end board is constructed in stripline with each circuit line channelized by plated through holes in the top and bottom PCB about $\lambda/16$ apart from each other. At an electronic controller, the

amplifiers, sample/hold functions, and an ADC are used to digitize the amplitude and phase data, and a DAC is implemented to control the voltage variable phase shifter. The digital control logic is provided to allow control of the timing of the sample and hold gates and the phase modulation of the reference signal. The noise isolation is also important for the reliable system operation in the noisy linac environment. The control processor is a 89C52 based microcontroller packaged in a 19" unit cases. The software in this controller specifies the operating modes of the RF front-end board and the specific measurement technique. This control software is an integral part of the phase and amplitude detection system. The architecture of the electronic controller is shown in Fig. 3.



Fig. 3. Electronic controller architecture for PAD unit

3.2 Phase Reference Line

Stable phase reference signal is required for the accurate phase measurement. This signal has to be available at 14m intervals for 11 klystrons except an injector module along the 154-m accelerator. To make these frequent drop-out points a reference line was chosen the highstabilized phase compensated, 7/8", 50 Ω , and semi-rigid coaxial cable using a foam dielectric, insensitive to changes in humidity or atmospheric pressure with a temperature coefficient of ±9 PPM/°C(Endrew LDF5-50A). This allows a 100 m cable length to be stable to $<1^{\circ}$ in electrical length for ambient temperature changes of 30 °C. Each 14-m reference line segment is enclosed with a heater insulation material for preventing an effect due to an environment temperature variation, which drop out 10 mW phase reference signals with 11 couplers. The total required reference power is about 5-W CW at 2856 MHz frequency.

4 SUMMARY

With the system upgrade of a new IPA controller, it is possible to control the rotary-field phase shifter with 0.1 ° resolution and 1° error, and the strip-line variable attenuator with a fine tuning. At the PAD unit of a prototype setup, the phase is measured with a resolution of 0.1°, and has the typical sensitivity of 7.47 mV/degree. The output response of amplitude detection has a good linearity and 60.75 mV/mW at the load resistor of 3.01 $k\Omega$. At the next stage, it is desire to develop the fastacting, electrical controllable high-power RF component such as phase shifters and attenuators operated at power levels to 4 kilowatts pulse. These devices are very useful for IPA system. This allows a real-time computer control of the RF system, and will be processed as the next system upgrade program.

5 ACKNOWLEDGMENTS

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