RF SYSTEM AT HIRFL-CSR MAIN RING

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Abstract

A heavy ion cooler-storage ring HIRFL-CSR[1] has been constructed at IMP. It consists of a main ring (CSRm) and an experimental ring (CSRe). Two RF cavities will be employed for CSRm. One is for beam acceleration, and another is for beam RF stacking. The accelerating cavity is designed to accelerate the beam from 10-50MeV/u to 400-900MeV/u with harmonic number h=1. The peak RF voltage is 8.0kV and frequency range is from 0.25 MHz to 1.7 MHz. The RF stacking cavity with maximum voltage amplitude of 20kV and tunable frequency range 6.0-14.0 MHz is used to capture the injected bunches from injector SSC (or SFC) and to accumulate the beam to high intensity by RF stacking method. In the present paper, the designed RF parameters and the details of hardware for the RF system are described.

1 Main Parameters of CSRm ring

CSRm has a maximum magnetic rigidity of 10.4 T.m, corresponding to $^{12}C^{6+}$ energy of 900MeV/u. The main parameters of the ring are shown in Table 1.

Table 1:Main parameters of CSRm

Circumference	161.2 m
Maximum magnetic rigidity	10.4 T.m
Max. Beam energy	900 MeV/u
Average radius	25.65 m
Rising time of magnetic excitation	3.0 s
Transition energy γ_{tr}	4.76

2 MAIN RF PARAMETERS

RF Acceleration Parameters

The specifications RF acceleration system of CSRm ring is shown in Table 2.

Table 2: RF Accelerating parameters

Injection Energy	10-25 MeV/u
Acceleration energy	900 MeV/u
Momentum spread at injection	< ±0.15%
Revolution frequency	0.25-1.7 MHz
Harmonic Number	1
Acceleration frequency	0.25-1.7 MHz
Maximum RF acceleration voltage	8.0 kV

The Lowest injection energy is 10 MeV/u for $^{238}U^{72+}$ ions among various ions from the injector SSC (or SFC), corresponding to the revolution frequency 0.25 MHz. At the top energy of 900 MeV/u for $^{12}C^{6+}$, the revolution frequency is 1.7 MHz. The harmonic number 1 will be employed to accelerate the ions thus the RF frequency should cover the frequency range from 0.25 MHz to 1.7 MHz. The Maximum acceleration voltage of 8.0 kV is needed for the beam acceleration with ±0.15% momentum spread within acceleration period of 3.0s.

3 RF CAVITIES

Two RF cavities will be employed for beam acceleration and RF stacking respectively. All of them have a single-accelerating-gap structure, which consists of two ferrite-loaded quarter-wave coaxial resonators.

3.1 Ferrite material

We selected the ferrite material 600HH and 200HH for accelerating cavity and RF stacking cavity respectively. The dimension of ferrite rings is 480mm in outer-diameter, 300 mm in inner-diameter and 20 mm in thickness. For accelerating cavity, ferrite rings are assembled in 4 stacks, 2 stacks for each of the two halves. Totally, 80 pieces of ferrite disks are stacked in an entire cavity. For RF stacking cavity, 48 ferrite disks of 200HH are assembled in whole cavity.

3.2Design of cavity

The cavities are load with ferrite rings, cooling copper plates, bus bars for bias currents. The average permeability $\bar{\mu}$ and dielectric $\bar{\varepsilon}$ constant in the cavity are represented by the following relations:

$$\phi = \ln(\rho_2/\rho_1)/\ln(r_2/r_1) \quad (1)$$

$$\mu_e = [1+\phi(\mu_r - 1)]d_1/(d_1+d_2) \quad (2)$$

$$\varepsilon_e = 1/(1-\phi) \quad (3)$$

$$\bar{\mu} = \mu_e \mu_0 \quad (4)$$

$$\bar{\varepsilon} = \varepsilon_e \varepsilon_0 \quad (5)$$

where ρ_1 and ρ_2 represent the inner and outer diameters of ferrite disks, r_1 and r_2 are the inner and outer diameters of the cavity, d_1 and d_2 are the thickness of ferrite disk and cooling plate, μ_r, μ_0 and ε_0 are the relative permeability of ferrite, the vacuum permeability and dielectric constant respectively. In the present designed cavities, the numerical values are: $\rho_1 = 300mm$, $\rho_2 = 480mm$, $r_1 = 200mm$, $r_2 = 642mm$, $d_1 = 20mm$, $d_2 = 2mm$. The inductance L_0 and capacitance C_0 of the coaxial resonator per unit length are presented by

$$L_0 = \bar{\mu}\ln(r_2/r_1)/2\pi \quad (6)$$

$$C_0 = 2\pi\bar{\varepsilon}\ln(r_2 / r_1) \quad (7)$$

And the characteristic impedance Z_0 is $Z_0 = \sqrt{L_0 / C_0}$. The shunt impedance R_s is expressed by.

$$R_s = 4\pi \times 10^{-7} \times < \mu_r Qf > \times (\mu_e / \mu_r)^2 \times G \quad (9)$$

Where G is a geometric factor of the cavity, namely

$$G \equiv \ln^2(r_2 / r_1) \cdot l \cdot (d_2 + d_1) \cdot (r_1 + r_2) / 2d_1 \cdot (\rho_2 - \rho_1)$$

And $< \mu Qf >$ is an averaged $\mu_r Qf$ product of ferrite. The RF power loss in the entire ferrite is given by

$$P = V_g^2 / 2R_s \quad (10)$$

According to the numerical calculation, at the operation of $V_g = 8.0kV$ for accelerating cavity, the maximum power dissipation in the whole cavity is 20 kW. And for RF stacking cavity, the maximum power dissipation in the ferrite is also 20 kW at the operation of $V_g = 20.0kV$. In table 3 the main parameters of cavities are shown.

Table 3: Specifications of the RF cavity

Frequency range	0.25 – 1.7	MHz
Harmonic number	1	
Peak RF voltage	8.0	
Peak RF power	20	
Total length	2.6	m
Ferrite material	600HH	
Ferrite ring dimensions	$480\times300\times20$	mm^3
Number of ferrite rings	80	
RF induction in ferrite	130	mT.MHz

4 LOW LEVERL RF SYSTEM

The low-level RF electronic system is composed of a Direct Digital Synthesizer (DDS) as the master oscillator and several feedback loops (Fig.1). Three memory modules store the ramping data: frequency, acceleration voltage and bias current as functions of bending-magnet field strength. These pre-set data are put into the DDS, magnitude modulation and bias current power supply respectively. The bias current error obtained from RF signal phase detector which get the deviate of the RF cavity by comparing the plate's and the grid's sampling signal will be used to correct the deviation of the cavity through the auto frequency control (AFC).

RF signal control unit is developed as PCI bus based modules. All these modules are independent sub-system, which have their own MCU.

4.1 DDS Circuit

The RF signal process applys the advanced DDS plan. The AD's AD9832 is functioned with the 16BIT processor in parallel connect mode to achieve high synthesis updating of signal. The local control processor sends data to DDS chip to release the RF signal. At mean time DDS receives the information from the control system to adjust the outputting frequency.

4.2 Phase Loop

Phsase loop is used to compensate the deviation between the DDS and cavity voltage, achieving phase lock among RF cavity voltage and cavity voltage phase. All sample signals serving above units come from one identical detector, each of them has its own isolator to proof interference.

4.3 Bias Current Control Loop

The signal of V/F converted from the DDS synthesis's RF signal or the signal of D/A converted directly from digital data applying to DDS input is put to FREQ/RES adjusting unit to control the bios current. The offset value from MCU and the signal from phase discriminating between the cavity voltage and grid of the final stage power amplifier are also fed into this unit. The FREQ/RES correction must be a real time analogy circuit to dynamically tune the cavity. The signals after F/V converter, which represents the changing of the frequency, add one from the phase discriminator. The sum is put into the bios current driver to control the saturation of the ferrite so as to tune the cavity.

MCU/DAC 's data compensates the nonlinear relation between the bios current and the permit of the ferrite and offsets the bios current's initializing value.

4.4 RF Frequency Control Loop

RF system requires frequency resolution be less than 100Hz, frequency stability less than 10^{-5} thus requires non less than 16Bits control word and less than 1us update rate of frequency sweeping. The digital dividing PLL may meet the requirement, but it update speed is determined by the frequency resolution. The fact is that the higher the frequency resolution the lower the updating speed. This is determined by the LPF of the PLL loop. Furthermore at high dividing rate 1/N requiring by large frequency range, the loop gain drop to 1/N to damage the loop stability, at this situation the high stability power supply is needed to meet the critical requirement. The advanced DDS tech can resolve this problem.

Applying 16Bit/32Bit MCU or PLD to control the DDS RF signal processing circuit to attain high speed and real time control. 16Bit of amplitude data are also applied to amplitude modulation unit, which also serves as amplitude stability control to achieve 10^{-2}-10^{-3} rate. The bios current data supplying by MCU are converted by DA to feed into the bios current power supply which actuating the coil. Bios current error derived from the deviation of cavity's resonance and DDS frequency tunes the cavity through AFC. MCU connected with PCI bus receives the control word. All DAC and ADC are high-speed products.

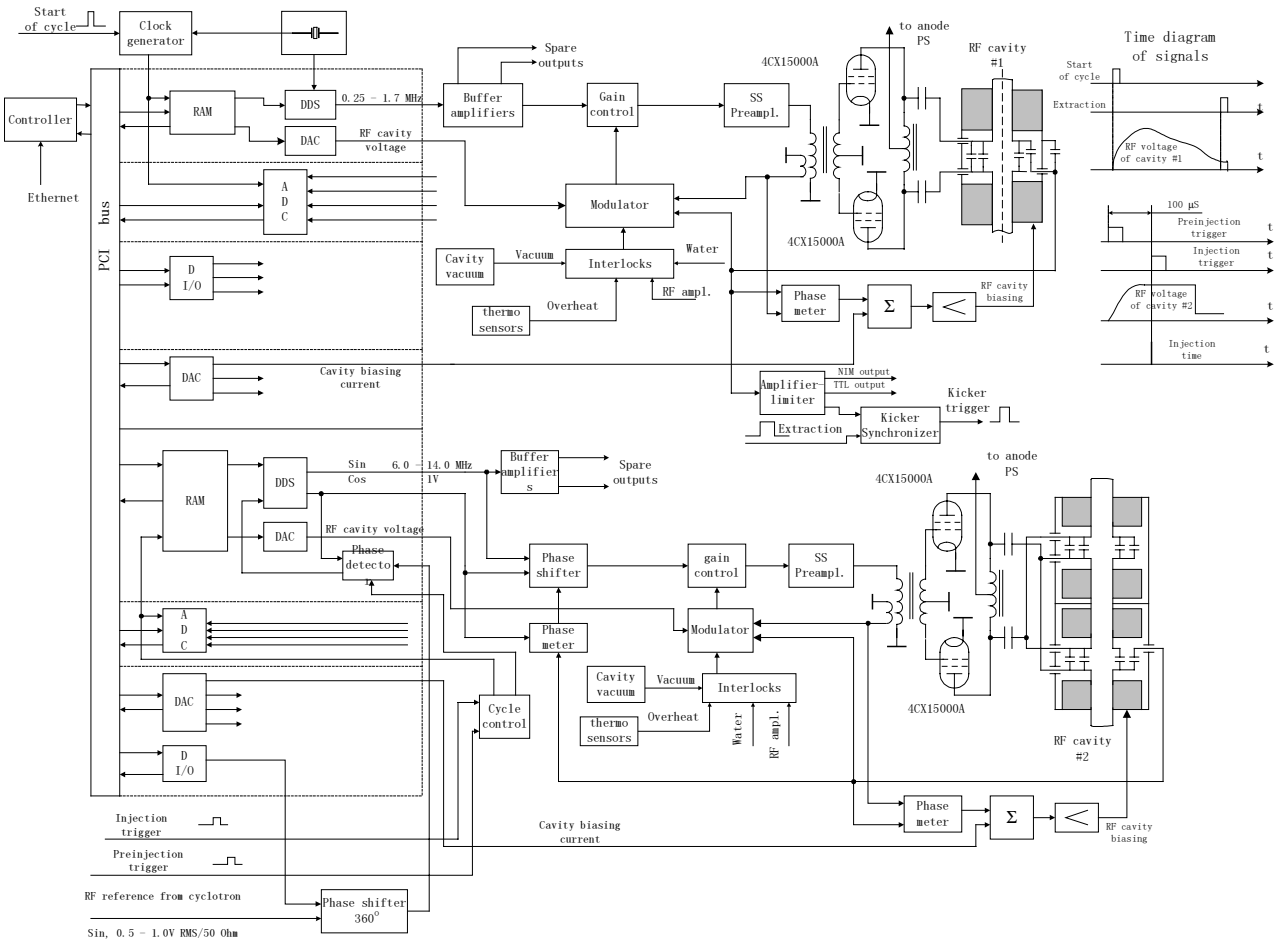

Figure 1: Block diagram of CSRm RF system

The connection between the RF and CSR control bus applies PCI function module and particular parameter and timing network.

REFERENCES

[1] J. W. Xia et al. “HIRFL status and HIRFL-CSR project in Lanzhou”. APAC’98, KEK, Tsukuba, Japan, March 1998.