Multipurpose Controller Based on a FPGA with EPICS Integration

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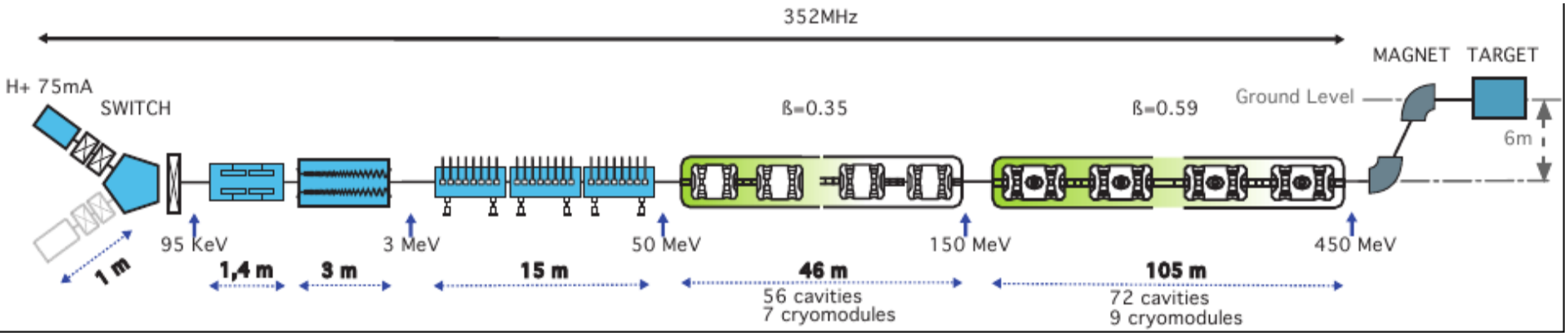
Outline

1. ESS-Bilbao Overview
2. Introduction
3. System description:
   - FPGA
   - Host PC
4. Host PC program
5. XML configuration
6. Applications
   - Beam position monitoring
   - Low Level RF

ESS-Bilbao Overview

- In-development **LINAC in Bilbao (Spain).**
- Will accelerate **H^+ and H^- beams up to 50 MeV in the first stage, and plans to reach several hundreds MeV in a later second stage.**
- Pulsed beam up to 1.5 ms long, up to 75 mA of peak current.
- Source (75 keV) → LEBT → **RFQ (3 MeV) → MEBT → DTL (50 MeV)**



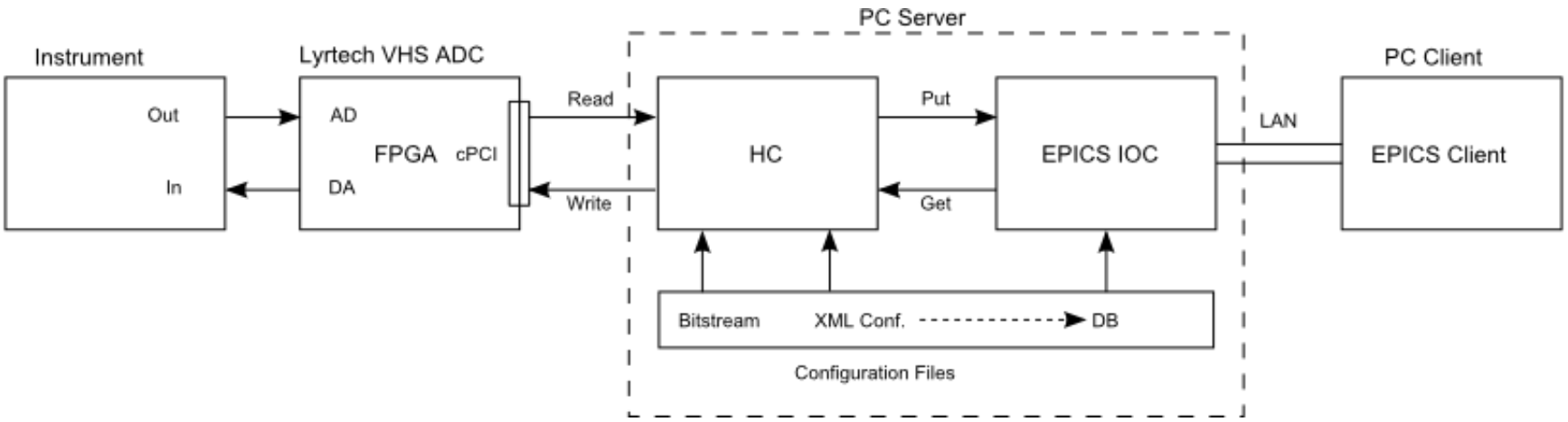
Introduction

- Beam diagnostics and design of control systems are key issues
- Real time necessity: fast signal acquisition and fast calculation rate
- Normally, when a system is tuned, it is controlled remotely

Local real time control with high performance hardware
and
Distributed networked control with a proper information management

- This works details a multipurpose controller based on:
  - High performance digital board.
  - Host PC with EPICS server using JavaIOC

System description



Formed by two elements:

- A Lyrtech VHS-ADC board: real time algorithm
- Host PC:
  - Reads and writes parameters to FPGA
  - EPICS server
  - Configured by XML files

System Description: FPGA

Lyrtech VHS-ADC board:

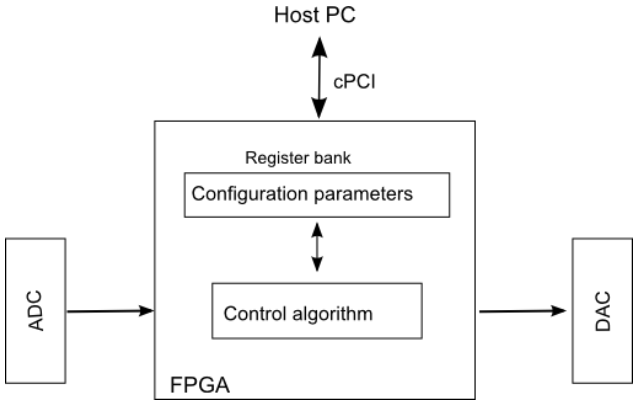
- Virtex 4 FPGA: 152000 logic cells. Up to 500MHz.
- ADC: 8 channels. Up to 105MHz.
- 128 MB SDRAM.
- Several clock sources.
- Expansion connector.
- Several communication channels.

Design tools:

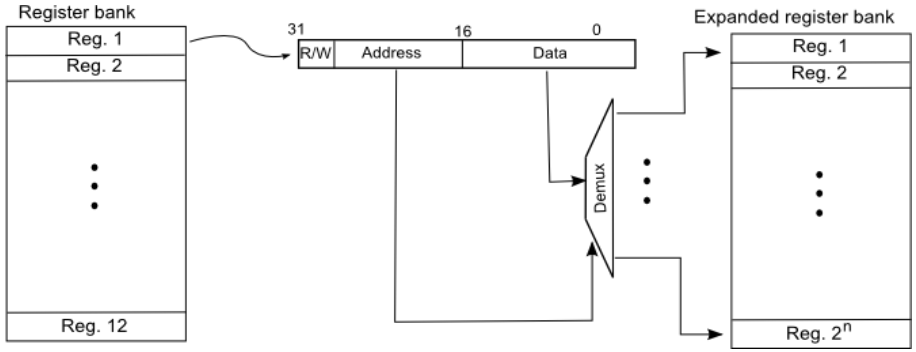
- Hardware: VHDL, Verilog or schematics → Xilinx ISE.
- Hardware/Software → Xilinx Embedded Development Kit.
- Xilinx System Generator + Matlab Simulink → Hw-in-the-Loop simulations.

System Description: FPGA

- Lyrtech provides a “by default” design for controlling peripherals.
- Bank of 12 registers of 32 bits.



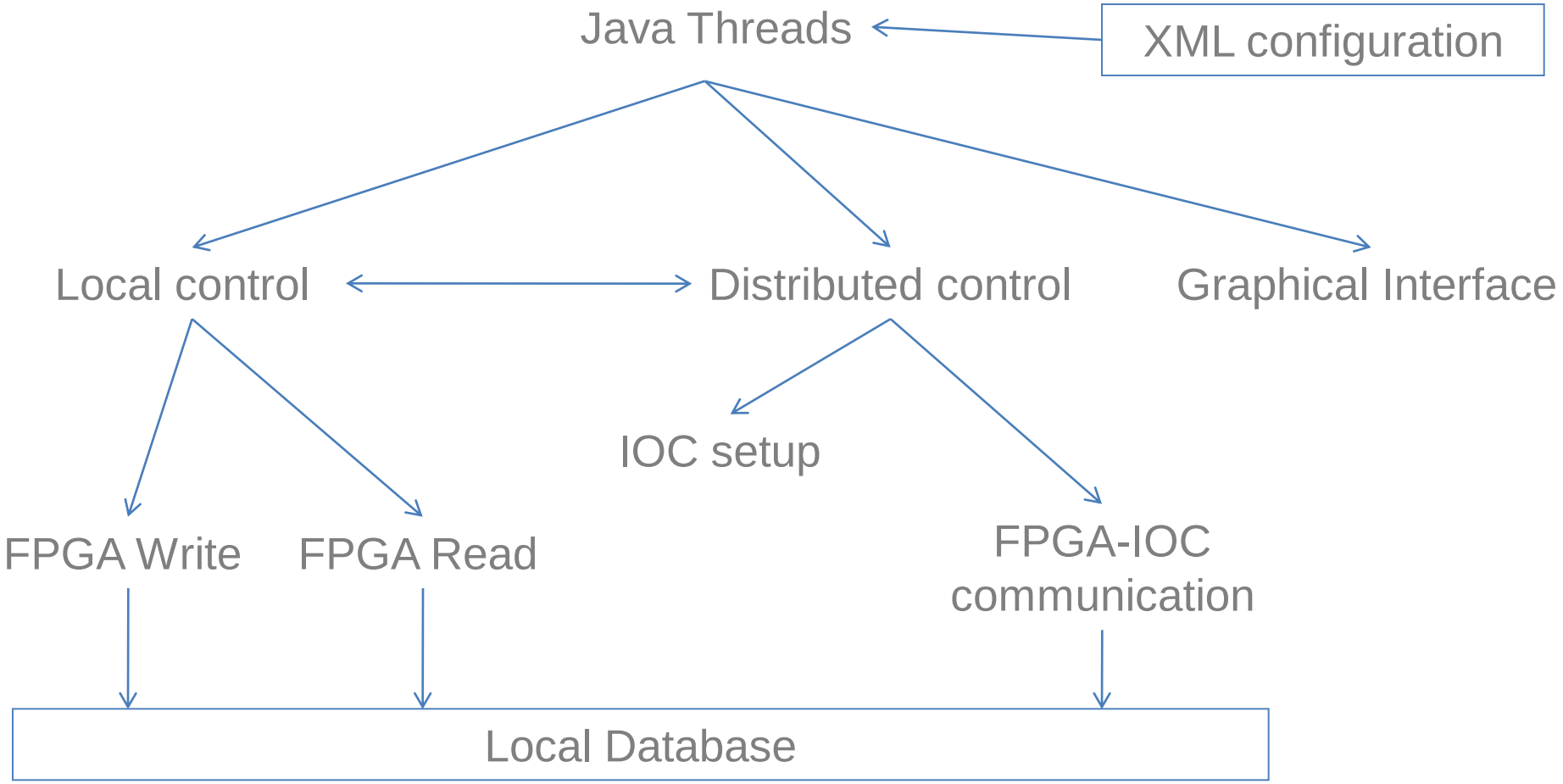
- The register bank can be expanded to 2^{15} 16-bit registers:



System descripton: Host PC

- Connected to the FPGA through cPCI bus.
- Simple control software to configure FPGA peripherals.
- Hardware-in-the-Loop simulations can be made with Matlab Simulink.
- Lyrtech provides an API for final software implementation.
- We built a Java application using Java Native Access

Host PC Program



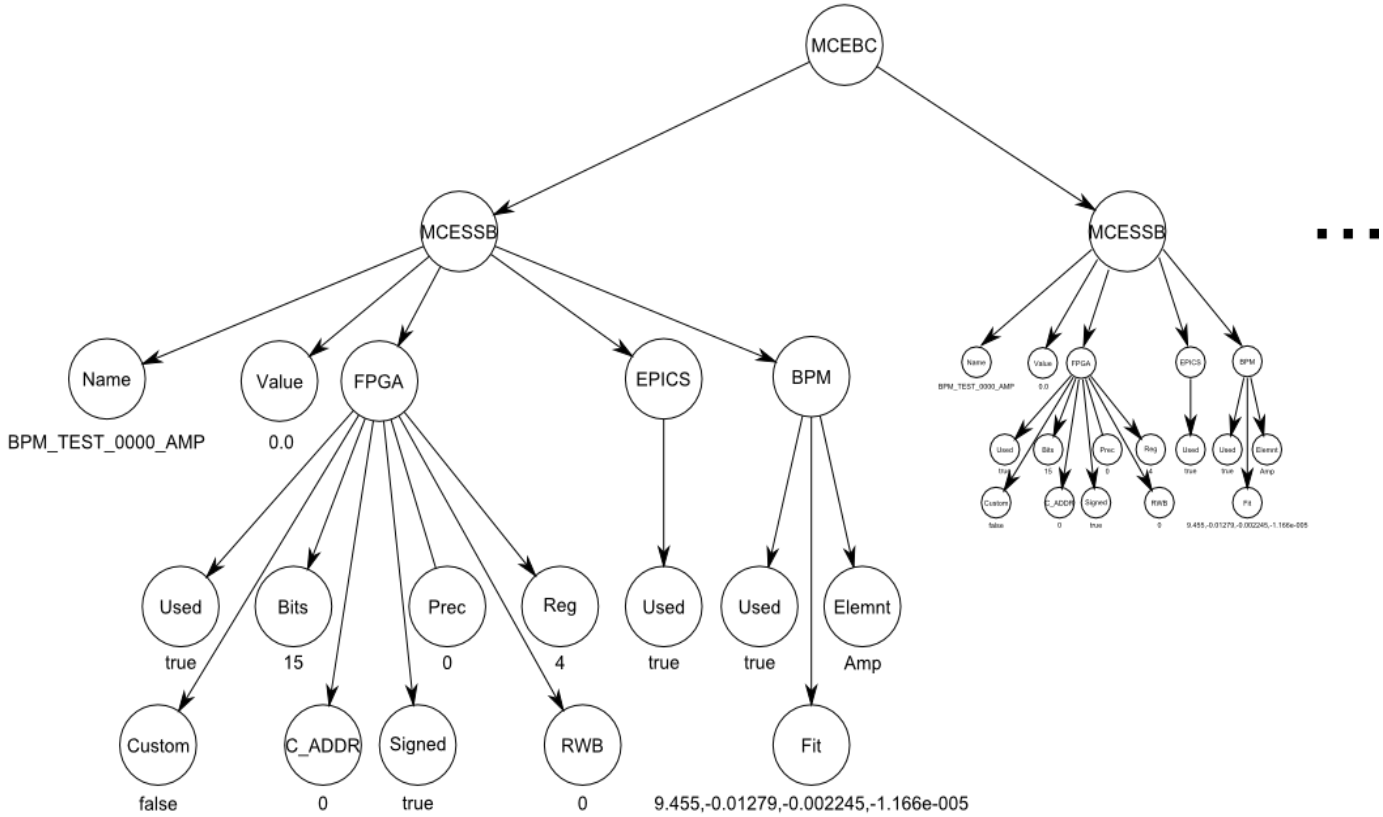
Program details

- Local thread: Lyrtech API (JNA)
- Distributed thread: Lyrtech API (JNA) and EPICS (JavaIOC)
- IOC Database: type, sampling rate, alarms,…
- EPICS clients: for example Control System Studio (SNS)
- Two possibilities for the database:
  - RDBArchiver
  - Specific developed Java library to record PVs structure

XML configuration files

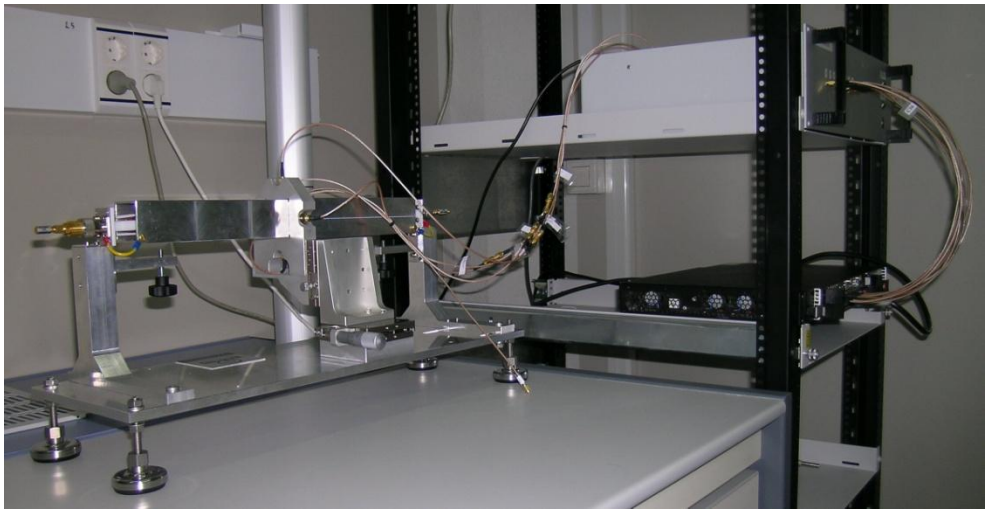
- Controller configuration parameters and IOC parameters

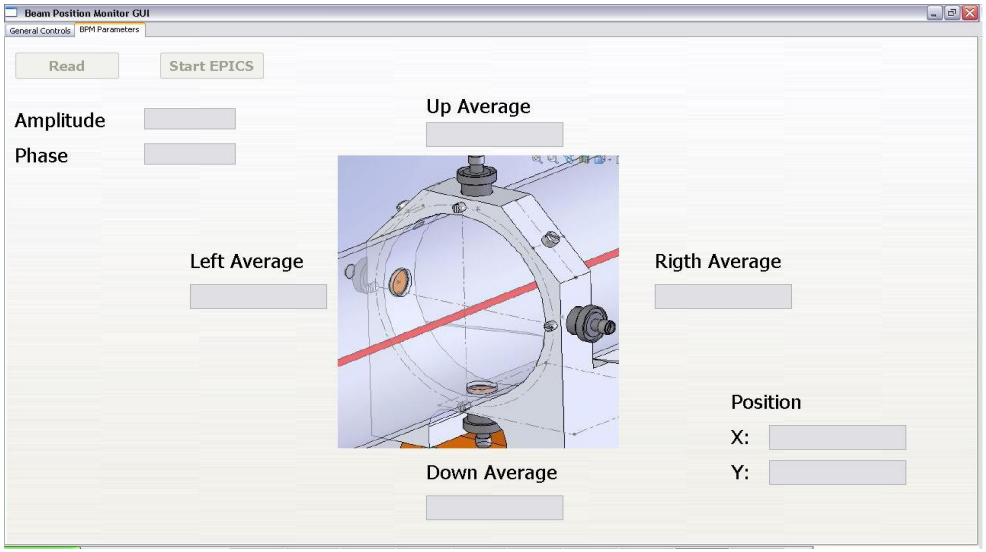
```
<MCEBC>
 <MCESSB>
  <Name>BPM_TEST_0000_AMP</Name> >
  <Value>0.0</Value>
  <FPGA>
   <Used>true</Used>
   <Bits>15</Bits>
   <Prec>0</Prec>
   <Reg>4</Reg>
   <Custom>false</Custom>
   <Custom_ADDR>0</Custom_ADDR>
   <Signed>true</Signed>
   <RW>0</RW>
  </FPGA>
  <EPICS>
   <Used>true</Used>
  </EPICS>
  <BPM>
   <Used>true</Used>
   <Element>Amp</Element>
   <Fit>9.455,-0.01279,-0.002245,-1.166e-005</Fit>
  </BPM>
 </MCESSB>
 <MCESSB>
  <Name>BPM_TEST_0000_PHASE</Name>
  <Value>0.0</Value>
  <FPGA>
   <Used>true</Used>
   <Bits>28</Bits>
   <Prec>14</Prec>
   <Reg>5</Reg>
   <Custom>false</Custom>
   <Custom_ADDR>0</Custom_ADDR>
   <Signed>true</Signed>
   <RW>0</RW>
  </FPGA>
  <EPICS>
   <Used>true</Used>
  </EPICS>
  <BPM>
   <Used>true</Used>
   <Element>Phase</Element>
   <Fit>0</Fit>
  </BPM>
 </MCESSB>
```



Applications: Beam Position Monitors

- Test stand with 4 buttons
- FPGA: Cordic algorithm
- Host PC:
  - Δ/Σ algorithm
  - Linearization
- Two BPMs per system





Applications: Low Level RF

- Analogue front-end for preprocessing
- RF signal distribution system
- Power supply unit
- Tuning unit
- FPGA: 3 control loops validated using Hw-in-the-Loop
- Hardware controller and EPICS server under development.

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