EMBEDDED SYSTEM ARCHITECTURE AND CAPABILITIES OF THE RHIC LLRF PLATFORM*

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Abstract

A high performance field programmable gate array (FPGA) based platform has been developed for the RHIC Low Level RF system upgrade, and is now replacing our aging VME based systems. This new platform employs a sophisticated embedded architecture to implement its core functionality. This architecture provides a control system interface, manages remote access to all configuration parameters and diagnostic data, supports communication between all system components, enables real time application specific processing, monitors system health, etc. This paper will describe the embedded architecture and its capabilities, with emphasis on its application at RHIC.

SYSTEM OVERVIEW

A major goal of the low level RF upgrade was to develop a digital signal processing platform which incorporates the latest advances in technology to obtain better performance, flexibility, ease of deployment and maintainability. The standard controller consists of a carrier board hosting up to six daughter modules [1], mounted in a 19" rack mount chassis. This format moved us away from the traditional use of VME systems, giving us better control over the electronic noise environment and facilitating deployment in remote areas. Both the carrier and daughter boards employ a Xilinx Virtex-5 FPGA with a PowerPC 440 embedded hard processor core supported by a wide set of peripherals. An embedded architecture was developed for the carrier and each daughter board to provide the PPC440 access to the different peripherals. The carrier PPC440 runs a custom generated VxWorks kernel [2] and is configured as a standard RHIC front end computer (FEC) providing control system interfacing compatible with the existing RHIC infrastructure. Daughter card CPUs are configured to run various versions of function specific code, including data acquisition, wave form generation, feedback loops, remote configuration and local parameter control.

BASIC HARDWARE

The basic hardware consists of a carrier board with six XMC daughter sites. The carrier and daughter boards were designed to use a large Xilinx-5 FPGA with a great number of peripherals such as a large memory bank, Flash memory, RS-232 and gigabit serial transceivers (GTX) [1]. External Connectivity is provided by gigabit Ethernet ports and four Small Form Factor Pluggable (SFP) transceiver modules connected to GTX on the carrier FPGA. Other import features of the hardware include four sets of controls data link receivers and temperature, current and voltage monitoring of all major components.

THE EMBEDDED DESIGN

The process of defining the internal architecture of the FPGA to allow a processor access to the set of peripherals usually starts in the early stages of the overall system design process. We used the Xilinx Embedded Development Kit (EDK) to create an architecture that supports the different peripherals on our boards.

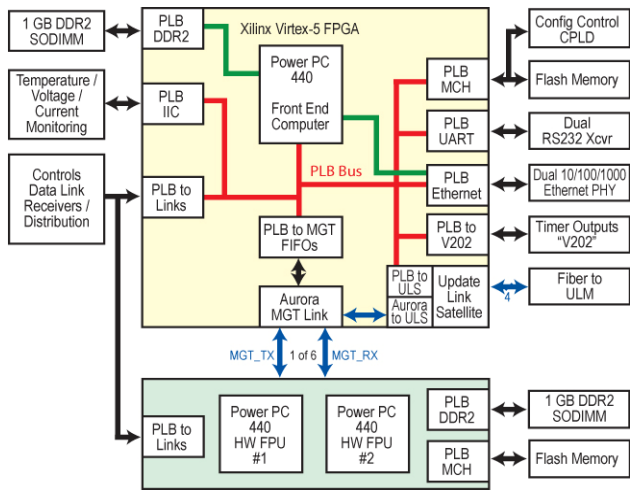

Figure 1: Block diagram of a carrier embedded design showing connection to daughter board.

The carrier FPGA is configured to run the PowerPC 440 at 400MHz and to access most of its peripherals over the processor local bus (PLB) as shown in Figure 1. Peripherals that required higher performance such as the Ethernet port and main memory controller were configured for direct CPU access over dedicated point-to-point buses that make use of hardware crossbar interconnect instead of a shared PLB.

Xilinx tools provide a large set of free IP cores that allow for interfacing the many external peripherals to a processor core. Examples of such cores are illustrated in Figure 1 and include: an external memory controller to control the Flash device, a DDR2 memory controller for the PowerPC 440, PLB to UART to connect to external RS232 port and a PLB to Ethernet IP core. These cores were used on our multiple designs and required only minimal configuration.

An additional set of custom IP cores was developed to provide the various systems an interface to specialized functionality unique to the LLRF. Examples of custom designed IP cores include: embedded versions of the

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RHIC V108 utility module and V202 delay generator, the Aurora communication link, a PLB to update link master (ULM) core and a PLB to IIC Bus.

Embedded Utility Module

The embedded utility module provides the FEC with synchronized, ring equipment parameters via Real Time Data Link, synchronous software event execution (Event Link) and FEC remote reset capability. This core is also used on the daughter card designs when there is need to access RTDL data or to execute functions synchronous to event link events.

Delay Generator Module

A VHDL version of a RHIC V202 delay module was developed for use in the LLRF FEC. This embedded delay generator supports up to 8 PPM users and a single instance can be configured for up to 32 external channels. It is often used to bring delayed events directly to other firmware blocks in our system such as NCO and the phase detector [4,5].

Status Monitor Support

Extensive monitoring of temperature, power supply voltage and currents is available for the carrier and daughter boards. The PLB to IIC bus shown in Figure 1 top left was develop to bring these measurements to the FEC which allows monitoring via the control system.

Aurora Communication Link

Aurora is a point to point, low latency protocol for high speed serial communication. The PLB to Aurora FIFO provides a high bandwidth connection between CPUs on both sides of the GTX Aurora core. Software drivers were developed for ease of communication between the FEC and a daughter card CPU. The aurora GTX was configured as a dual lane design with peak speed of 500 Mbytes/Sec. In practice data transfer between the FEC and a daughter card is limited by the speed of the processors. We have reached data throughput higher than 16 Mbytes/Sec between PowerPCs across an aurora link. A fabric connection from a daughter digitizer to aurora will deliver data to the FEC at much higher rates.

Update Link Access

A deterministic, gigabit serial timing and data link was developed and is used by every sub-system to deliver data used for time critical purposes [3]. The Update Link (UL) consists of a fiber optic network connecting all chassis together via a centralized master chassis we called the Update Link Master (ULM). In the current implementation the UL provides a means of communication between all sub-systems including the FECs, daughter CPUs as well as other logic cores in FPGA fabric.

Remote Re-Configuration

Device drivers and Accelerator Device Object (ADO) software were develop to support remote programming of the flash device which is an integral part of all boards in this platform. A user can download new firmware or software to any board and then remotely reconfigure the card to load the new code into the FPGA.

CONTROL SYSTEM DEVELOPMENTS AND FUNCTIONALITIES

The carrier was designed to connect seamlessly into the existing control system infrastructure via Ethernet. The control system accesses the different daughter resources through the FEC. The PowerPC on the various daughter cards run event-driven, purpose specific, stand alone code instead of an operating system. Standalone code was chosen for the daughter cards over VxWorks to maintain a higher level of determinism and synchronization with the hardware. Examples of standalone code running on a daughter PowerPC include: RHIC wave form generators, feedback loops, etc.

Kernel Developments

We used Wind River Workbench 2.6 to create a VxWorks 6.5 kernel for the carrier PowerPC, and added the necessary software utilities to give it the functionality of a RHIC FEC [7]. The default Xilinx board support package was enhanced by adding kernel support for the configuration flash device. This allows the FEC to manage the flash device for updating FPGA firmware, storing the boot-rom and modifying boot line configuration parameters.

Waveform Generator Functionality

Waveform Generators are used to define each cavity voltage and phase on a RHIC ramp [8]. A new feature of the DAC/DDS daughter module is the implementing of digital IQ modulation and Waveform Generator software in the FPGA [4], replacing analog RF modulators and VME based WFG hardware from the old system. WFG software was ported to run on the DAC PowerPC, maintaining the same functionality of standard VME style WFG. The new WFG uses the same ADO as the VME implementation to present higher level software (WFG GUI) with the same interface. Digital I/Q modulators combined with WFG on the same device is a great improvement for the RF systems in reducing cavity phase drift, eliminating RF noise at the I/Q modulator and providing better dynamic range for control of voltage and phase functions.

Time Stamping And Data Correlation

All LLRF data can be time stamped using a 48bit time stamp generated and distributed by the ULM. Data is usually acquired in a daughter card, tagged with its corresponding time stamp and handed off to the FEC for time stamping at the FEC level. We can guarantee data correlation across all RF chassis within 10us granularity and the rest of the RHIC control system is guarantee to within 1ms.

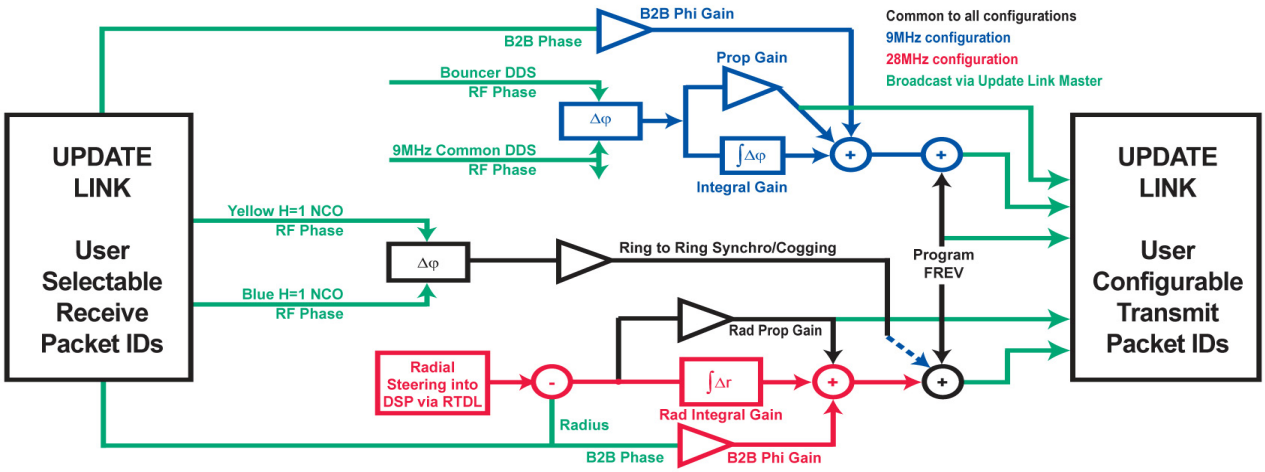

Figure 2: Two modes of Feedback loops configuring simultaneously supported by the DSP.

Beam Control Feedback Loops

The DSP hardware consists of a DAC daughter card populated with a Virtex-5 FX100 with dual PowerPC 440 processors configured with floating point units and used as DSPs. The FPGA provides the DSP with easy access to machine functions over RTDL, event link decoding capabilities and a direct connection to the UL for receiving and transmitting time critical data, Figure 3.

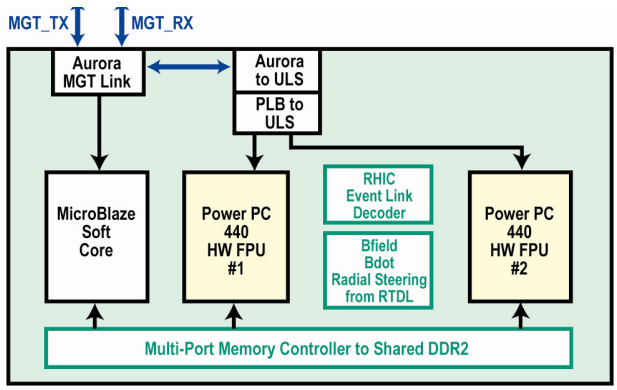

Figure 3: Embedded block diagram of the RHIC DSP.

PowerPC #1 (program DSP) calculates a very accurate open-loop rf frequency derived from the RHIC dipole field transmitted over RTDL [8]. PowerPC # 2 (feedback DSP) process turn by turn radius and bunch to bucket (B2B) phase data to produced a corrected rf frequency word which is used by the Direct Digital Synthesizers (DDS) to generate all RF signals, Figure 2.

This DSP offers much better performance over the previous DSP in three ways. The first is the ability to perform real-time loop computations at faster rate (under 10uS). The second benefit comes from the possibility of generating much larger amounts of diagnostic data accessible by the control system. The final strength of this DSP is the flexibility provided by the use the UL to support very distinct modes of feedback loop operation.

Figure 2 presents a view of the two major loop configurations used to support 28MHz and 9MHz operation. Black represents static configuration elements. Red elements are switched in for 28MHz operation and blue for 9 MHz. Green lines represent UL based connections to other LLRF sub-systems. Details of the loop dynamics are beyond the scope of this paper.

Flexibility in operation comes from the ability of the DSP to trivially reconfigure both internal loop configuration and the packet IDs used to encode data for the UL via user defined parameters. Because sub-systems decode UL data based on these parameterized IDs, connections between the DSP and sub-systems become software defined and dynamic. Thus the combination of an embedded processing platform coupled with the sub-system interconnection afforded by the Update Link provides for a very powerful and reconfigurable system.

CONCLUSION

Systems based on embedded architectures have become common for many applications. The embedded system of the LLRF upgrade supports the goal of providing a custom, flexible platform which seamlessly interfaces with the RHIC control system. It has better performance than the previous VME platform for the LLRF systems. It allows for rapid development and easy deployment of new functionality, and it supports the modular approach to system design.

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