SYNCHRONIZE LASERS TO LCLS e^- BEAM*

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Abstract

Fiber based synchronization system is used in LCLS to synchronize the lasers for pump probe experiments to the average electron beam arrival time[1] . Electron bunch arrival time measured by phase cavity is one of the best measurement represent the FEL X-ray pulse arrival time[2]. The average bunch arrival time is transmitted through electronic length stabilized fiber link to AMO and SXR[3]. The laser oscillators are phase locked to this reference signal to maintain low jitter and drift between pump and probe. The error shows the jitter is less then 100 fs and meets the experiment requirement[8].

INTRODUCTION

LCLS users need perfect timing between the X-ray and laser for the pump-probe experiments to understand all kinds of ultra-fast dynamics. Both electron bunch length and the laser pulse length are at or lower then 10 femtoseconds level. But the jitter between them limit the resolution of experiments. The jitter source can be many things during x-ray and laser generation and propagation. The electron bunch could be jitter around the RF, the FEL lasing process generate jitter between x-ray and the electron bunch, the laser jitter itself, and on the path between the laser and x-ray jitter the could change because of temperature, humidity and/or ground moving. In LCLS case, the laser oscillators are located upstairs in the near experimental hall, where is tens meters away from the experiments chamber. The distance between the x-ray and laser make the jitter and drift problem complex.

The X ray is generated by the free electron laser. The arrival time of the X-ray is correlated to the arrival time of the electron. Electron bunch arrival time measured by phase cavity is one of the best measurement represent the FEL X-ray pulse arrival time [2]. We developed timing and synchronization system to distribute it as a fiducial marker to multiple laser oscillators and also potentially other clients have similar requirements [3].

In this paper, we describe the system configuration and software/firmware architecture for LCLS application.

SYSTEM CONFIGURATION

The ultra-fast timing and synchronization system is illustrate in Figure 1.

Since the NEH laser room located near the center of all the end station, we put the transmitter of the timing and synchronization system there to minimize the overall fiber length.

The transmitter including a cw fiber laser, a Rb frequency locker, a modulator, an amplifier and a sender. The sender consist a splitter and Faraday rotator mirror for each channel in a temperature stabilized chassis. The modulator amplitude modulate the RF fiducial maker onto the cw fiber laser light.

Each link contain one Michelson interferometer to measure the phase variation from the sender to the receiver as a function of time. The short arm is located inside the sender, and the long arm is the fiber we use to transmit time fiducial. Another non-critical long fiber transfer the beat signal of the interferometer from the sender to the receiver. The RF receiver detect the transmitted signal and apply the phase variation to the RF signal. This corrected RF signal is used to control the device under control, here is the lasers and a phase shifter, but can also be a klystron driver signal, or a cavity measurement signal etc.

The cable from the device under control(DUC) to the receiver is not under control, so a SYNChronization HEAD is put away from the receiver chassis to reach the critical signal from the DUC. The beat phase detection and RF phase detection/correction are processed by a LLRF4 board [4] and are integrated in a 3U chassis.

One of the end station is set next to the beam arrival time measurement system to compare the fiducial marker received from the end station with the beam arrival time signal and then adjust the IQ phase shifter in front of the modulater accordingly to maintain them following each other.

SOFTWARE/FIRMWARE ARCHITECTURE

The soft and firmware architecture is shown in Figure2. The higher level interface for the LCLS application is based on EPICS. PVs are archived in the LCLS channel archiver. EDM based user interfaces provide system monitor and control to both operator and expert level users.

IOC driver is running on each end station together with the receiver chassis to communicate with the LLRF4 board. AsynDriver is used in the device support layer to call the usb interface, and provide EPICS PVs. A separate thread is used to communicate with usb port. The FPGA firmware provide registers and waveforms to monitor for each PID control loops.

USB driver and firmware together setup the end point and trigger etc. to provide a transparent communication.

* Work supported by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231
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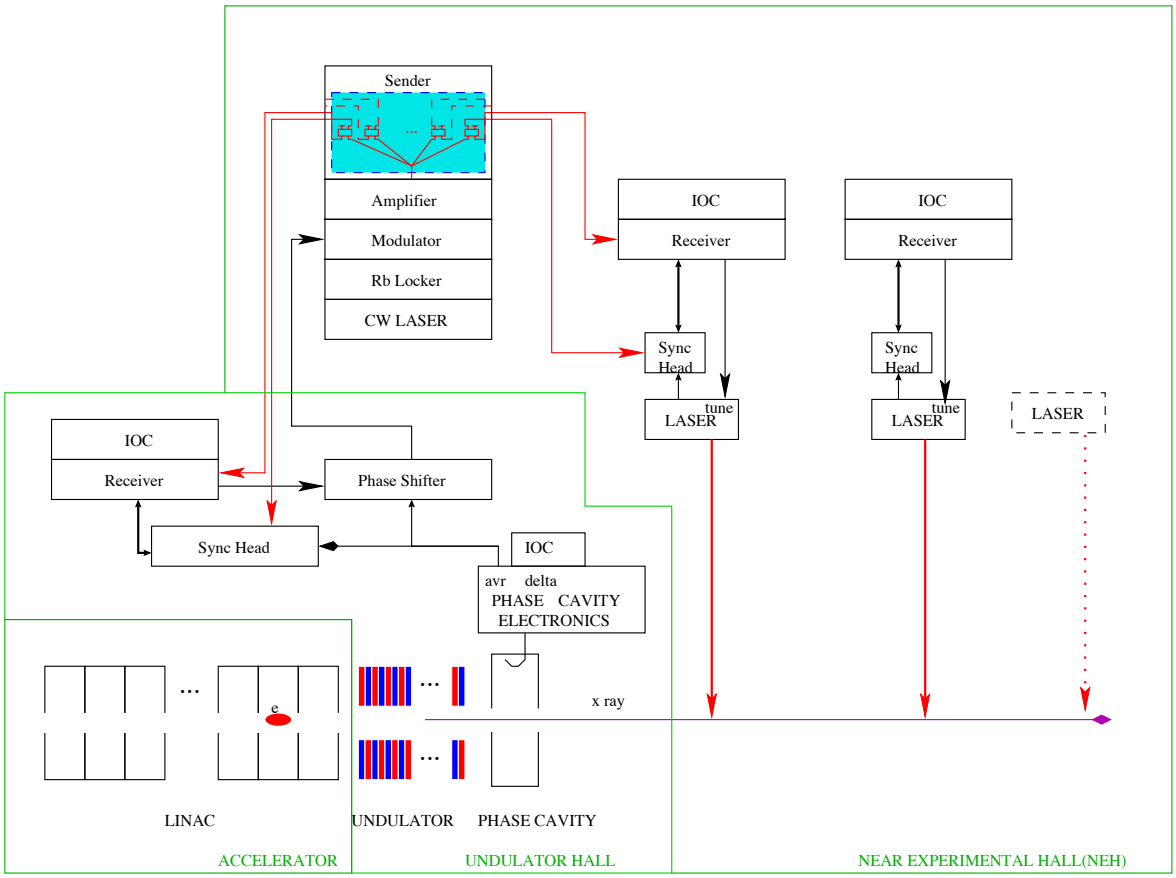

Figure 1: LCLS Berkeley femto-second timing and synchronization system

We adopt the USRP [6] usb driver and the firmware for the FX2 chip, which also provide C interface to the upper level IOC driver.

FPGA firmware including two layers: the board infrastructure and the DSP. The board infrastructure provide all the interface to the hardware, including IF ADC/DAC/, slow ADC/DAC, clock divider etc. The DSP implement all the necessary control algorithm [7]. So the system can just run with appropriate initial setting, which make the usb/ethernet not critical to the system performance.

CONCLUSION AND FURTHER DEVELOPMENT

The ultrafast timing and synchronization system have been running in LCLS since October 2009. Due to the limited channels we have, we can not characteristic the system by ourself after installation.

The overall jitter from the user experiment report less then 100 fs meet the original design requirement[8].

But of course, we and users want a even better system.

- A 16 channel sender and amplifier is manufactured and going to be tested. Once we got this working, we will be able to have a extra receiver somewhere and just measure the out of loop control results.
- The Sync Head and the Receiver chassis are re-engineered under the collaboration with SLAC. Compare to SMA connectorized circuit, using PCB technique make mess production easier. First several set of productions are under final test.

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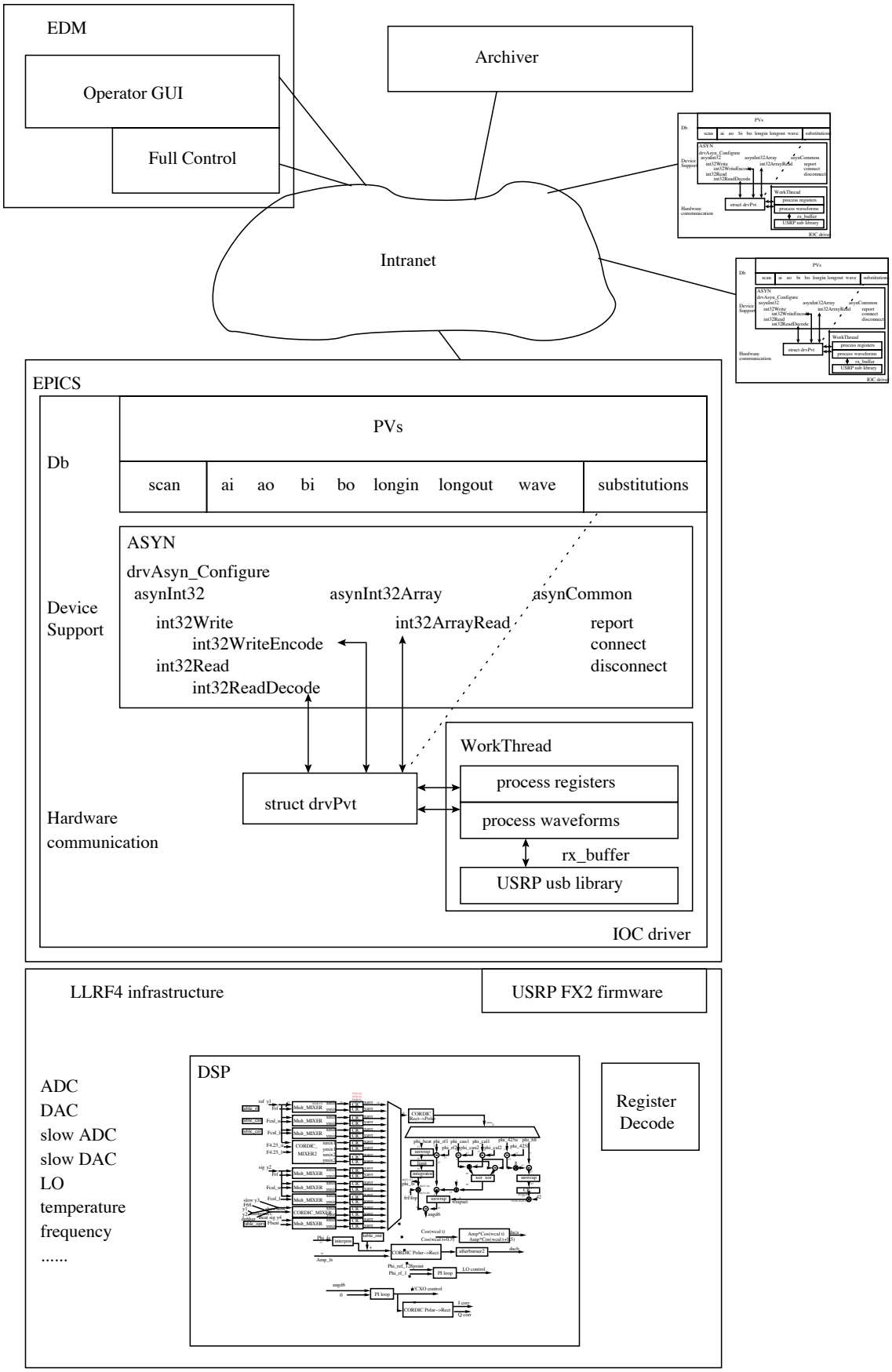

Figure 2: LCLS Berkeley femto-second timing and synchronization system Software and firmware architecture

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