NSLS-II RF BEAM POSITION MONITOR*

Kurt Vetter#, Al Joseph Della Penna, Joseph DeLong, Bernard Kosciuk, Joe Mead, Igor Pinayev, Om Singh, Yuke Tian, Kiman Ha, Young Hu BNL, Photon Sciences, Upton, NY 11973, U.S.A.
Gregory Portmann, (LBNL, Berkeley, CA), James Sebek (SLAC, Menlo Park, CA)

Abstract

An internal R&D program has been undertaken at BNL to develop a sub-micron RF Beam Position Monitor (BPM) for the NSLS-II 3rd generation light source that is currently under construction. The BPM R&D program started in August 2009. Successful beam tests were conducted 15 months from the start of the program.

The NSLS-II RF BPM has been designed to meet all requirements for the NSLS-II Injection system and Storage Ring. Housing of the RF BPM's in +-0.1°C thermally controlled racks provide sub-micron stabilization without active correction. An active pilot-tone has been incorporated to aid long-term (8hr min) stabilization to 200nm RMS.

INTRODUCTION

The NSLS-II RF BPM incorporates the latest technology available in the RF, Digital, and Software domains. A single design has been achieved that meet's all NSLS-II operational requirements for the Injection, and Storage Ring.

This paper will report on the architecture and beam tests conducted at the Advanced Light Source (ALS) at Lawrence Berkeley Lab (LBNL).

BPM ARCHITECTURE

The NSLS-II RF BPM architecture is described below. A high level overview is provided of the hardware, embedded software, and control system.

Analog Front End (AFE)

The AFE topology is based on bandpass sampling. In this particular bandpass sampling architecture the RF fundamental harmonic signal digitally mixes with a harmonic of ~117MHz phase-locked ADC clock in the 9th nyquist zone to produce a digital IF signal at ~30MHz in the 1st nyquist zone. The fundamental 500MHz RF signal is generated by convolution of the 20ps periodic pulsed BPM button signal with a 500MHz bandpass filter response. The frequency domain representation of the signal has a periodic line structure with the line spacing related to the machine bunch fill structure.

The AFE consists of four identical channels, phase-locked loop ADC clock synthesizer, and a phase-locked RF synthesizer for pilot-tone generation. The four AFE receiver channels incorporate standard RF amplifier packaging to enable optimization based on specific use case.

* Work supported by DOE contract No: DE-AC02-98CH10886
#*kvetter@bnl.gov

The receiver has been designed for a highly linear dynamic operational range to mitigate time-varying non-linear beam dependent effects. The receiver parameters referenced to the ADC input are: P1dB=+19dBm, IP3=+43dBm, Noise Fig. = 5.3dB and instantaneous SNR=63dB. The worst-case receiver channel-channel isolation has been measured at 60dB.

The ADC clock synthesizer is phase-locked to the machine clock via external LEMO connection. A phase noise test port is included on a spare synthesizer output to enable phase jitter quantification in real-time directly at ADC clock input. Sub-miniature RF connectors are also provided to enable S-parameter characterization of all four receiver channels. Recently developed Sub-miniature stripline balun technology has been incorporated to optimize phase and amplitude balance to the ADC to improve linearity. Transient Voltage Suppression (TVS) have been incorporated at the receiver inputs to protect device breakdown due to high instantaneous voltage.

An integrated RF synthesizer phase-locked to the ADC clock generates a programmable CW pilot tone for dynamic calibration. The pilot tone is combined with the beam signal within the Pilot Tone Combiner Module.

Pilot Tone Combiner Module (PTCM)

The PTCM is a passive module located on the girder below the BPM button pickup. A 1m SiO2 cable connects the BPM button to the PTCM. The PTCM incorporates state-of-the-art Anaren Xinger sub-miniature integrated RF technology for signal combining. The PTCM consists of a 4-layer PCB contained in a milled Aluminium housing.

Digital Front End (DFE)

The DFE is responsible for all digital signal processing of the button signals and communication of the results with the control system. The main component of the DFE is a latest generation Xilinx Virtex-6 Field Programmable Gate Array (FPGA). The digital signal processing chain consists of four identical channels. Each channel contains a digital down-converter, which is then followed by programmable digital filters which sums the magnitude outputs over a single turn. Further processing yields FOFB (Fast Orbit Feedback) and SA (Slow Acquisition) data. Position measurements can alternatively be obtained by direct frequency domain FFT transformation. A separate processing engine is included to dynamically process the continuous in-band pilot tone.

The FPGA instantiates a soft-core Microblaze processor, which is responsible for all communication with the control system and also coordinates all on-board functionality. Memory for the board is provided with a

1Gbyte SO-DIMM DDR3 memory module. This memory provides the program memory space for the Microblaze as well as a large buffer area for raw ADC data and turn-by-turn data. The total throughput of the memory is over 6GBytes/sec, which is enough to store continuous bursts of raw ADC data, turn-by-turn data, fast-orbit-feedback data and provide program and data memory for the Microblaze.

The BPM communicates with EPICS IOC through gigabit Ethernet interface. On the BPM side, a Microblaze processor running TCP/IP lwIP stack is implemented for robust communication in conjunction with TEMAC Ethernet core. On the EPICS IOC side, Asyn driver based on TCP/IP communication is used. This BPM- EPICS IOC interface provides 10Hz real-time position data as well as on demand requests for ADC, turn-by-turn data, fast-orbit feedback data, and configuration settings.

The DFE provides 6 SFP modules, for communication of fast-orbit feedback data, which supports data rates of up 6.5Gbit/sec. This 10Khz updated data connects directly from the FPGA fabric to the high speed SERDES section of the FPGA. This data is transmitted to dedicated cell-controllers which process the data and provide deterministic low-latency updates to the fast corrector magnet power supplies.

For non-volatile memory the DFE has a single 1Gbit FLASH memory. This FLASH memory stores the FPGA bit-stream as well as the program data for the Microblaze.

An embedded event receiver (EEVR) is included based on a Xilinx Pcore which connects to the Micro -blaze processor. This core uses one of the available SFP connectors on the DFE to receive the incoming event stream.

BEAM TEST RESULTS

Overview

There have been three beam tests conducted at ALS to date where BNL staff has participated at ALS. The first test was conducted in June 2010 with AFE version 1 and DFE version 1 (Virtex-5). The second test was conducted in January 2011 with AFE version 2 and DFE version 1. The third test was conducted in March 2011 with AFE version 2 in conjunction with Virtex-6 transitional platform.

For all tests the NSLS-II BPM was controlled remotely via TCP/IP connection to both Matlab and EPICS from the ALS Control Room. Since the January 2011 test ALS staff has routinely collected data from the NSLS-II BPM via automated Matlab scripts. Typical automated data extraction includes; 1-2 Million raw ADC samples from each of the four channels simultaneously, 1-million samples of X and Y TbT data, 1-million samples of X and Y FOFB data, real-time streaming of 10Hz Slow Acquisition data.

The tests results described below were from the most recent March 2011 beam test on the Virtex-6 based platform with the AFE 2nd revision. Each test was conducted on a split button in order to quantify the BPM noise floor performance. The overall attenuation between the button pickup and BPM electronics is 16dB.

Single Bunch

A single 25mA bunch was injected at the ALS SR in decay mode. A Matlab script was created to automate data capture of 1M ADC samples, and TbT data at 5min intervals. The ALS revolution period is 656ns or 1.52MHz corresponding to 77-samples per turn.

Shown below in Fig.-1 is the single-bunch TbT raw ADC data representing four turns. With 0dB BPM attenuation the ADC level is 22.8k/32,767 counts.

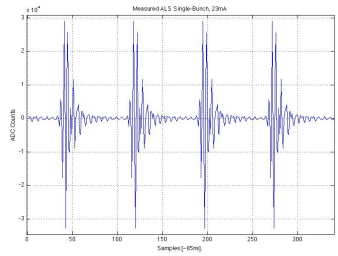

Fig. 1: Measured ALS Single Bunch

Shown below in Fig.2 is a scatter plot and associated histograms for the measured 23mA single Bunch. The measured X and Y TbT RMS position is 9.91um. The X and Y RMS position reduces to ~1um at 10KHz bandwidth.

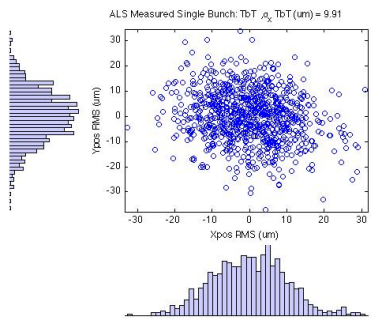

Fig. 2: Single Bunch TbT Scatter-Histogram

Shown in Fig.3 below is the measured position resolution as a function of single-bunch charge.

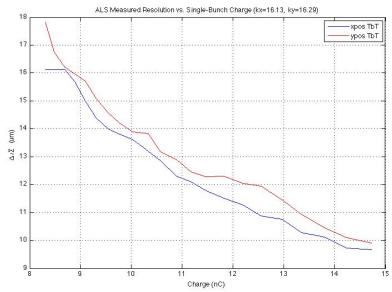

Fig. 3: Measured Resolution vs. Charge

246 Bunch Fill

The ALS was configured for a 246-bunch fill at 500mA in decay mode. This fill corresponds to 75% (i.e. 246/328 bunches). Three single turns of raw ADC data separated by 10-turns is shown below in Fig.4.

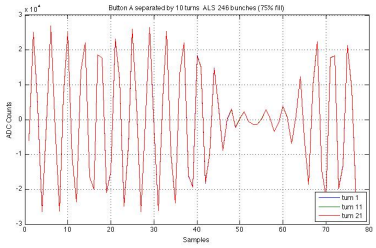

Fig. 4: 246-Bunch 75% Fill Single Turn

Turn-by-Turn data obtained directly from the BPM fixed-point DSP is illustrated below in Fig.5. With the ALS geometric scale factor applied TbT RMS resolution was measured as 1.6um, and 2KHz RMS FOFB data yielded 0.192um, and 0.165um for X and Y respectively.

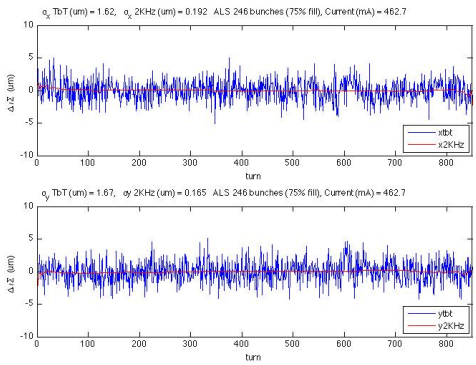

Fig. 5: 246-Bunch TbT and 2KHz Resolution

3-Turn Vertical Kick Experiment

One calibration test of the BPM electronics is to measure turn-by-turn data for a vertical orbit that closes after 3 turns. This was created using a fast magnet operating at one third the revolution frequency with a single bunch. The advantage of doing this is the orbits are different on each of the three turns yet it's a stable orbit with known displacements. One can think of the kick as a DC corrector for three concatenated rings. The measured data in Fig.6 clearly identifies the three distinct vertical positions on each turn at a relatively low single bunch current.

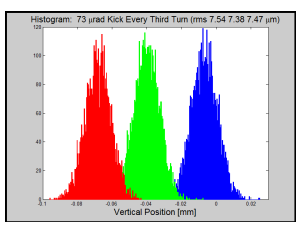

Fig. 6: Orbits kicking every 3rd turn

Table 1: Measured Orbits vs. Orbit Model

	Turn #1	Turn #2	Turn #3
Measured Orbit (mean)	-0.007 mm	-0.040 mm	-0.068 mm
Model Orbits	-0.005 mm	-0.043 mm	-0.078 mm

LONG TERM STABILITY

The major challenge in the development of sub-micron BPM's for 3rd generation and beyond synchrotron light sources is long-term stability. As part of the BPM system stability strategy the dominant thermal effect is predominantly mitigated by the use of highly stable +-0.1°C thermally regulated racks.

Long-Term Stability Test Results

Thermal stability tests are conducted by placing the BPM electronics inside the thermally stable rack. Power splitters and cables are also placed inside the rack. Thermal tests have also been conducted with 50ft of LMR240 cable external to the rack. An Ethernet cable connects the BPM to computer that streams real-time 10Hz data into Matlab.

Thermal stability data illustrated below in Fig.7 was taken during an overnight 11hr period without use of a pilot tone. The RMS variation is 0.233um and 0.289um for X and Y respectively. This set of data was taken with 50ft of LMR cable coiled outside of rack. A 4-way power splitter was located inside the rack.

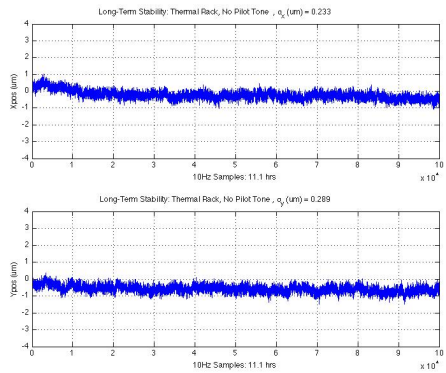

Fig. 7: Measured Long-Term Stability

SUMMARY

The development of a sub-micron BPM for the NSLS-II has successfully demonstrated performance and stability. Pilot Tone calibration combiner and RF synthesizer has been implemented and algorithm development is underway.

The program is currently on schedule to start production development of 60 Injection BPM's starting in the Fall of 2011. The production of ~250 Storage Ring BPM's will overlap the Injection schedule.

REFERENCES

[1] K.Vetter et al., "NSLS-II RF Beam Position Monitor", BIW10, Santa Fe, NM, US.

[2] A.Blednykh et al., "Rogue Mode System Protection From Rogue Mode Coupling", Proceedings of PAC 2011 NY, New York