HIGH DYNAMIC-RANGE HIGH SPEED LINAC CURRENT MEASUREMENTS *

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Abstract

It is desired to measure the linac current of a charged particle beam with a consistent accuracy over a dynamic range of over 120 dB. Conventional current transformers suffer from droop, can be susceptible to electromagnetic interference (EMI), and can be bandwidth limited. A novel detector and electronics were designed to maximize dynamic range of about 120 dB and measure rise-times on the order of 10 nanoseconds.

BACKGROUND/GENERAL THEORY

An ideal beam of current in a linac can be expressed as a series of Gaussian pulses of current separated by a unit of time, t_o, as described $I(t) = \sum_{n=-\infty}^{\infty} I_m(t - nt_o)$, where $I_m(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-t^2}{2\sigma^2}}$. Since the current, I(t), is periodic, the current can be realized as a Fourier series $I(t) = \sum_{n=0}^{\infty} a_n \cos(n\omega_o t), \omega_o = \frac{2\pi}{t_o}$. Many linac beam measurement systems make use of this spectral analysis technique and rely on a measurement of a particular harmonic. For example, beam position and phase measurement systems measure the first and/or second harmonic component, and draw various conclusions about the beam position within the beampipe or beam phase relative to some rf source.

Measurements of a beam harmonic have an inherent advantage that baseband noise, interference, or EMI can be easily filtered and therefore not contaminate the intended spectral measurement. For example, switched power supplies can easily inject parasitic baseband signals into the intended measurement signal and therefore reduce the signal-to-noise ratio. It is desired, therefore, that thermal noise be the limiting factor in many of the linac beam measurements.

To measure the beam current, a measurement of a signal that can be calibrated to an individual harmonic of the beam and is directly proportional to beam harmonic is desired. Many BPM (Beam Position Monitoring) systems rely on this technique, and a signal that is proportional to beam current is reported. Unfortunately, output signals from BPM electrodes by its design are strongly dependent on beam position, and therefore the design of the BPM electrodes can produce a nonlinear calibration of the reported current. Also, many linac BPM systems use an IQ under-sampled/down converted signal processing technique which may not adequately measure the sharp rise/fall times of linac beam, which is essential in any chopped linac current.

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A detector is sought that:

- can successfully measure a signal that is proportional to a beam harmonic,
- does not intercept the beam and can support high intensity operation,
- has an output signal that is independent of beam position as beam traverses through it,
- has a low quality factor (or "Q"), so that accurate rise-times and fall-times can be measured,
- is optimized for measuring high dynamic range.

SYSTEM DESIGN

A description of the overall beam current measurement system is described. Particular and practical design issues are discussed.

Detector Design

The detector design was inspired by a stripline BPM, as it possesses most of the design criteria in the preceding section. A stripline can be optimized for beam response for a particular harmonic, and thereby is optimal for high dynamic range. The output of most BPM designs, however, is dependent on beam position. This effect can be reduced by placing the BPM striplines outside of the beampipe diameter. A schematic of the envisioned detector is depicted in Fig. 1.

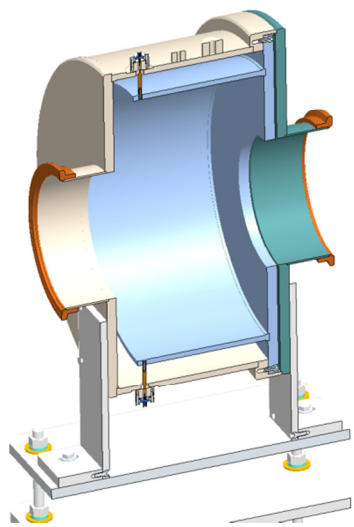

Figure 1: Schematic of the beamline detector.

A circumferentially continuous electrode that is λ/4 in length is short circuited to the wall of the vacuum vessel. Two of the four feed-thrus are shown.

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To optimize the output signal, a single electrode was envisioned to encircle the beampipe, and it was designed to be λ/4 in length. The inside diameter of the electrode and number of feed-thrus were simulated and optimized to have an output signal that is minimally dependent on beam position inside of the detector. Initially, only one feed-thru was simulated for the design. The single feed-thru permitted, however, a strong output signal dependence which was proportional to beam position inside of the electrode. Additional feed-thrus were added to the design until the output sum signal had less than 1% variation on beam position in the beampipe, and the inside diameter of the electrode was close to a factor of two of the diameter of the beampipe. The number of feed-thrus necessary for any particular beampipe is determined by the pipe diameter and frequency of harmonic which is measured. An additional schematic of the detector is shown in Fig. 2.

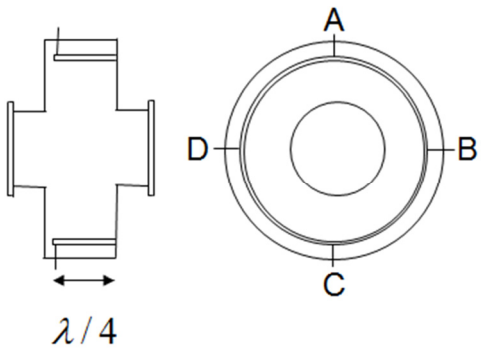

Figure 2: Schematic of detector. Output signal is the sum of the four feed-thrus, A+B+C+D. The frequency and beampipe dimensions required 4 feed-thrus for a 1% variation in output signal for beam signal.

A photo of the installed detector in the injection dump beamline at the Spallation Neutron Source (SNS) is shown in Fig. 3. A combiner is located inside of a green radiation shielded enclosure. Also inside the enclosure is a small circulator tuned to the SNS first beam harmonic, 402.5 MHz, and small single stub tuner.

Analog Electronics and System Design

The analog electronics and overall system design are shown in Figure 4. The signals from the electrode are sent to a summing hybrid. The reflection from the detector itself is 0 dB, and therefore a circulator and single stub tuner is introduced to reduce the reflection from the detector to about -60 dB. The output from the tuner is sent to the long haul cable that goes from the beam enclosure in the tunnel to the service building where the analog and digital electronics are housed in a rack.

From the long haul cable, the signal enters into an rf enclosure chassis. Spurious signals were observed using conventional simple enclosures due to overlap from the first harmonic of the beam signal and cellular devices carried by personnel. The signal then passes through two diplexers. The diplexers are used to properly terminate any out-of-band signals (i.e. baseband and higher order harmonics) and then be properly terminated into a load resistor and not spoil the intended signal measurement.

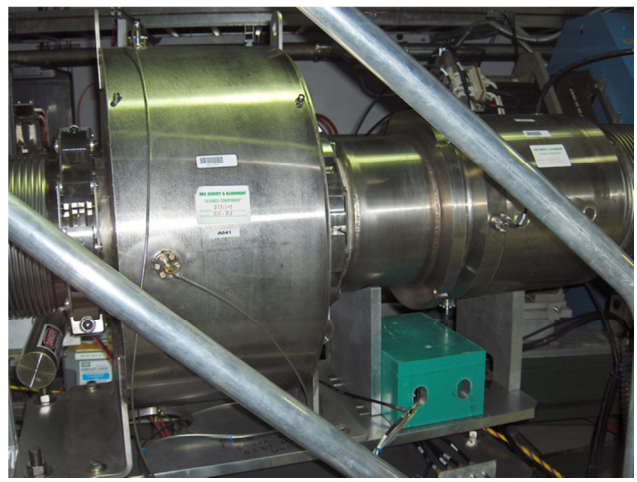

Figure 3: Installed detector and shielded box (in green) with analog combining hybrid, circulator, and single stub tuner.

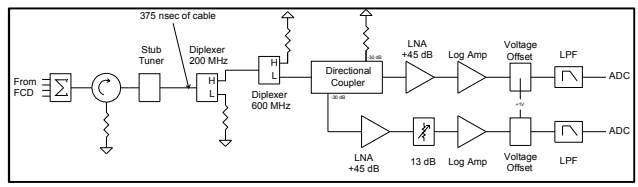

Figure 4: Schematic of cabling and analog electronics.

The next part of the analog signal processing involves taking advantage of the properties of logarithmic amplifiers. As with all conventional amplifiers, logarithmic or otherwise, there exists an operational region where the device was intended to be used. The logarithmic amplifiers that were chosen [1] for this system have a fairly fast rise/fall time of 10 nsec, but also, has an operational region of input power from -70 dBm to 0 dBm. The directional coupler therefore was used to create two data channels from the detector, and then use digital signal processing to recombine the two data channels into a single data channel.

It was desired, therefore to keep the thermal noise floor as low as possible by using low noise amplifiers (LNA). The LNAs are Miteq AMF-2F-00250050-06-10P, which has a noise figure of 0.5 dB and gain of 45 dB. As shown, the logarithmic amplifier follow the LNA. One of the features of the logarithmic amplifier is that its output ranges from about 2.4 volts to 0.5 volts. Since most ADCs (Analog to Digital Convertors) are bipolar, an advantage exists to add a DC offset to the output of the logarithmic amplifier. This permits the full range of the ADC to be utilized. The final component in the analog chassis is an antialiasing low pass filter.

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Digital Electronics

A commercially available platform was chosen to implement the digital front end electronics. It was assembled using a BenNUEY VME Field Programmable Gate Array (FPGA) carrier card from Nallatech [2] with a single BenADDA-V4 DC coupled 14-bit dual channel Analog to Digital Converter (ADC) module operating at a 105 MHz sampling rate. The ADC channels are connected to the analog electronics and are driven by the high and low gain outputs respectively.

The key advantage of designing with commercially available hardware was in the deployment of rapid prototype designs. The initial basic implementation was completed in two weeks. This provided a simple and effective method for verifying the performance of the entire system early in the design cycle. It also let users work with the interface and enabled the collection of feedback immediately.

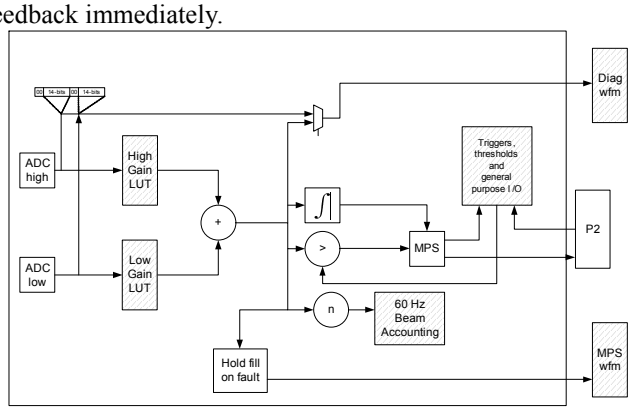

Figure 5: Simplified block diagram of the final digital design implementation.

A pipeline architecture was used to implement the final design. An overview of the digital design is shown in Fig. 5. Each of the 14-bit ADC's possible values are converted to a beam current value by referencing a local look-up table contained within the FPGA. The high and low gain channels are then combined into a single 32-bit value. The contribution from each channel is dependent on the operating range of its associated analog amplifier. The look-up tables are aligned to ensure each channel's impact on the final value is contained within its usable dynamic range. The look-up tables can be bypassed to preserve the raw ADC values if desired. This allows a simple method for calibrating the ADCs and troubleshooting without requiring special firmware builds to be loaded into the FPGA. The technique to calibrate the analog and digital electronics is described in [3] [4] [5].

To prevent incurring loss of critical data due to bandwidth limitations of the VMEbus, the waveforms and beam accounting information is stored in the large banks of local dynamic memory that are connected to the FPGA. It can take several cycles for the VME processor to retrieve these waveforms depending on the system load. Utilizing this memory relaxes the processor's requirement to respond immediately upon receiving an interrupt from the hardware that the waveforms are available.

An additional advantage of utilizing a real-time parallel processing-based design was the integration of a 60Hz shot-to-shot beam accounting scheme and a Beam Dump protection component without compromising the functionality of the original system requirements. The machine protection portion of the design incorporated four independent power measurements that utilized a sliding window technique to calculate the integrated power on the dump for monitoring high losses over a few micro-seconds to low losses that occur over several seconds. The necessary hardware required to interface the machine protection system was included on the rear transition card.

A sample beam measurement of current is shown in Fig. 6.

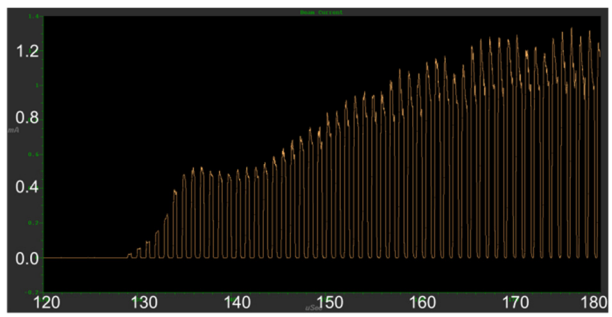

Figure 6: Sample measurement of beam current in the injection dump. Vertical units are in milliamps, horizontal in microseconds. Individual minipulse are clearly visible and the noise floor is a microamp.

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