THE DEVELOPMENT OF TIMING CONTROL SYSTEM FOR RFQ

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Abstract

In order to meet the need of RFQ accelerator, Timing extension hardware based on VME configuration has been developed. In the future, it will be used in the diagnostics system of CSNS. This paper introduces the function of Timing extension hardware, EPICS driver for Timing extension hardware and MEDM operator interface.

BACKGROUND

The core research of intense-proton beam accelerator is mainly concentrated in the field of beam loss control. Based on the intense-beam RFQ accelerator [1] which accelerates proton beam of 46mA pulse current to 35MeV at more than 7% duty factor, a beam line has been built. In order to do beam loss control experiment, many devices have been developed, one of which is Timing extension hardware. Timing extension hardware, as an important device in the running of RFQ accelerator, provides high accuracy and high stability timing trigger signals for the whole system. In the future, it will be used in the CSNS (Chinese Spallation Neutron Source).CSNS adopts EPICS [2] (Experimental Physics and Industrial Control System) as its software environment. So it is necessary to develop EPICS driver [3] for timing extension hardware.

INTRODUCTION OF TIMING EXTENSION HARDWARE

Timing extension hardware uses VME bus of A24 nonpriviledged data access address modifier [6]. It is listed below as fig. 1. Since A24 space is of predicable size 16MB, default window encompassing the full space is always provided. The A24 window is for VME bus address from 0x000000 to 0xffffff, which is usually mapped by VxWorks subroutine sysBusToLocalAdrs to local memory from 0xfa000000 to 0xfaffffff [6].

```
#define VME_AM_STD_USR_DATA     0x39    /* A24, nonpriviledged data access*/
```

Figure 1: Address Modifiers of A24 nonpriviledged data access

Timing extension hardware based on VME configuration is not only consistent with RFQ requirement, it but also avoids the disadvantage of original timing control system, achieving parameters remedy on line. When operators need to remedy parameters of original timing control system, they have to stop the accelerator and calculate the parameters according to the request of experiments, and then use dip switch to change the parameters. The whole process will last almost two hours and affect the efficiency, stability and continuity. Besides, Timing extension hardware based on VME architecture achieves utility of the same hardware to perform different functions by using reconfiguration of the FPGA, which enhances the flexibility of timing extension hardware.

Timing extension hardware has two types of functions [4]. One is providing primary timing signals for RFQ and secondary timing signals which divide frequency of primary timing signals for beam commissioning and RF system. The other is providing delaying or broadening timing signals according to the needs of various devices. In fact, the principle of these two functions is calculating clock signals. For example, primary timing outputs a timing pulse when it calculates the clock signal to the certain amount. Broadening hardware is triggered by timing signal and starts counting program. It will output a TTL pulse with the width of 3us when counting program reaches to the setting value.

Fig. 2 shows timing signals of RFQ, and the timing extension hardware is shown in Fig. 3.

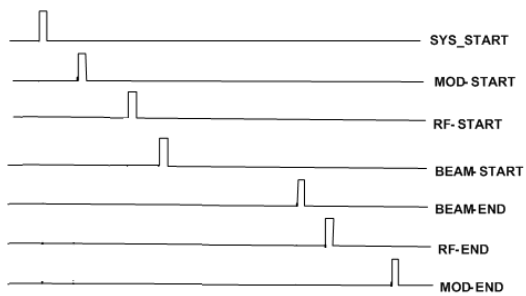

Figure 2: Timing signals of RFQ

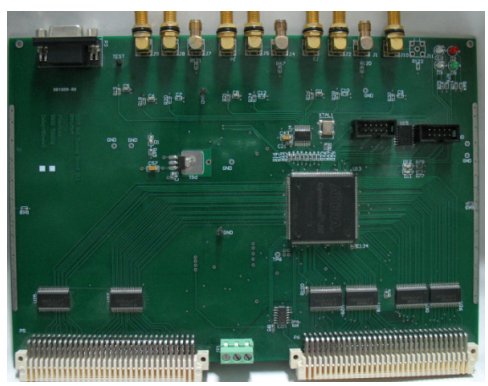

Figure 3: The timing extension hardware

Table 1: Timing control system records access registers step by step

Function	db	dbd	Device support	Driver support
Set primary timing/secondary timing value	Time:$(CARD): $(CHAN): TimingValue:set	device(ao,VME_IO, devAoTime, "Time")	devAoTime{ ….. Write_ao, ……}	Write _Val
Set delay/ broaden value	DelayOrBroaden:$(CARD):$(CHAN):Value :set			
Chose clock signal from internal or external	Time:$(CARD):ClockSignal:set	device(bo,VME_IO, devBoTime, "Time")	devBoTime{ ….. Write_bo ……}	Write _CSR
Chose logic of primary timing/secondary timing	Time:$(CARD): $(CHAN):TimingLogic:set			
Chose logic of delay/broaden	DelayOrBroaden:$(CARD): $(CHAN):Logic :set			
Chose delay or broaden	DelayOrBroaden:$(CARD): $(CHAN):Select :set			
Read timing register of card	Time:$(CARD):CSR:read	device(mbbiDirect,VME_IO, devMbbiDirectTime, "Time")	devMbbiDirectTime { ….. Read_ mbbiDirect ……}	Read_CSR
Read delay/broaden register of card	DelayOr Broaden:$(CARD):CSR:read			
Read actual primary timing/secondary timing value	Time:$(CARD): $(CHAN): TimingValue:read	device(ai,VME_IO, devAiTime, "Time")	devAiTime{ ….. Read_ai, ……}	Read_Val
Read actual delay/ broaden value	DelayOrBroaden:$(CARD): $(CHAN): Value:read			

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EPICS DRIVER FOR TIMING CONTROL SYSTEM

The functions of timing extension hardware achieve by single read or write register [5]. Table 1 is provided to give an outline about how records access registers step by step.

OPERATOR INTERFACE

The operator interface which is under development makes use of MEDM [7] (Motif Editor and Display Manager). With the interface of Timing control system, operator can chose system clock, logic of primary timing and secondary timing, delay or broaden of every channel and logic of every channel. Besides, primary timing, secondary timing, delay or broaden time of each channel can be set through the Interface. Fig. 4 is the operator Interface for Timing control system.

According to the control of interface, timing extension hardware can work normally.

ACKNOWLEDGEMENTS

The authors would like to thank the CSNS Control Group, Accelerator Center, Institute of High Energy Physics, CAS to provide the EPICS platform to work on and technical support.

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ISBN 978-3-95450-122-9

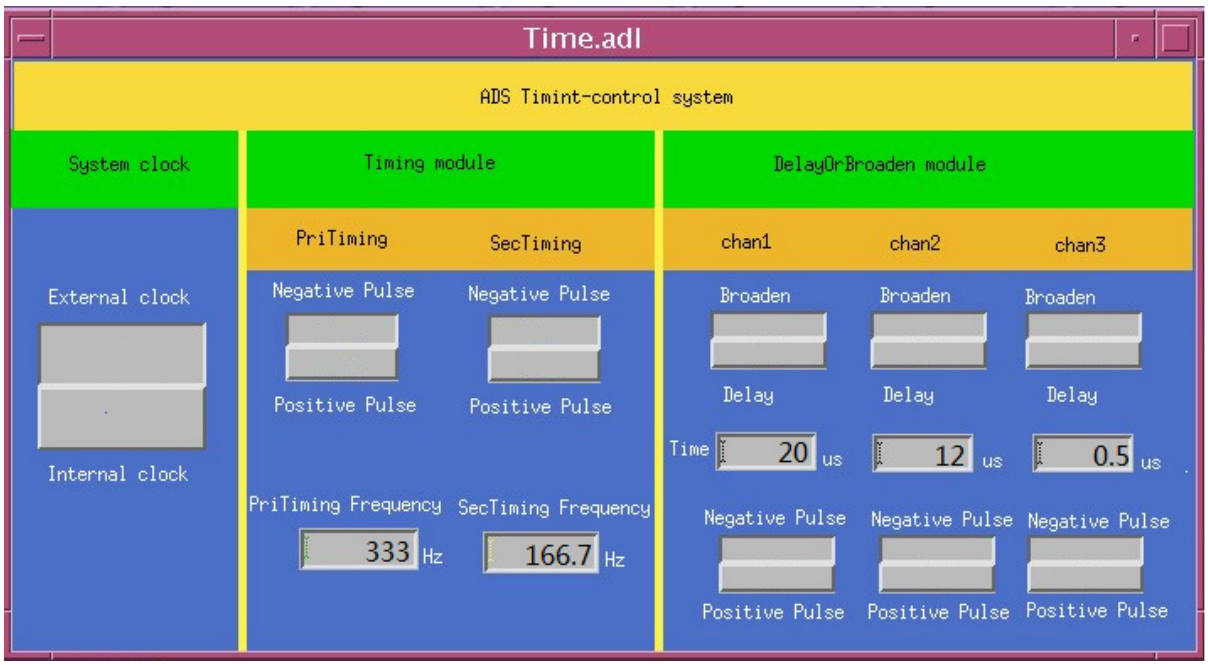

Figure 4: The operator interface