# NEXT GENERATION IGBT SWITCH PLATE DEVELOPMENT FOR THE SNS HIGH VOLTAGE CONVERTER MODULATOR*

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*Abstract*

The RF source High Voltage Converter Modulator (HVCM) systems installed on the Spallation Neutron Source (SNS) have operated well in excess of 200,000 hours, during which time numerous failures have occurred. An improved Insulated Gate Bipolar Transistor (IGBT) switch plate is under development to help mitigate these failures. The new design incorporates two significant improvements. The IGBTs are upgraded to 4500 V, 1200 A, press-pack devices, which increase the voltage margin, facilitate better cooling, and eliminate explosive disassembly of the package in the event of device failure. The upgrade to an advanced IGBT gate drive circuit decreases switching losses and improves fault-condition response. The upgrade design and development status will be presented.

## BACKGROUND

### *SNS HVCM*

The topology of the SNS HVCM is shown in Fig. 1 [1]. There have been numerous upgrades to the original design which have greatly improved the reliability [2]. However, to further improve reliability and to provide voltage regulation of the output pulses at full average power, additional improvements are required. Work is underway at SLAC to develop a new H-bridge switchplate, a part of the modulator which has caused many of the modulator failures. The new design incorporates higher power IGBTs, improved fault current control and an advanced fault-detecting IGBT gate drive.

### *Press-Pack IGBTs*

The press-pack IGBTs selected to replace the flat-pack devices used in the present switchplate, offer several advantages. First, the new IGBTs will have an increased voltage margin (3.3 kV vs 4.5 kV). Second, these IGBTs can be cooled on two sides, which will aid in heat removal. Third, press-pack IGBTs have been shown to have increased reliability in pulsed-power applications [3]. Lastly, unlike the flat-pack devices, the press-pack will not explosively disassemble in the event of an IGBT failure.

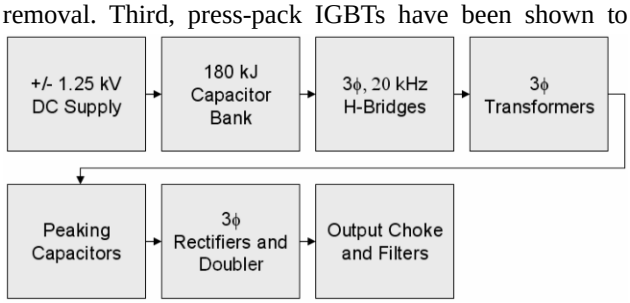


Figure 1: Simplified diagram of the SNS HVCM.

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## DESIGN

### *Press-Pack Switchplate*

A photograph of the current switchplate is shown in Fig. 2 and the simplified circuit schematic is shown in Fig. 3. The flat-pack IGBTs utilized in the present switchplate design have an advantage in being relatively straightforward to implement mechanically. The anti-parallel diode is in the same package as the IGBT, further simplifying the assembly.

A drawing of the SLAC press-pack switchplate is shown in Fig. 4. Compared to the current design, the press-pack based design has several key advantages in addition to those mentioned above:

- The bottom heat-sink is at the same potential as the

Figure 2: Photograph of one SNS H-bridge card on the SLAC single phase test stand.

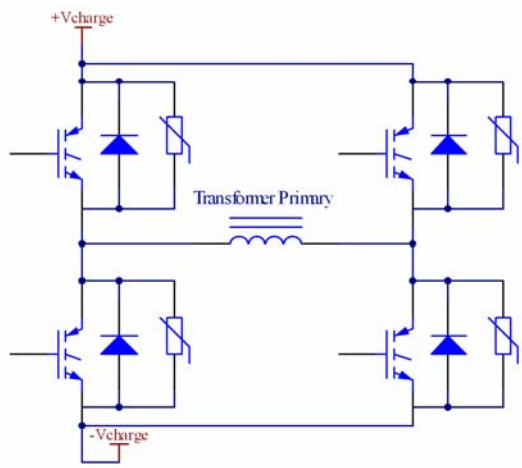


Figure 3: Simplified circuit model of the SNS H-bridge. In the original design, the IGBTs and diodes are in one, flat-pack package and there is no parallel MOV.

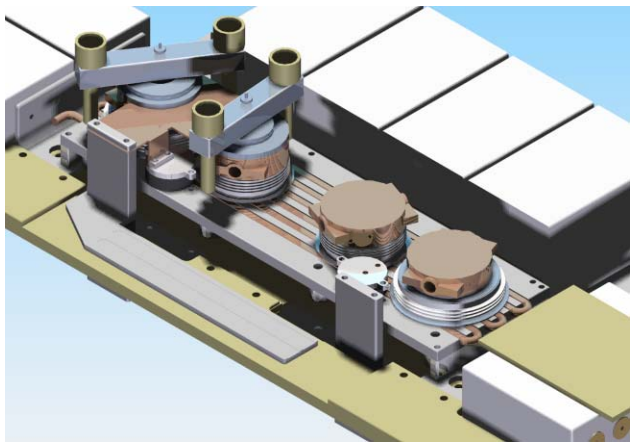

Figure 4: Rendering of the designed press-pack switchplate. Some parts are omitted for clarity.

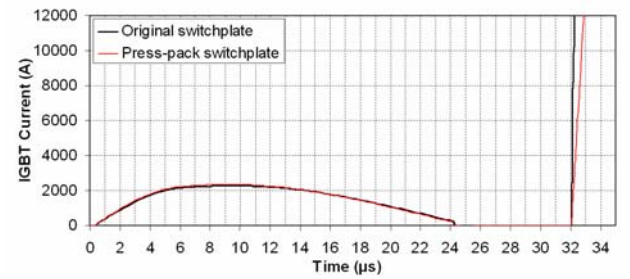


Figure 5: Simulated IGBT current during a shoot-through fault. The opposing IGBT is triggered at ~32 µs.

nearby bus, unlike the current design, which relies on the liberal use of dielectric insulating sheets between the heat sink and bus, which suffer coronic degradation over time.

- The diode will be packaged separately from the IGBT. Diode failure cannot be differentiated from IGBT failure in the flat-pack and a fault in either results in the loss of the entire package.
- A MOV is incorporated to clamp voltage transients.
- The IGBT drivers will be mounted over the side snubber capacitors to improve accessibility.

Finite Element (FE) simulations were used to estimate the inductance of the normal conduction path and the shoot-through fault path (both IGBTs on one side of the H-bridge in conduction) of both designs, as shown in Tab. 1. The inductance of the press-pack plate's normal conduction path is slightly higher, which will increase the transient voltage during switching. This is offset by the increased IGBT breakdown voltage and the MOV that is co-located with the switch and diode. Conversely, the shoot-through inductance of the new design is about twice as large as the original. This increase in inductance will lower the di/dt during a shoot-through fault, decreasing the fault current and increasing the probability that the IGBT can be commutated after a fault is detected.

The FE program generated a matrix of inductance values for each design. These details were added to the model of the SNS modulator that is used for circuit simulation. One simulation result is shown in Fig. 5. The period from zero to ~24 µs on the plot is the normal conduction current through the IGBT. At ~32 µs, a shoot-through condition was induced. The calculated di/dt for the press-pack switchplate is 10 kA/µs, as compared to 45 kA/µs for the original switchplate. For the estimated fault detection and IGBT commutation time of 1 µs, this corresponds to an estimated decrease in commutation current from 45 to 10 kA. Future experiments will be conducted to confirm whether or not this value is low enough to allow detected faults to be suppressed.

Table 1: Values from FE simulation of the total inductance for the shoot-through and normal conducting paths for one leg of the H-bridge. The defined paths are from the +HV to -HV snubber capacitors and ignore the inductance of the transformer, snubber capacitors, and internal IGBT connections.

| Design | Total Path Inductance during Shoot-through | Total Path Inductance during Normal Conduction |
|---|---|---|
| **Original** | 77 nH | 123 nH |
| **Press-Pack** | 153 nH | 171 nH |

### *Gate Driver*

One of the primary motivations for the advanced gate drive development is to improve fault suppression. The existing gate driver has a "fault out" signal which indicates either a power dip or a tripped klixon. The new gate driver will add spurious trigger, excess di/dt, and excess $V_{ce,sat}$ detection. The spurious trigger fault is caused whenever a trigger signal is sent to two IGBTs in a shoot-through path. The gate drivers send a "handshake" enable signal to each other during operation.

The excess di/dt is indicative of a fault that has lowered the impedance of the current path, e.g. a shoot-thru fault. It is detected by a differential voltage measurement between the emitter and a nearby point. The inductance between the two points will induce a voltage proportional to the IGBT di/dt. If the measured voltage is above a preset level, a fault will be indicated.

A second check for excess current through the IGBT is made by monitoring $V_{ce}$, which will increase dramatically if the IGBT current exceeds the saturation value. The new gate driver incorporates a commercial gate driver chip with integral $V_{ce,sat}$ detection. The occurrence of any of the monitored faults will be indicated by a latching LED indicator, and if so configured, terminate modulator triggering.

## EXPERIMENT

### *Single Phase Test Stand*

A test stand was developed at SLAC to simulate the switching conditions of a single SNS H-bridge switchplate. It was designed to match the switching voltage as well as the peak and commutation currents through the IGBTs. An example waveform is shown in

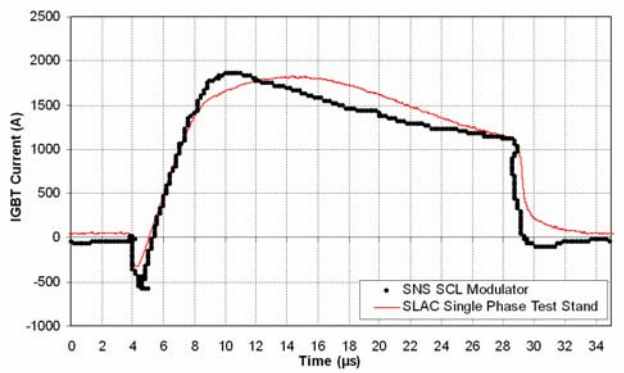


Figure 6: Comparison of the measured IGBT current in a SNS SCL modulator to the SLAC single phase test stand.

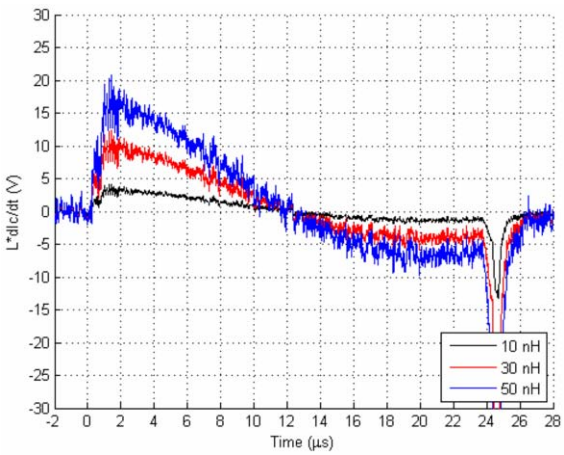


Figure 7: Calculated L*dI/di using measured IGBT collector current values and three estimated inductance values.

Fig. 6. This test stand provides a convenient platform to evaluate the impact of switchplate modifications. Additionally, fault conditions can be simulated in a controlled environment.

The test stand has been used to evaluate the efficacy of using a di/dt measurement to detect the onset of a current fault condition, e.g. shoot-thru. Using the test stand, the IGBT collector current was measured and di/dt was calculated. Fig. 7 illustrates the expected diagnostic response for three different inductance values. The preliminary estimate of the diagnostic's differential voltage measurement path inductance is 30nH. Therefore, the normal signal, ~10V maximum, is large enough for good signal-to-noise, but significantly less than expected under fault conditions, 30 V for 1 kA/µs. Future, measurements using the single phase test stand will confirm nominal and fault condition behavior.

### *Single Device Test Stand*

The SLAC 2-pack test stand was modified to provide a platform to evaluate candidate IGBTs and gate drivers for the switchplate upgrade. The IGBT emitter is ground referenced in the test stand to simplify the measurement of gate and collector voltages coincident with emitter current under switching, normal conduction, and fault conditions. The test stand inductively couples the IGBT under test to a 1 ohm load. A photograph of part of the test stand with a press-pack IGBT is shown in Fig. 8.

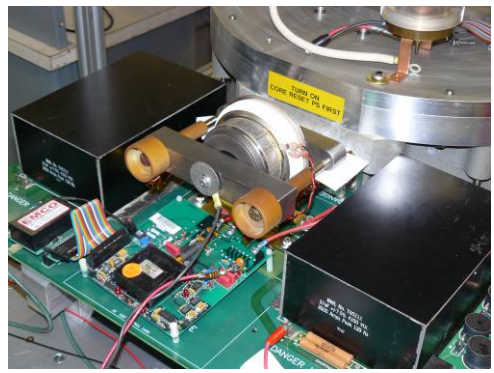

Figure 8: Photograph of the single device test stand with a press-pack IGBT.

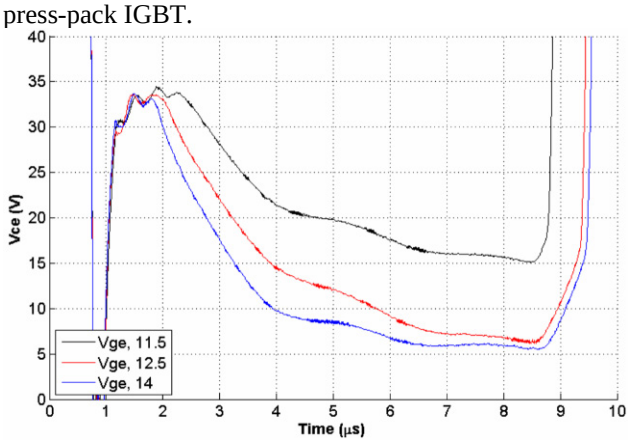


Figure 9: Vce values measured on the single device test stand for various values of Vge.

One preliminary test result is shown in Fig. 9. The $V_{ce}$ voltage was measured for a range of applied gate voltages. The gate voltage should be low to minimize the IGBT saturation current, for protection during a fault condition. However, low gate voltage increases the IGBT losses during normal operation. The test stand aids in identifying the appropriate levels.

## SUMMARY

An advanced switchplate for the SNS HVCM, incorporating press-pack IGBTs and improved gate drivers, is under development at SLAC. Test stands to evaluate the improved switchplate and key components under nominal and fault conditions have been developed and commissioned at SLAC. The switchplate design has been finalized and commissioning is currently underway. Future work will include further testing of these devices under nominal and fault conditions.

## REFERENCES

[1] W.A. Reass, *et al.*, IEEE Trans. Plasma Sci. 33 (2005) 1210.
[2] D.E. Anderson, *et al.*, Power Modulator Symposium 2006, p. 427.
[3] F. Wakeman, *et al.*, Pulsed Power Plasma Science Conference 2001, p. 1051.