PROGRESS IN DEVELOPMENT OF NEW LLRF CONTROL SYSTEM FOR SUPERKEKB

T. Kobayashi#, K. Akai, K. Ebihara, J. Odagiri, A. Kabe, K. Nakanishi, M. Nishiwaki,
KEK, Tsukuba, Ibaraki, Japan
H. Deguchi, K. Harumatsu, K. Hayashi, T. Iwaki, J. Mizuno, J. Nishio, M. Ryoshi,
Mitsubishi Electric TOKKI System Corporation, Amagasaki, Hyogo, Japan

Abstract

For the SuperKEKB project, a new LLRF control system has been developed to realize high accuracy and flexibility. High power test of the prototype was performed with the ARES cavity. The feedback control stability with klystron driving agreed well with the low-level evaluation and it is enough good. Auto tuner control also worked successfully. The start-up sequencer program for the cavity operation and auto-aging program also worked very well.

The temperature characteristics of the system depend largely on band-pass filters (BPF). We tried to tune the BPF to reduce the temperature coefficient. Consequently the temperature dependence was improved to satisfy the required stability.

INTRODUCTION

SuperKEKB is a new upgrade project to make the luminosity of the KEKB accelerator 40 times higher [1]. For high-current and low-emittance beam acceleration without instability, accurate and flexible RF control are very significant. Therefore, a new digital low level RF (LLRF) control system was developed for SuperKEKB [2]. It is an FPGA-based digital RF feedback control system using 16-bit ADC's, which works on the µTCA platform [3]. The FPGA boards control accelerating cavity fields and cavity tuning, and the EPICS-IOC is embedded in each of them [4]. It is planned that the existing LLRF systems used for KEKB operation will be replaced by new ones, step by step.

Evaluation of a prototype of the new LLRF system, which is called α-version, was performed in low-level operation and the results were reported in Ref. [2]. Furthermore second trial model, which is called β-version, was developed and evaluated. The new progress since the last IPAC is reported in this paper. For the detail of the KEKB RF system and the new LLRF system, refer to [2][5][6].

The accelerating frequency is about 508.9 MHz (CW operation). Required stability in accelerating fields is ±1% in amplitude and ±1° in phase. For the LLRF system, our target value of the stability is less than ±0.3% in amplitude and ±0.3° in phase.

UPGRADE OF TRIAL MODEL

The β-version (the second trial model) has been produced and its high power test was performed in March 2013. Main difference between the α and β-version is mechanism of discriminators for RF inter-lock (I/L) system. As shown in Fig. 1,analogue comparators are used to detect abnormal RF level in the α-version. Threshold of the comparator is given from PLC-DAC module. On the other hand, in the β-version, digital sampling method is adopted. RF-detector outputs are A/D-converted on FPGA at 10MHz. 14-bit ADC's are used. In this way, waveforms at I/L event can be obtained via EPICS like an oscilloscope. External trigger is also available. Arc discharge in the high power structure is also detected by similar way. The flashlight of discharge at cavity input coupler, klystron window and so on is transferred through optical fiber and the photo-detected and then A/D-converted by the FPGA. These I/L detections worked successfully in the high power test.

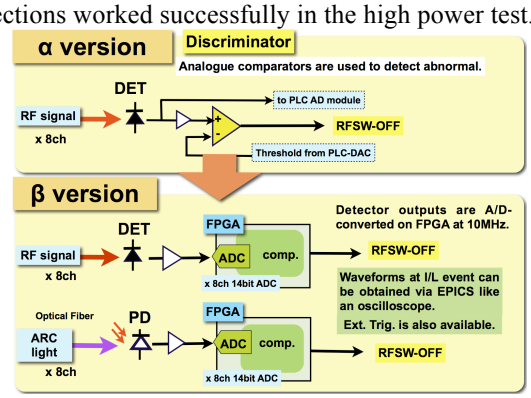

Figure 1: Main difference between the α and β-version.

THERMAL STABILITY

Acceptable temperature coefficients of the amplitude and phase are within 0.1%/deg.C and within 0.1 deg./deg.C, respectively. However, the measurement results of the prototype did not satisfy the requirements as reported in the last IPAC [2]. And then it was found that the main factor of the temperature dependency is band-pass filter (BPF) property in the down-converter. BPF's are located before the mixer to convert into IF signals. 10 BPF's are used in the down-converter unit.

For improvement of the thermal stability, at first, we changed the structure type of BPF for the β-version. In the α-version, lumped constant circuit structure was used. In the β-versin, cavity type BPF was chosen instead, because cavity type has better regularity of characteristics between manufacture lots. Furthermore, additionally fine-tuning was applied to all BPF's for the thermal stability.

Figure 2 shows sample results of the fine-tuning for one BPF. After the tuning, the phase property was improved to be quite small. The amplitude property is already enough small before the tuning. But the phase tuning also

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affects the amplitude tuning. So amplitude property was slightly degraded. The amplitude and phase property is not independent, so iteration work is needed for the both adjustment.

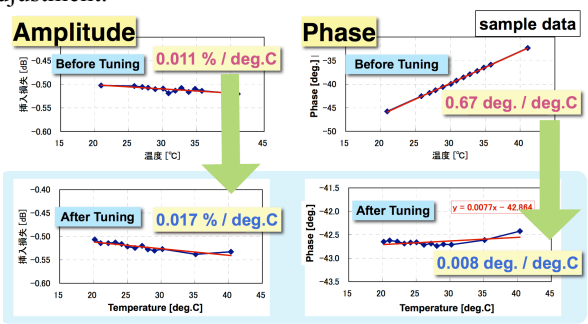

Figure 2: Fine-tuning of BPF temperature characteristics to improve thermal stability.

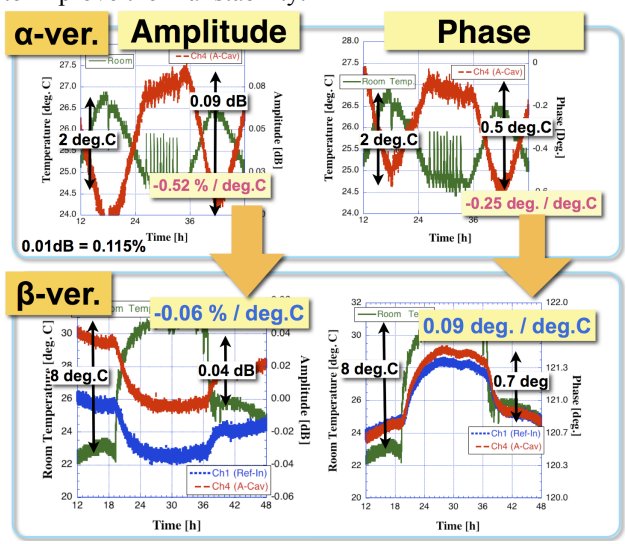

Figure 3: Measured thermal stability of the overall LLRF system. Trend graph for 2 days.

Figure 3 shows measured results of thermal stability of the overall LLRF system in comparison between the α and β-version. In the figure, trend graph of amplitude and phase are plotted for 2 days. The green line indicates the room temperature. The red line and blue line corresponds to cavity-pickup channel (ch4) and the reference channel (ch1), respectively. The amplitude and phase temperature coefficients of the β-version are 0.06%/deg.C and 0.09 deg./deg.C, respectively. These values could satisfy the requirements. Furthermore, if the cavity-pickup phase is calibrated by the reference channel constantly (that is, Ch4 is referred to Ch1), then 0.02 deg./deg.C of phase stability can be expected from the plot.

HIGH POWER TEST

High Power Operation

High power test operation of the new LLRF system (both of the α and β-version) was performed by using practical ARES cavity. (See Ref. [5] for the ARES cavity.) Figure 4 shows a strip-chart at the cavity start-up sequence for about 30-minute duration. The red line indicates the klystron output power, and the faint red is cavity level. The cavity power was raised up slowly by sequencer program with cavity FB control acting. The blue and cyan lines are tuner positions of the accelerating cavity and the storage cavity, respectively. Auto tuning controller was working and then the both tuners were moving successfully to make cavity resonance.

Without the FB control, the klystron phase fluctuates by 3~4 degrees due to DC voltage variation.

The CSS-BOY [7] was adopted for an user interface of our system.

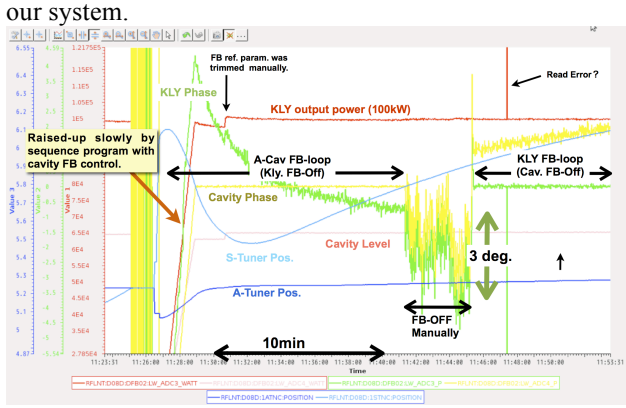

Figure 4: Strip chart of cavity power rising-up.

FB Control Stability

FB control stability was also evaluated by "out-of-loop" measurement in the high-power operation. The cavity pickup signal was divided for the monitor, and the amplitude and phase was measured by using an RF detector and a mixer, respectively. Figure 5 shows the results of the FB control stability at 100-kW klystron output power. These are oscilloscope acquisition data of 4-ms time duration. Small beat can be found in the phase, but it is negligible small for our specification. As shown, very good stability was obtained. The stability in r.m.s is 0.02 % in amplitude and 0.02 degree in phase. These stabilities did not depend on FB gains.

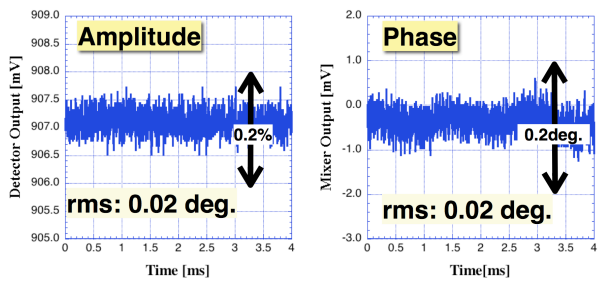

Figure 5: Short-term amplitude and phase stability under feedback control evaluated by out-of-loop measurement.

Frequency Domain Behavior

Figure 6 shows an example of Bode plots of cavity response to disturbance inside the closed loop such as DAC output noise, etc. Modulation (base band) amplitude and phase response are plotted for various FB gains (P: proportional gain, I: integral gain). The solid line indicates the calculation, and the circle marks are measured results, which agree well with the calculation.

From these results, the noises of 10~30 kHz can be only suppressed to be -10 dB. The beam effects of synchrotron oscillation (~1 kHz) will be reduced to be -20 dB. The gap transient effect (~100kHz) of the revolution beam will simply conform to the cavity response. More details of beam interaction will be discussed in next report.

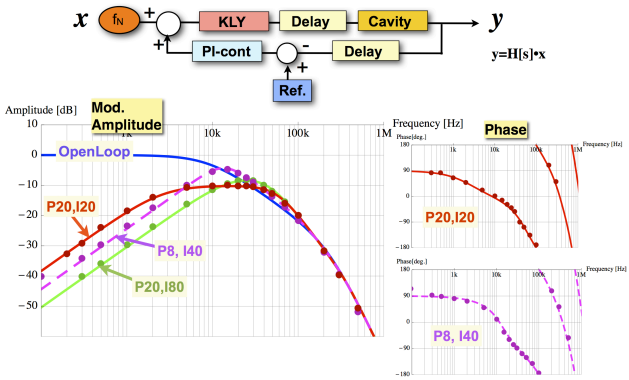

Figure 6: Bode plots of cavity response to disturbance inside the closed loop (e.g. DAC output noise).

KLYSTRON PHASE LOCK LOOP

For efficiency optimization, the anode voltage is controlled depending on klystron input power to reduce the collector loss as shown in Fig. 7. In this control, upper limit and lower limit are applied. As the shown result in the figure, the 80-degrees phase shift of klystron output was observed due to the anode voltage control in the high power test. This phase change of 80 degrees is unexpectedly large. In the I/Q-FB technique, acceptable phase change in the closed loop is restricted to only within +/-90 degrees in principle. According to our calculation and simulation analysis, it will be limited to within +/-60 degrees in our operation condition. The high power test result was consistent with the analysis.

Therefore, klystron phase lock loop (KLY-PLL) is necessary as a next step. Figure 8 shows the illustration of implementation of klystron phase lock loop. It is implemented digitally in the FPGA with FB-control. For the KLY-PLL, additional phase rotation function is inserted for I/Q modulation. The klystron phase is detected and calibrated by output phase as the reference. “θ” will be accumulated by a increment constant to cancel the klystron phase shift, then the phase rotation parameters (cosθ and sinθ) are given dynamically. The “cos” and ”sin” values are given by reference table in 2-deg. step and interpolated by 1st-order approximation. The required loop band is supposed to be about 1kHz, because the anode voltage response is about 1~10Hz.

SUMMARY

Prototype of a digital LLRF system for SuperKEKB was developed and high power test was performed. FB control and auto tuning control worked successfully, and very good FB stability of 0.02% in amplitude and 0.02 deg. in phase was obtained in “out of the loop” measurement.

Large klystron phase shift of 80 degrees due to the anode voltage control for efficiency optimization, which depends on input power, was observed. Because acceptable phase shift in the closed loop is within +/-60 degrees in our system, KLY-PLL function should be implemented into the FPGA as a next step.

Temperature dependency of the system were reduced by BPF fine-tuning, and then required thermal stability (0.06%/deg.C in amplitude and 0.02 deg./deg.C in phase) was satisfied.

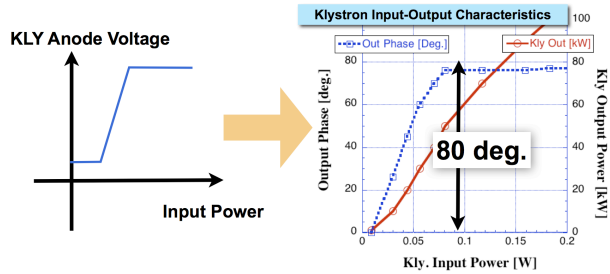

Figure 7: Klystron phase shift due to the anode voltage control.

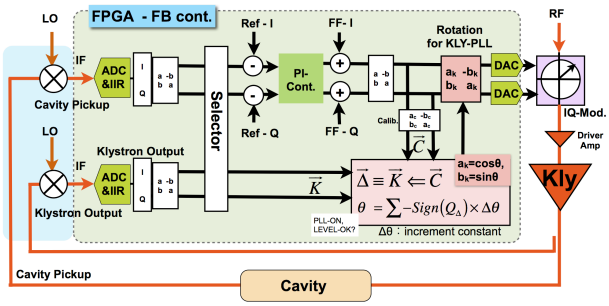

Figure 8: Design of klystron phase lock loop, which will be implemented in the FPGA.

REFERENCES

[1] K. Akai, et al., "Design Progress and Construction Status of SuperKEKB", Proc. of IPAC12, pp. 1822-1824 (2012); http://accelconf.web.cern.ch/AccelConf/IPAC2012/papers/tuppr006.pdf

[2] T. Kobayashi, et al., "Prototype Performance of Digital LLRF Control System for SuperKEKB", Proc. of IPAC12, pp. 3470-3472 (2012); http://accelconf.web.cern.ch/AccelConf/IPAC2012/papers/thppc079.pdf

[3] M. Ryoshi et al., "LLRF Board in Micro-TCA Platform", Proc. of the 7th Annual Meeting of Particle Accelerator Society of Japan, p. 668 (2010); http://www.pasj.jp/web_publish/pasj7/proceedings/P_4PM/P_EH_4PM/WEPS109.pdf

[4] J. Odagiri at al., "Fully Embedded EPICS-Based Control of Low Level RF System for SuperKEKB", Proc. of IPAC'10, p. 2686 (2010); http://accelconf.web.cern.ch/AccelConf/IPAC10/papers/wepeb003.pdf

[5] T. Kageyama, et al., "The ARES cavity for KEKB", Proc. of APAC98, pp. 773-775 (1998)

[6] K. Akai, et al., "RF systems for the KEK B-Factory", Nuclear Instruments and Methods in Physics Research A 499 (2003) 45–65

[7] http://ics-web.sns.ornl.gov/css/index.html

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