PERFORMANCE ENHANCEMENTS FOR THE TRANSVERSE FEEDBACK SYSTEM AT THE ADVANCED PHOTON SOURCE*

N. DiMonte#, R. Farnsworth, A. Scaminaci
Argonne National Laboratory, Argonne, IL 60439, U.S.A.

Abstract

With the success of the transverse feedback system at the Advanced Photon Source (APS), an upgrade to this system is being developed. The current system is operating at a third of the storage ring bunch capacity, or 324 of the available 1296 bunches. This upgrade will allow the sampling of all 1296 bunches and make corrections for all selected bunches in a single storage ring turn. To facilitate this upgrade, a new analog I/O board capable of 352-MHz operation is being developed along with a P0 bunch cleaning circuit. The clock cleaning circuit is also needed for the high speed analog output circuit, which is transmitted about 200 m to a separate DAC unit in real time. This remote DAC will have its transceiver data rate triple from 2.3 Gb to about 7 Gb on a fiber optic link. This paper will discuss some of the challenges in reducing the clock jitter from the system P0 bunch clock along with the necessary FPGA hardware upgrades and algorithm changes, all of which are required for the success of this upgrade.

INTRODUCTION

While remarkably stable, the APS experiences beam instabilities in both the transverse and longitudinal planes [1]. The P0 feedback system, in its initial version, corrects these instabilities in a bunch pattern that has up to 24 bunches. This is accomplished by using an FPGA system based on the Altera Stratix II GX FPGA-based DSP development board [2] coupled with a Coldfire CPU. The Coldfire CPU uses EPICS [3] with RTEMS [4] for all the remote monitoring and control. This paper discusses hardware performance upgrades that are in progress.

SYSTEM DESCRIPTION

The system consists of a pick-up stripline, a front-end signal-processing unit, an Altera Stratix II GX DSP processor unit, drive amplifiers, and a driver stripline. This system has been described in detail [5]. Figure 1 shows a block diagram of the current system without the remote DAC hardware. At the core of the FPGA processor are the 864 32-tap FIR filters running at 117.3 MHz. The algorithm used for the filter is based on the least square fitting method to determine filter coefficients [6]. The pickup and drive striplines are located in different locations of the storage ring, which is a major issue for the Y-channel since the distance between pickup and drive is seven sectors, or about 188 m, apart. A remote DAC linked to the main transverse feedback system via high-speed fiber optic cable utilizing a real-time data transfer protocol. Figure 2 shows the addition of the transceiver in the main transverse feedback chassis used to connect the remote DAC chassis.

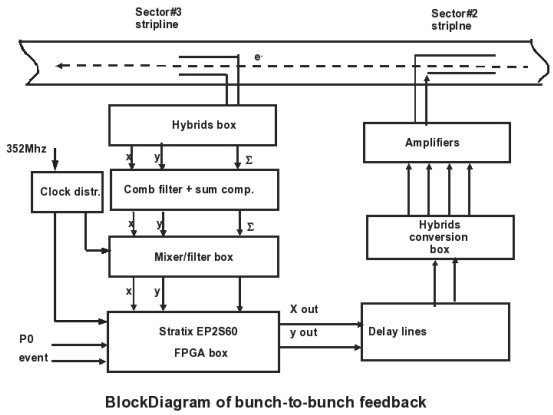

Figure 1: Block diagram of the feedback system.

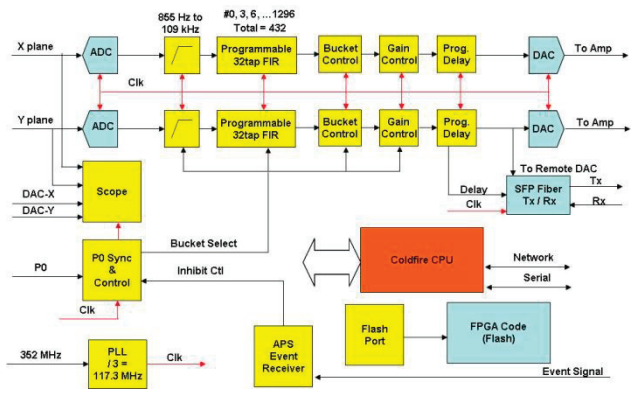

Figure 2: FPGA block diagram of the P0 feedback.

SYSTEM LIMITATIONS

The current FPGA system described above has been very successful for the Advanced Photon Source as it has been detailed in a previous paper [7]. This system is limited to 324 or 432 buckets depending on the operating frequency of 88 or 117.3 MHz that's configured for a particular bunch pattern. With the proven success of this system an opportunity to expand the transverse feedback system to encompass all 1296 buckets has been proposed. This would require the system to operate at the full storage ring frequency of 352 MHz. At 432 buckets the system is operating at 117.3 MHz, which is a limitation of the ADC/DAC interface to the FPGA. The current ADC

*Work supported by U.S. Department of Energy, Office of Science, under Contract No. DE-AC02-06CH11357.
#Email: npd@aps.anl.gov

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ISBN 978-3-95450-115-1

has a maximum sample rate of 125 MHz while the DAC can perform at 150 MHz. The current FPGA (Stratix II GX) is limited to a maximum transceiver rate of 6.376 Gbps of which 2.3 Gbps is needed to transport data to the remote DAC at system clock rate of 117 MHz. To transport data to the remote DAC with a system clock rate at 352 MHz, the transceiver needs to triple its transmission rate from 2.3 Gbps to 6.9 Gbps, which is beyond the Stratix II GX chip's capabilities. The current ADC and DACs are also not sufficient for 352-MHz operation. One solution is to have several ADCs and DACs in parallel to achieve 352-MHz operation. While standard methods can be used to multiplex the ADC front end, it becomes very complicated to mux several DACs to generate a 352-MHz analog control signal. This option also requires more board space, a minimum of three ADCs and three DACs, and would require a larger power supply. For the transverse feedback system with two channels, a total of six ADCs and six DACs would be needed. A simpler option is to have a single ADC/DAC pair per channel, which saves on space and power consumption.

One of the biggest hurdles that this upgrade overcame was the jitter in the 352-MHz RF clock and the jitter in the P0 timing trigger. This has not been an issue at the Advanced Photon Source in the past because the existing digitizing systems were running at sub-harmonics of the clock (e.g., 88 MHz, 117.3 MHz, 176 MHz), which precluded the possibility of sampling the full 1296 buckets in the storage ring. This jitter would cause the transverse feedback system to skip to an adjacent bucket with undesirable results. This issue had the potential to put this enhancement on hold.

HARDWARE UPGRADES

These limitations were addressed by closely examining the current transverse feedback system that is using an Altera Stratix II GX PCIe development kit. This kit contains built-in SFP cages to allow optical transceivers to be plugged into it. It also has two HSMC (High Speed Mezzanine Card) ports, one which is populated with a Coldfire CPU daughter board and the other with a two-channel ADC/DAC board. The upgraded Altera development board was required to have all these ports in order to be a drop-in replacement, but the closest drop-in that Altera provided was a Stratix IV GX Development Kit [8], which has two HSMC and PCIe connectors but no SFP cages. It was necessary to move to the Stratix IV GX chip for the higher clock rates needed for this enhancement, and the number of FIR filters tripled as can be seen in Table 1. The Stratix II GX could only accept a 500-MHz clock input on an I/O pin and a 500-MHz (max) internal clock speed. Compiling the Stratix II GX for 352-MHz operation failed to meet internal timing specs because there was not enough ceiling between 352 MHz and 500 MHz. With the Stratix IV GX chip, the clock ceiling in the FPGA fabric is high enough to not violate any timing requirements. Since the Stratix IV GX transceiver logic cores are completely configurable, a PCI card was developed with SFP cages that could plug into the Altera development kit's PCIe connector. Testing will need to be performed with this configuration since the PCIe specification is only good for 5.0 Gbps (Gen2), but this design will push that to just under 7.0 Gbps through a card edge connector. The PCIe to SFP+ adapter board adds about 25 mm to the signal trace but this signal is a point-to-point connection, so signal degradation will be at a minimum. This adapter card has been tested at the current 2.3-Gbps transfer rate with no data loss. Using new SFP+ transceiver capable of 8.5 Gbps will require a performance test with the Finisar transceiver [9] capable of 8.5 Gbps with bi-directional data links to be tested first. A transceiver produced by Avago [10] is also being considered for testing.

Table 1: Possible Bucket Modes

88 MHz	Samples only 324 buckets 1) 324 mode 2) Hybrid mode 3) 648 FIR filters needed
117.3 MHz	Samples only 432 buckets 1) 24 singlet mode 2) Hybrid mode 3) 864 FIR filters needed
352 MHz	Samples all 1296 buckets 1) Any bucket configuration 2) 2392 FIR filters needed

The existing data conversion board (DCB) [11] has a HSMC connector that connects to the main Altera development board. This DCB has two ADC channels and two DAC channels. The maximum sample rate for the ADC is 125 MHz at 12bits and the DAC maximum sample rate is 150 MHz at 14 bits. For this upgrade this system needs to operate at 352 MHz, which these devices will not be able to accommodate. The cost of having a new board developed to our specifications by a commercial vendor is prohibitive. It was concluded that a custom board would not only meet the needs of the transverse feedback system but would serve other FPGA designs applications being developed at the APS. For the ADCs, two Texas Instruments ADS5474s were selected; this is a 14-bit device capable of 400 MSPS sample rate. A 16-bit dual DAC by Analog Devices with a part number of AD9783 has a sample rate of 500 MSPS.

A major design consideration in developing the new DCB is how to deal with an ADC`s high sensitivity to jitter of the sampling clock when digitizing analog signals at high sampling rates. Long-term testing of the LLRF clock signals at APS have shown that the existing clock contains a number of spurs in the -75 to -95 dbm range and a prominent spur at 1 MHz, which appears to be a product of the 10-MHz reference synthesizer. For the vast majority of operations within APS, the LLRF clock is sufficiently clean, but for direct sampling at 352 MHz, the existing clock must be cleaned further. The new DCB will provide two 14-bit 400 MSPS Analog Devices ADCs and

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one dual 16-bit 500 MSPS DAC, thus providing two independent ADC and DAC signal channels. In order to maintain the ~12-bit ENOB of the ADC at 352 MSPS, the LLRF sample clock must have the lowest jitter possible. To that end, a high-speed RF comparator, a jitter cleaner chip, and a clock distribution chip are included on the DCB. The jitter cleaner chip provides four independent LVDS outputs at frequencies up to 704 MHz with each output capable of incrementing and decrementing its phase offset from the input reference clock in 20-ps steps. Each clock output's phase steps are completely independent of the other three outputs. The clock distribution will be configured so that each of the two ADCs will have its own clock, the dual DAC will have its own clock, and the FPGA will get the remaining clock. Each clock will have its own individual phase control. The FPGA will forward its 352-MHz clock via an LVDS differential output pair to an external coupler with a single-ended output for use elsewhere. Additional clock outputs may be added in the future.

This new DCB will also provide the capability of functioning as a standalone IOC (input/output/controller) running EPICS under a modified version of Xilinx`s micro-C embedded Linux, or it can run application-specific software with or without an OS and/or EPICS. All software functionality is provided by a 32-bit Microblaze soft processor embedded in the FPGA fabric, resulting in the DCB being a true system-on-a-chip solution. Linux boots directly from on-board flash, and EPICS may load locally or remotely via an NFS mount over Ethernet. For applications such as the transverse feedback daughter card, the DCB will be a slave to the IOC running on the Stratix IV board, so there is no need for an IOC to run on the DCB itself. Other applications may benefit from using the DCB as a standalone IOC.

FUTURE PLANS

The existing transverse feedback system has a great potential for being a bunch cleaner for every bucket in the APS storage ring; however, since it can only monitor every third bunch, it appears that this system cannot be used in all bunch modes. We are now moving forward to an enhanced version of the transverse feedback system that will monitor and control all 1296 buckets, but this will require us to design and build our own board based on our experience with the Altera development boards.

Much work has gone into the clock cleaning circuit for the 352-MHz main clock and the P0 trigger cleaning circuit, which has been successful enough to move forward with the enhancement. A delivery estimate for the DCB is in the time frame of summer 2012. This will include a clock/trigger cleaning circuit along with the ADCs and DAC circuits all packaged in a daughter board that will plug into the Altera Stratix IV GX development kit. Once the 8.5-Gbps transceivers are delivered, a data integrity test will begin by doubling the fiber optic cable from its current configuration. Part of the enhancement is to relocate the remote DAC unit from sector 35 to sector 30, roughly doubling the length of the fiber. Sector 30 is the furthest this unit can move and still be effective within one beam revolution. The FPGA algorithm process time with the added fiber delay is the main cause for the sector limitation.

CONCLUSION

The transverse feedback system has proven to be very flexible in that it was easy to adapt when the need arose, e.g., increasing the number of buckets and adding a remote DAC function. This system has proven that it can stabilize 432 bunches in both the horizontal and vertical planes at the APS and possibly function as a bunch cleaner.

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ISBN 978-3-95450-115-1