Development of a Front-end Data Acquisition System with a Camera Link FMC for High-bandwidth X-ray Imaging Detectors

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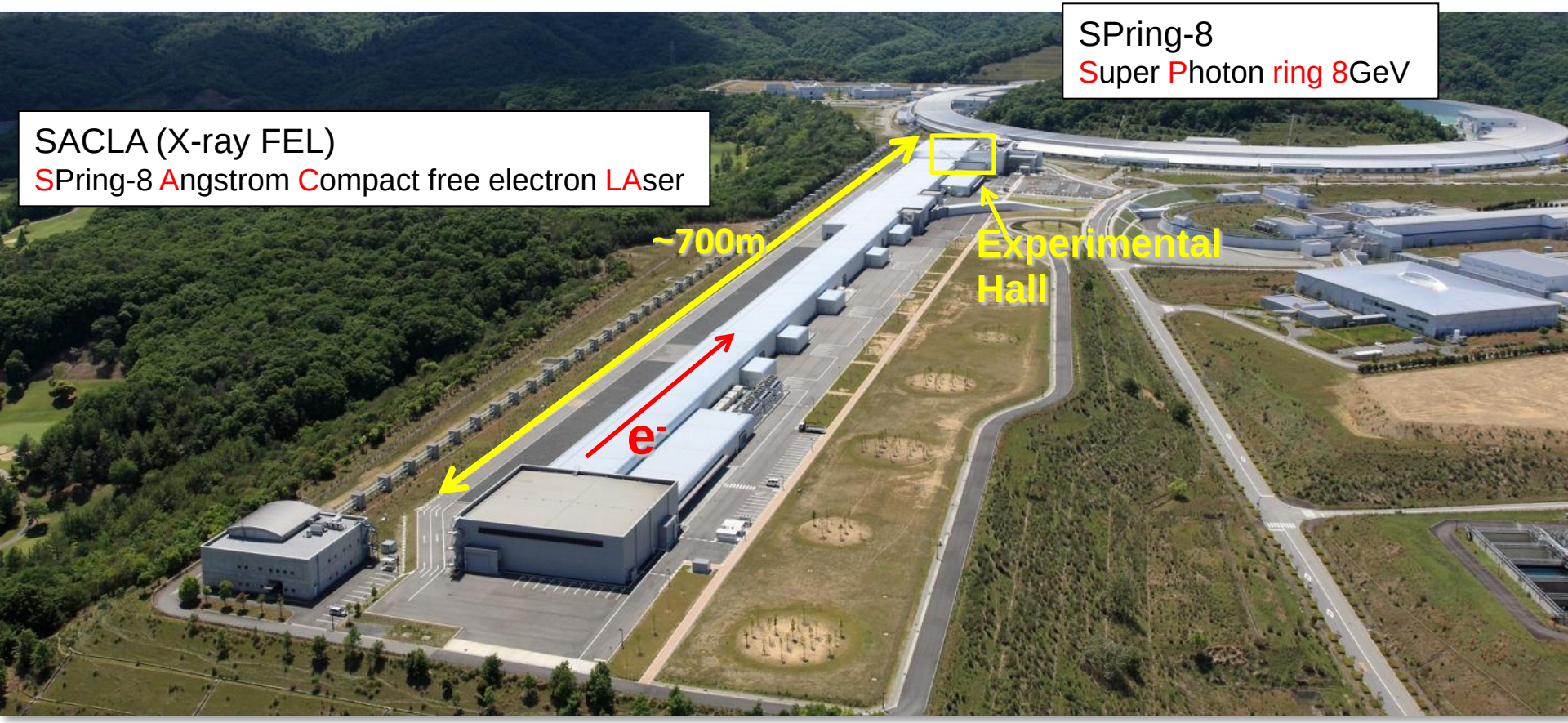
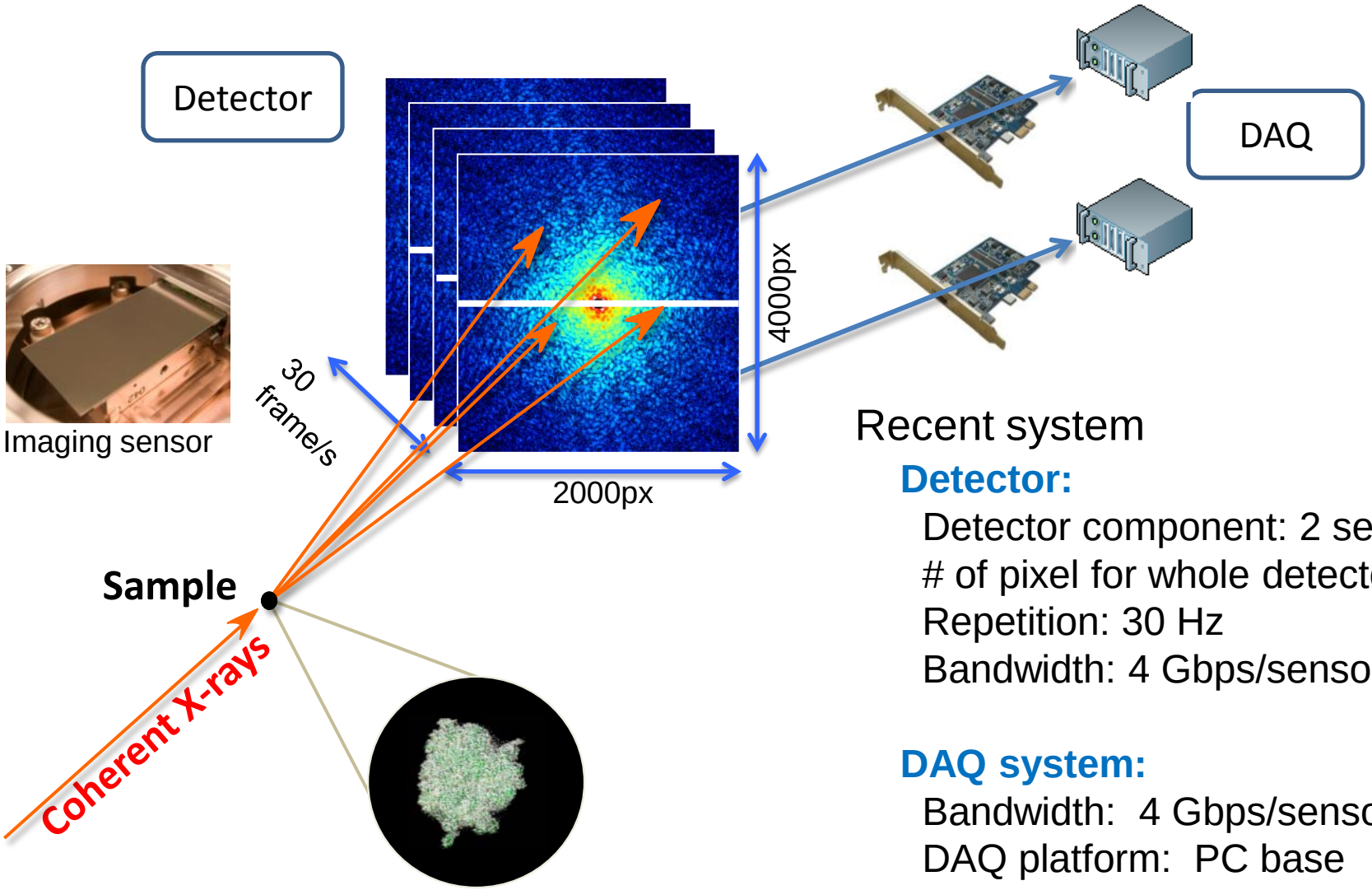
Introduction

- SPring-8 site -



X-ray Imaging experiment



Recent system

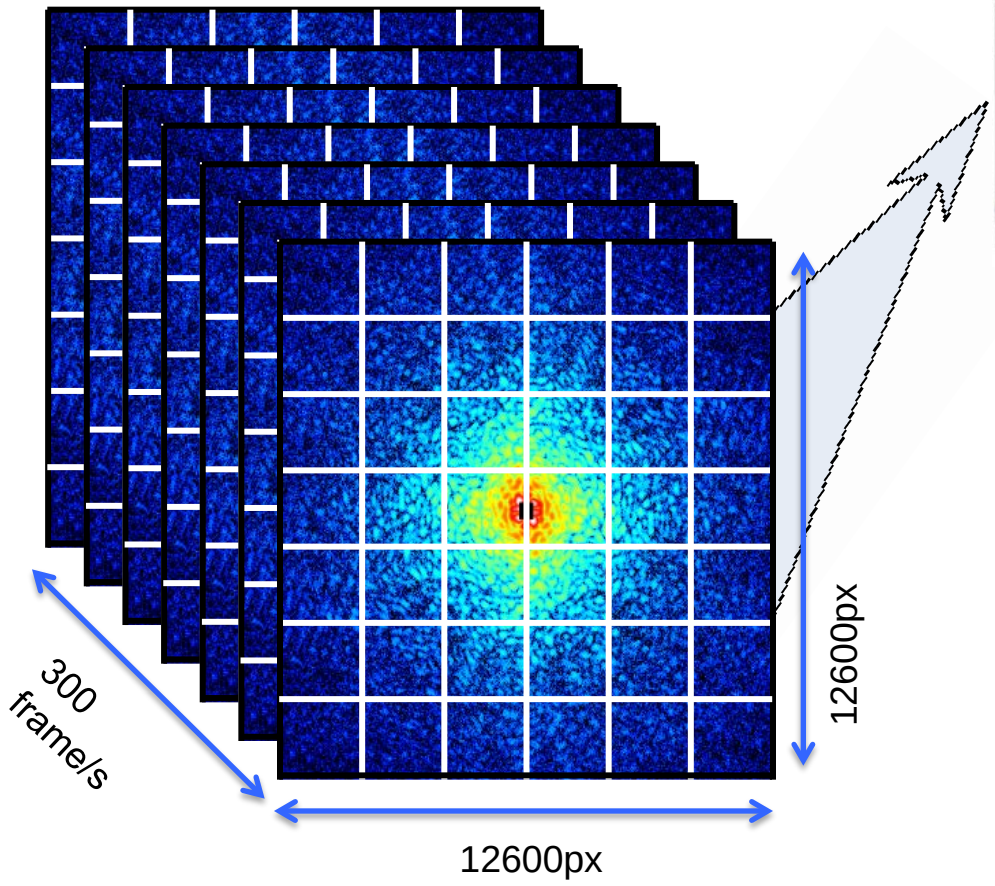
Detector:

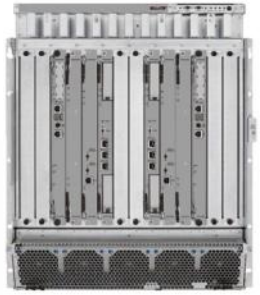
Detector component: 2 sensors
# of pixel for whole detector: 8M
Repetition: 30 Hz
Bandwidth: 4 Gbps/sensor

DAQ system:

Bandwidth: 4 Gbps/sensor
DAQ platform: PC base
Form-factor of board:
PC base

X-ray Imaging experiment





Next generation

Detector:

Detector component: 40 sensors

# of pixel for whole detector: 160M

Repetition: 300 Hz

Bandwidth: 20 Gbps/sensor

DAQ system:

Bandwidth: 20 Gbps/sensor

→Require new interface supporting higher bandwidth

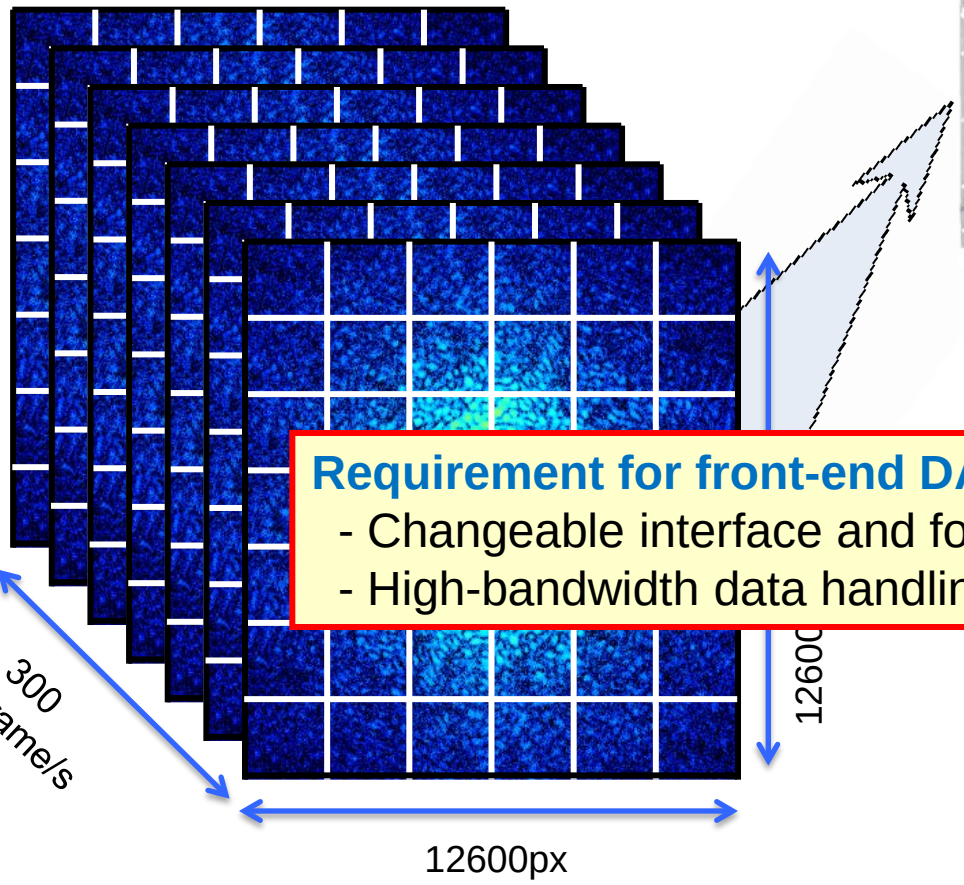
DAQ platform:

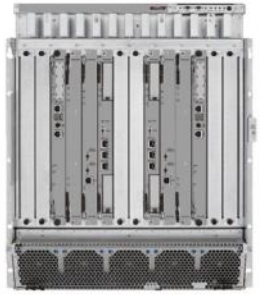
PC base → Backplane base

Form-factor of board:

PC base → Backplane base

X-ray Imaging experiment





Next generation

Detector:

Detector component: 40 sensors

tector: 160M

nsor

Requirement for front-end DAQ:

- Changeable interface and form-factor of DAQ board
- High-bandwidth data handling (up to 20 Gbps)

DAQ system:

Bandwidth: 20 Gbps/sensor

→Require new interface supporting higher bandwidth

DAQ platform:

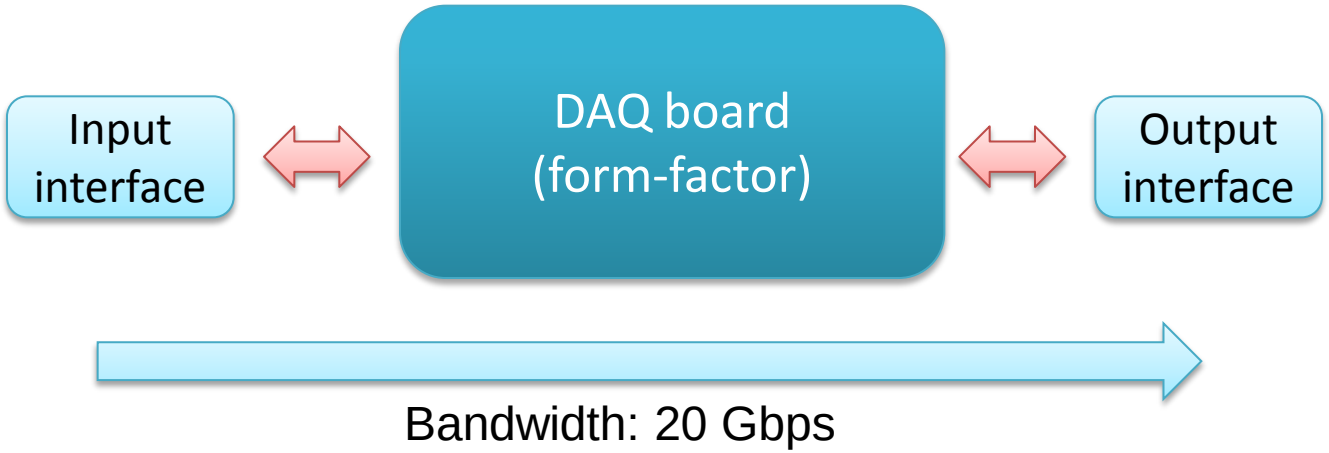
PC base → Backplane base

Form-factor of board:

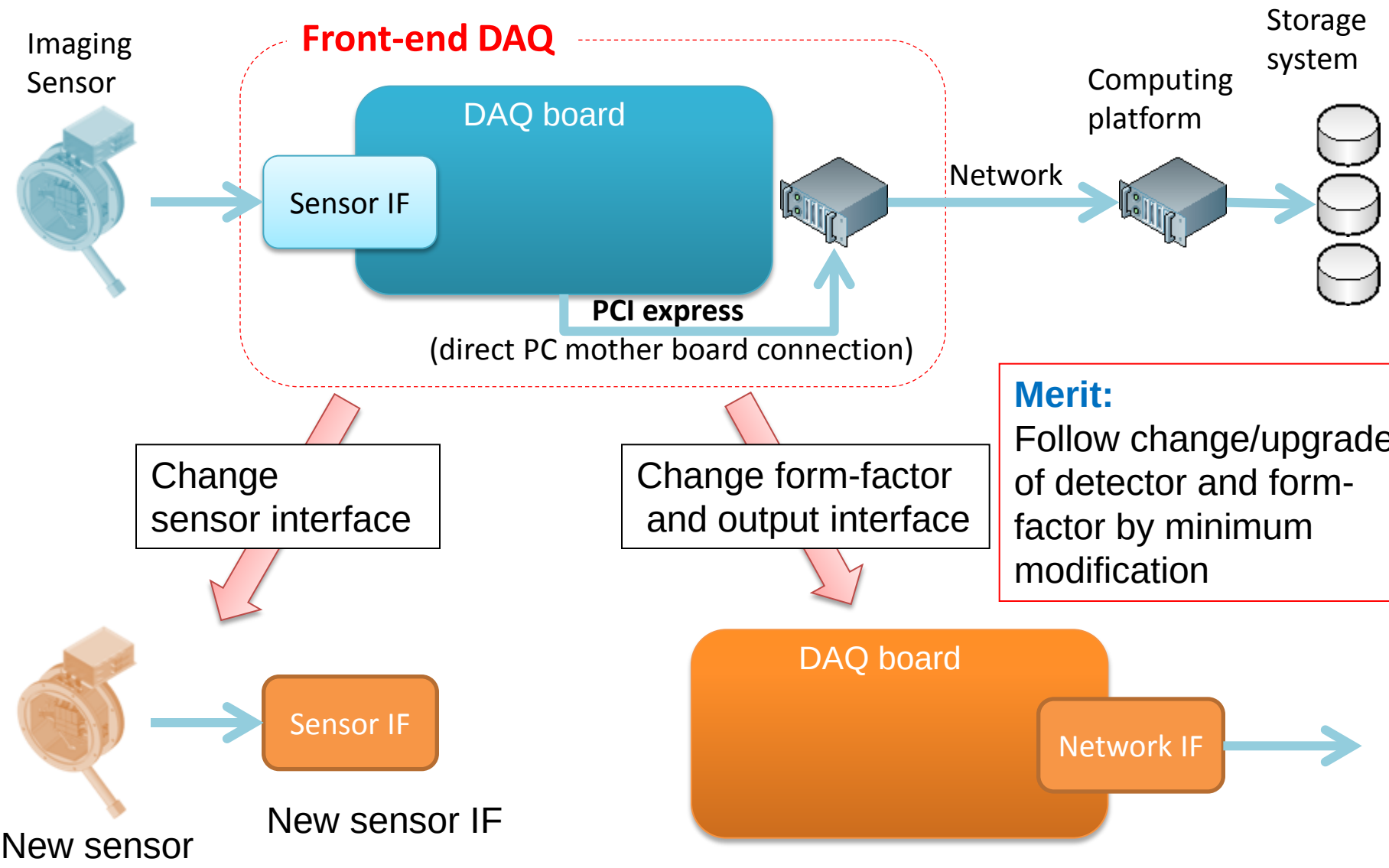
PC base → Backplane base

Conceptual design

1) Adaptive composition
   - Separate interfaces and DAQ board
2) High-bandwidth data handling



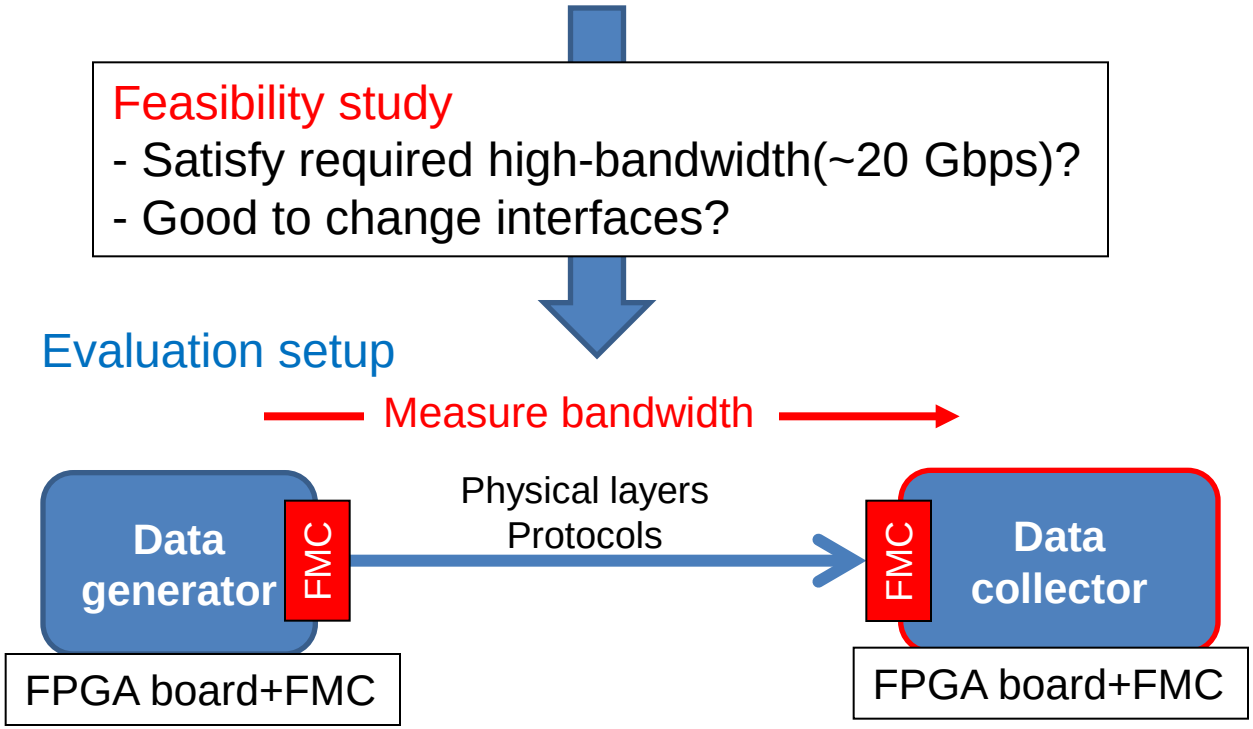
Conceptual DAQ design



Selection of appropriate techniques

- **Changeable interface and DAQ board**
  - FMC (FPGA mezzanine card)
    - Separate I/O from FPGA carrier board

- **High-bandwidth:**
  - FPGA w/ Multi-Gigabit-Transceiver (MGT) based board



Feasibility study

Hardware selection:

Based on COTS products
→ Reduce cost and time for development

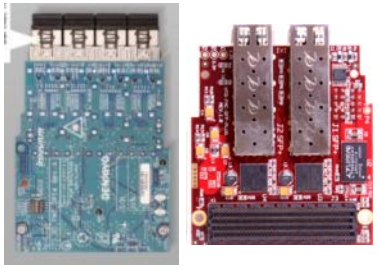
FPGA board (evaluation board):

Platform:	PCI express
PCI express:	8 lanes (Gen 2)
FPGA:	Virtex6 w/ 6.6 Gbps transceiver

FPGA board

IO interface (FMC):

Physical layer	Protocol	Expected	Measured
1) QSFP+ (1ch : 4 lanes)	Aurora	~20 Gbps	19.7 Gbps
2) SFP+ (4ch: 4 lanes)	Aurora	~20 Gbps	19.7 Gbps
3) SFP+ w/10GbE PHY	XAUI	~10 Gbps	9.8 Gbps



FMCs

- FMC has potential of ~ 20 Gbps bandwidth
- FMC is good for changing interfaces

FPGA board and FMC satisfy requirements of our conceptual design

Development of front-end DAQ system

- Camera Link system for SOPHIAS first phase -

Improvement of SOPHIAS detector

SOPHIAS
(Silicon-On-Insulator Photon Imaging Array Sensor)

Prototype sensor

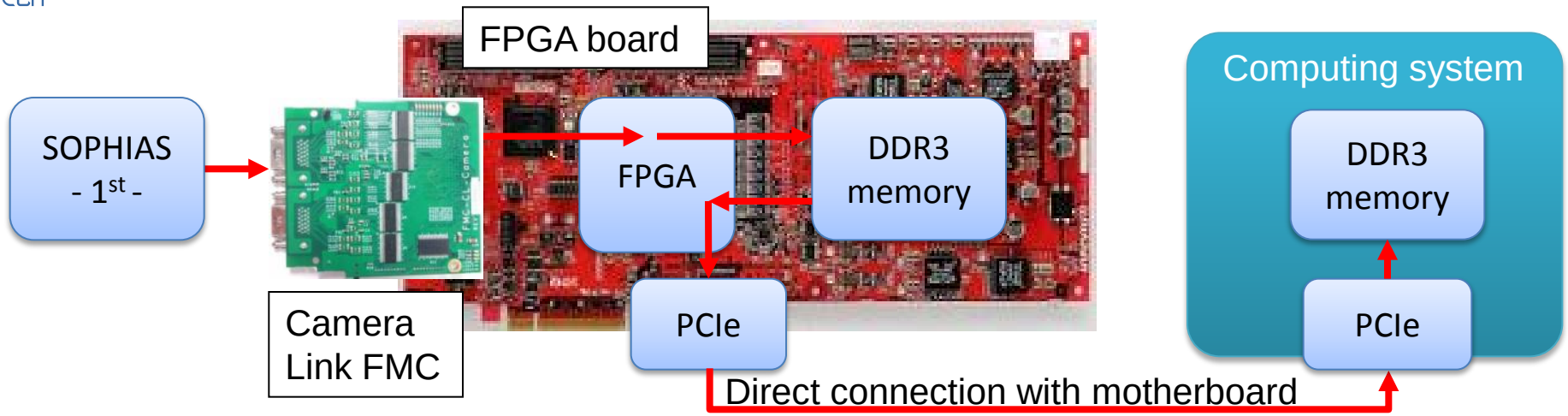
- Under development in SACLA
- Phase-by-phase upgrades are planning
- 1st phase operation will start in 2014

At final phase:
- Detector components up to ~40 sensors
- Bandwidth up to ~20 Gbps/sensor
- Sensor interface should be changed

Our DAQ concept was applied to FE-DAQ for SOPHIAS 1st phase as the first application.

	SOPHIAS (1st)	SOPHIAS (Final)
Sensor		
No. of pixels	~2M	~2M
Depth (bit)	16	16~32
Frame rate	60 Hz	<300 Hz
Release	2014FY	TBD
Experimental conditions		
Frame rate	30 Hz	TBD
Data size for one frame	~16 MB	TBD
Detector components	Dual sensors	~40 sensors
FE DAQ		
Required bandwidth	3.7 Gbps/sensor	~20 Gbps/sensor
Sensor interface	Camera Link full configuration	(should be changed)
Computer interface	PCI express gen2 × 8	TBD

DAQ system for SOPHIAS 1st phase



SOPHIAS:

Output Interface:

Camera Link
full-configuration

Actual bandwidth:

3.7 Gbps

FPGA board:

Form: PCI express

Input Interface:

Camera Link FMC

Output Interface:

PCI express gen2x8

Function:

- Data transmission
- Protocol conversion
- Adjust transmission timing and throughput

Computing system:

OS: Linux

- Only sensor interface of Camera Link FMC and its logic were newly developed

- Re-used existing some boards and logic

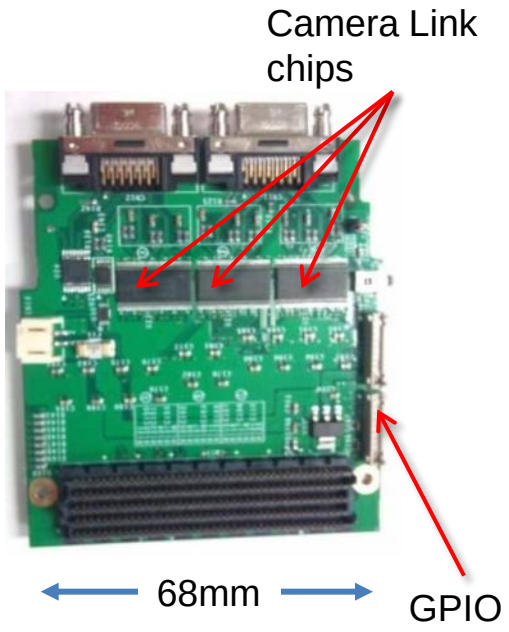
Camera Link Interface FMC

- New development in-house

- FMC (VITA 57) standard
- Camera Link standard ver2.0

-General purpose I/O (GPIO):
→ external trigger signal etc..

- Followed FMC and Camera Link standards
→ can use for any FMC carrier boards and cameras



Checked connection with some devices

FPGA boards:
Virtex6 based (Tokyo electron device)
Kintex7 based (Xilinx)

→ Various COTS products

Commercial cameras:
Adimec OPAL 2000 (base-configuration)
Pco.edge Scientific CMOS (max 6.8 Gbps)

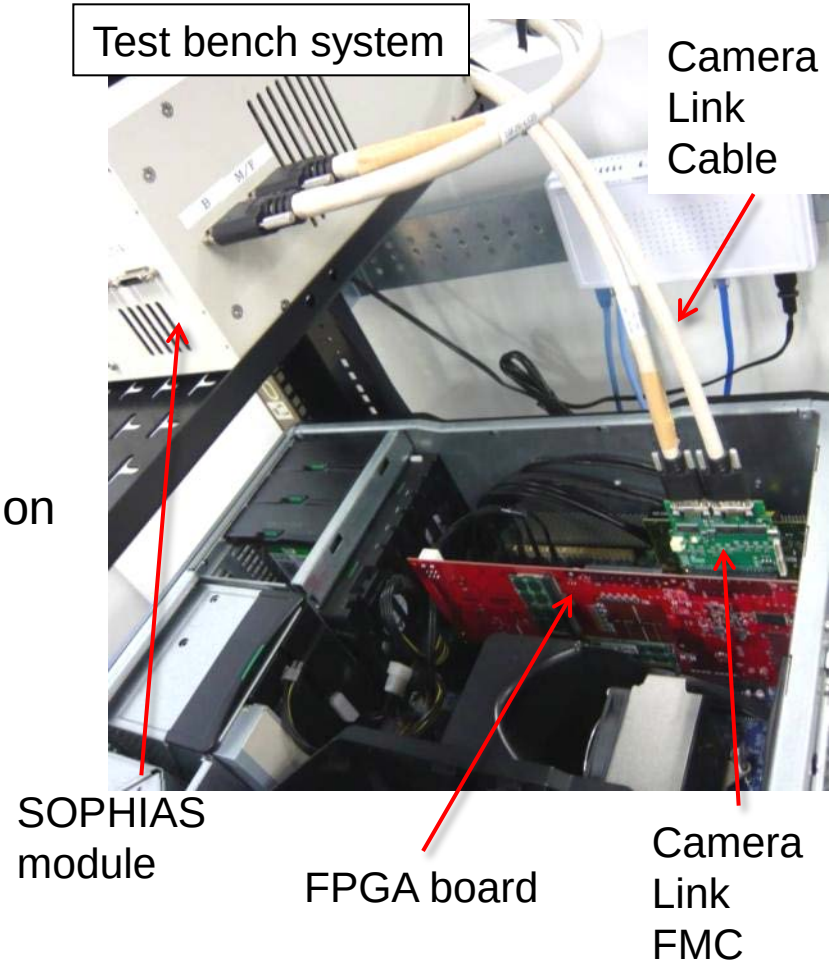
→ Various experimental applications

Evaluation

- Evaluation was applied to connect with SOPHIAS readout module

Checked items:

- Data acquisition:
  - Error check by bit-by-bit comparison
- Sensor configuration:
  - Using Camera Link serial command function
- Stability:
  - 12 hour continuous operation
    w/ 16MB/frame 35Hz
    → ~ 4.5 Gbps bandwidth
    → Acquired 1.5 million events
    → No data error, no data lost



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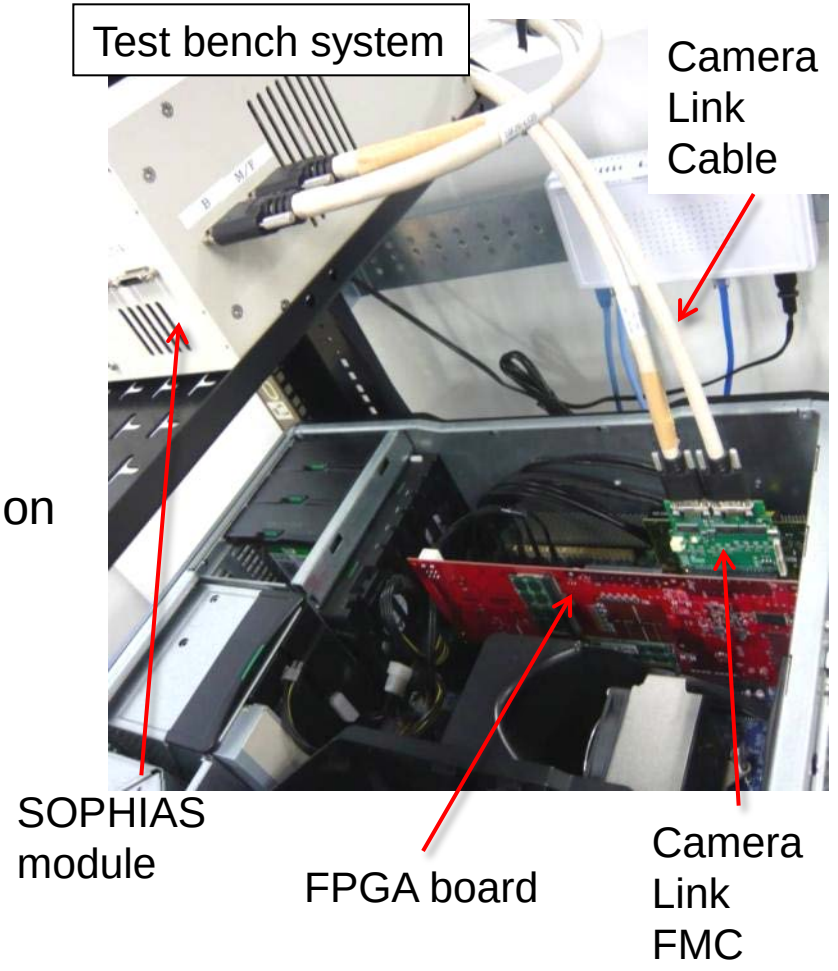


- Front-end DAQ system is ready for 1st phase of SOPHIAS detector
- Our DAQ concept successfully applied

Future Plan (1)

For SOPHIAS final phase:

-Detector components: Up to 40 sensors

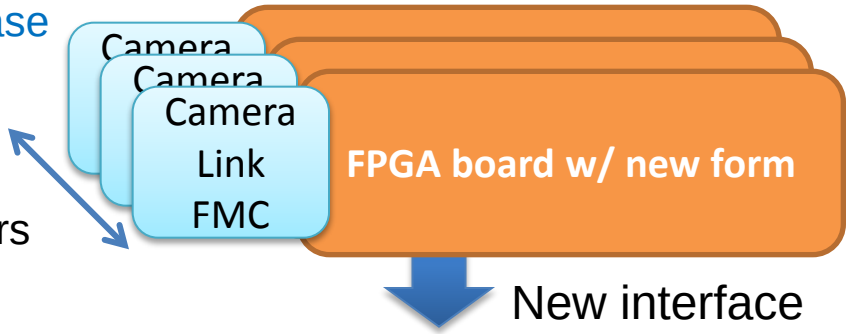
PC based platform → Backplane based platform (e.g. xTCA)

Apply DAQ concept to scalable upgrade of SOPHIAS:

1st phase:
(2014FY~)

-Start 1st phase operation w/ current devices

Phase-by-phase upgrade:



-New FPGA board can be studied its feasibility and stability

-Existing Camera Link FMC can be utilized

Final phase:

-Only sensor interface should be upgraded

-New FPGA board will be under stable operation

Future Plan (2)

For SOPHIAS final phase:

-Higher bandwidth requirement (~20 Gbps)

- We already have experience of AURORA and XAUI protocol w/ FMC

AURORA: 19.7 Gbps

= 6.25 (Gbps) x 4 (lanes bonding) x 0.8 (8b/10b encoding)

- More bandwidth is possible

→ Higher transceiver/more lanes bonding

XAUI: 9.8 Gbps

- Good physical layer for 10GbE implementation w/ low cost FPGA

- For sensor communication

- When exceeds Camera Link bandwidth (6.8 Gbps)
  - New interface can be applied by FMC
  - AURORA and XAUI is ready
- More than 10 Gbps
  - AURORA is ready

- For computer platform communication:

- HW based 10 GbE implementation will be started

Summary

- We have developed a front-end DAQ platform of X-ray imaging detectors for synchrotron radiation experiments.

- Selected technical components were evaluated to satisfy flexible interface change with high-bandwidth.

- For one of applications, the front-end DAQ system with Camera Link interface was developed for 1st phase of SOPHIAS detector, and well performed ~4.5 Gbps stable data acquisition.

-The developed Camera Link interface was designed to be applied to various applications.

-In the future detector upgrade, the front-end DAQ should smoothly follow the scale-up of the detector component. The front-end DAQ system will shift to a suitable platform/interface and achieve further high-bandwidth.