



# Measurement Technology Trends In Instrumentation and Control

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# Agenda

- NI's Involvement in Physics Research
- Technology Trends
- Platform-Based System Development
- Looking Forward



#### NI at Past ICALEPCS

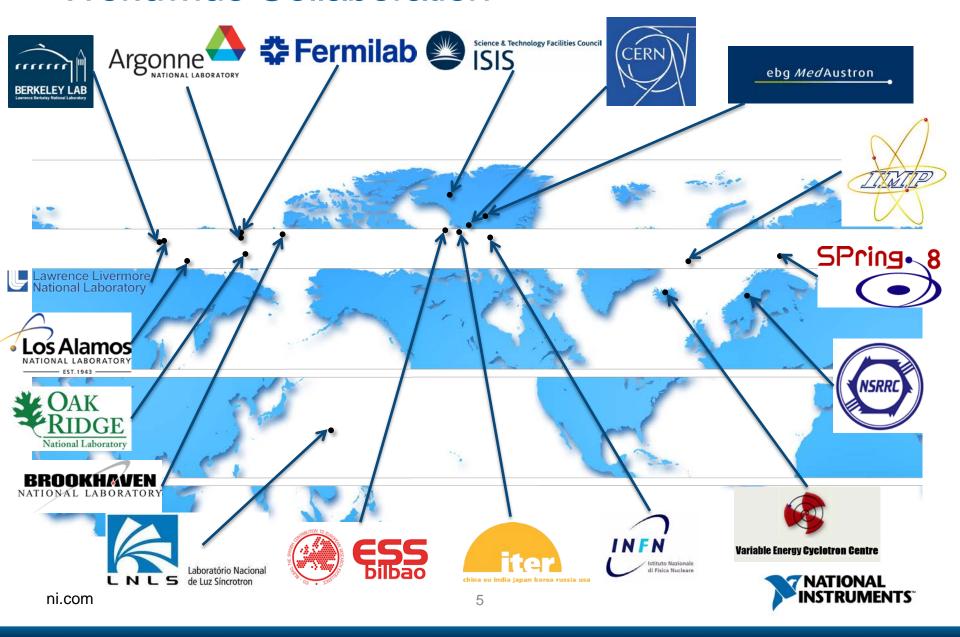
- 2007 It's all about time
  - Dr. Jacob Kornerup, NI Software Architect
- 2009 Leverage Hardware & Software Technologies to Meet Your Control System Needs
  - Murali Ravindran, Sr. Product Manager
- 2011 Customized Off-The-Shelf Technologies Through Industry/Research Facility Partnership
  - Dr. James Truchard, NI Founder/CEO





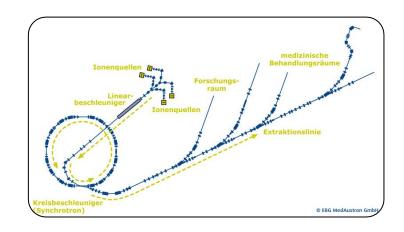


#### Worldwide Collaboration



#### Beam Control System - MedAustron Ion Beam Therapy

- Custom Front End with COTS Real-Time Computing
  - 30k parameters through FPGAbased real-time computation
  - Fast, reliable power supply control for 300 magnets with high precision timing





Customized COTS to meet requirements and complete project on time



#### Instrumentation & Control for LANSCE LINAC

- LANSCE Upgrade project at LANL
  - ~ 10,000 I/O points for remote instrumentation and control



- Latest instrumentation and control hardware compatible with existing drivers and records
  - Existing EPICS interface and IOC records with latest hardware
  - FPGA-based motion control

Upgrading to latest technology while preserving existing investment

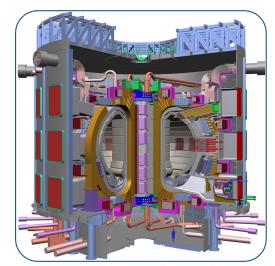




# Fast Interlock, Control and Diagnostics - ITER

- ITER instrumentation and control requirements
  - 1 million I/O points
  - 20 GB/s archive rate
- COTS hardware with Linux drivers
- Native EPICS device drivers
- Special testing
  - Fast and Thermal neutrons
  - Gamma rays

Developed custom drivers and performed special testing to meet needs



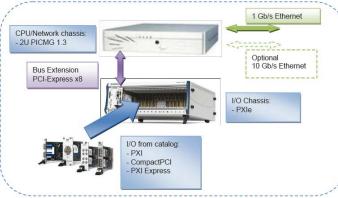
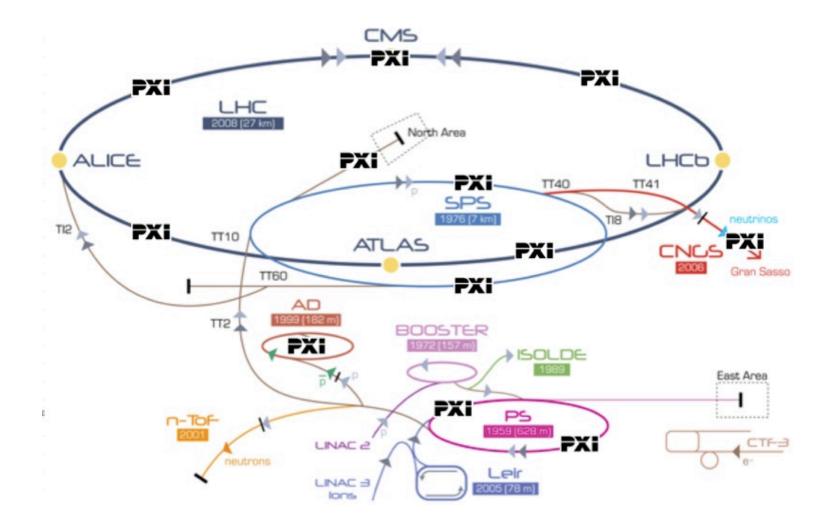


Figure 1 – A General Purpose Fast Controller

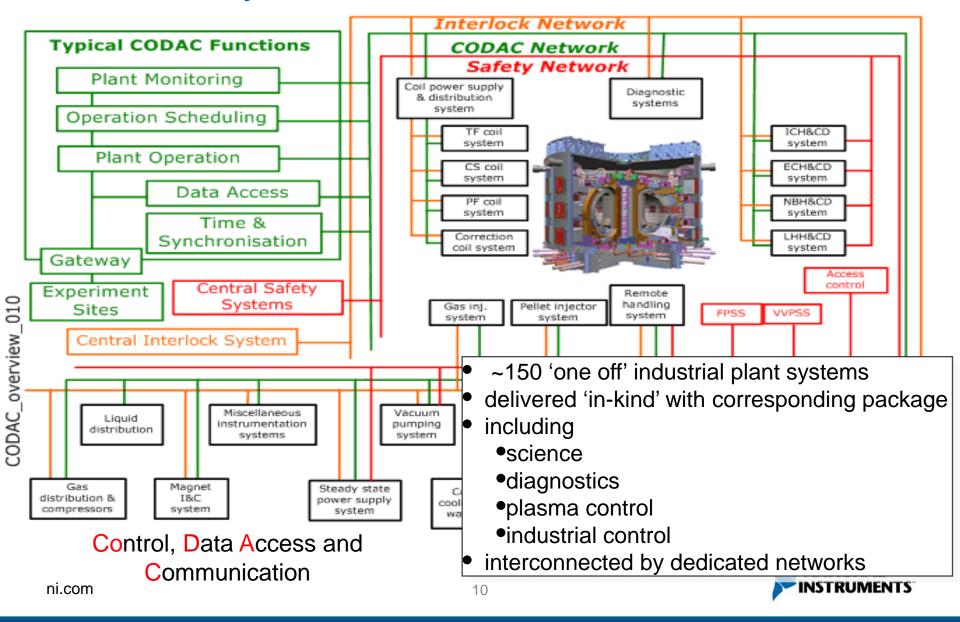


#### CERN Accelerator Control Systems and NI Technology

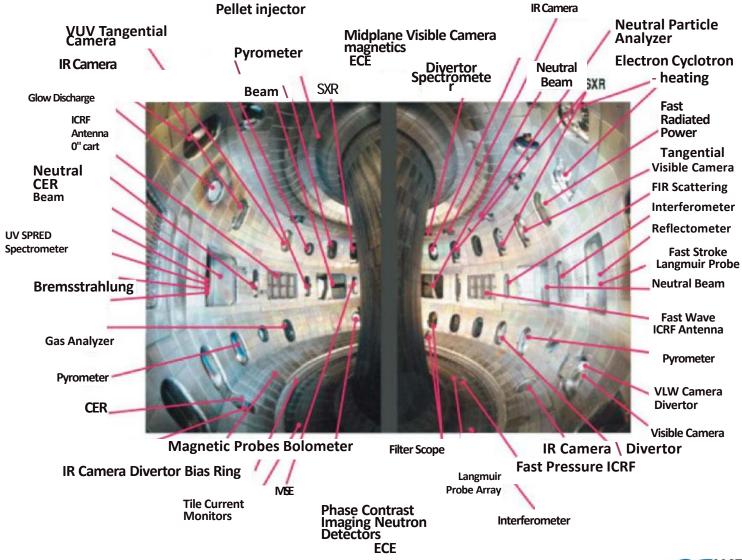




# CODAC System Architecture for ITER



# DIII-D Example Installed Diagnostics





# **Technology Trends**



Data Converters



High performance processing



Network communication



# Trends in High Resolution ADC (most bits and most speed)

1990 1998 2006 A/D CONVERTER ADC- ECONOVERTER 8 bit 50MS/S 16 bit 250MS/s 10 bit 5GS/s 8 bit 3MS/s **Pipeline Pipeline Pipeline Pipeline** 16 bit 1MS/s SAR 16 bit 3MS/s 18 bit 3MS/s 16 bit 1MS/s SAR monolithic **SAR** monolithic **SAR** monolithic Hybrid 20 bit 10kS/s Σ-Δ 24 bit 105kS/s Σ-Δ 24 bit 250kS/s Σ-Δ 16 bit 50kS/s Σ-Δ

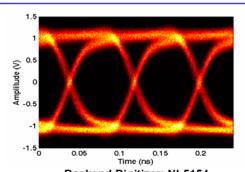
Look for 12 to 14-bit, 5-10 GS/s Pipelines by 2016



# Beyond 2013

- Massively interleaved CMOS ADC's
  - 56 GSPS/8 bit (320 converters x 175 MSPS) already available
  - Magical Track and Holds
  - Designed for optical high speed communications
- Experimental Time Stretch Photonic ADCs
  - TiSER (Time Stretch Enhanced Recorder)
  - "Fits in a single room"
  - 10 Terasamples/sec transient ADC



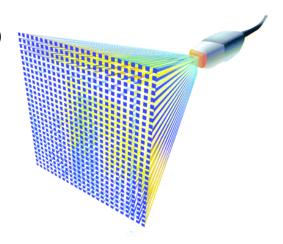


Backend Digitizer: NI-5154 (1-GHz bandwidth, 2-GS/s sample rate) Stretch Factor: 23

Optoelectronic Circuits and Systems Laboratory



- 12 Gbps+ serial data links
  - CMOS scaling minimizes pin count/traces (JESD204B)
  - Very high bandwidth OR high channel count
  - Imaging applications



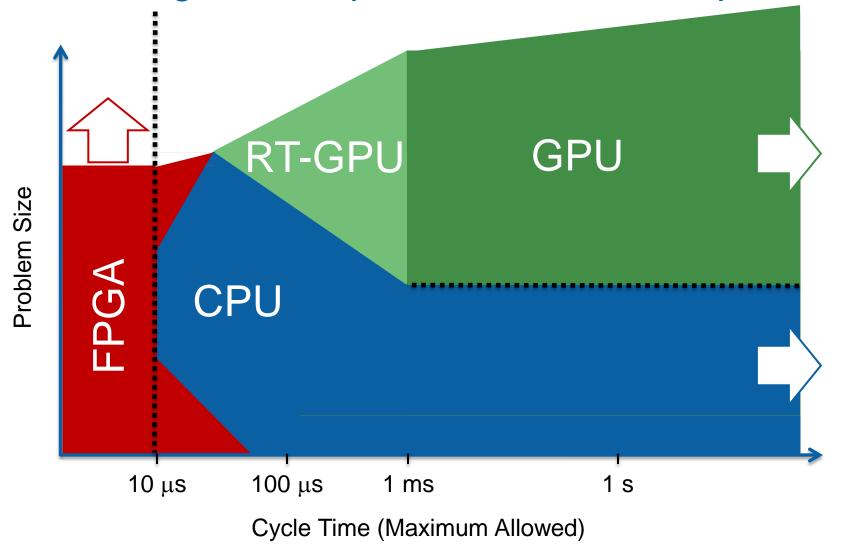
Matrix Array Transducer for Ultrasound

#### Real-Time HPC Trend

#### **Size and Complexity / Cycle Time Quantum Simulation** ELT M4 **DNA Seq** Tokamak (GS) **AHE** ELT M1 1 x 1M+ FFT Tokamak (PCA) 1M x 1K FFT 2007 2008 2009 2010 2011 2012

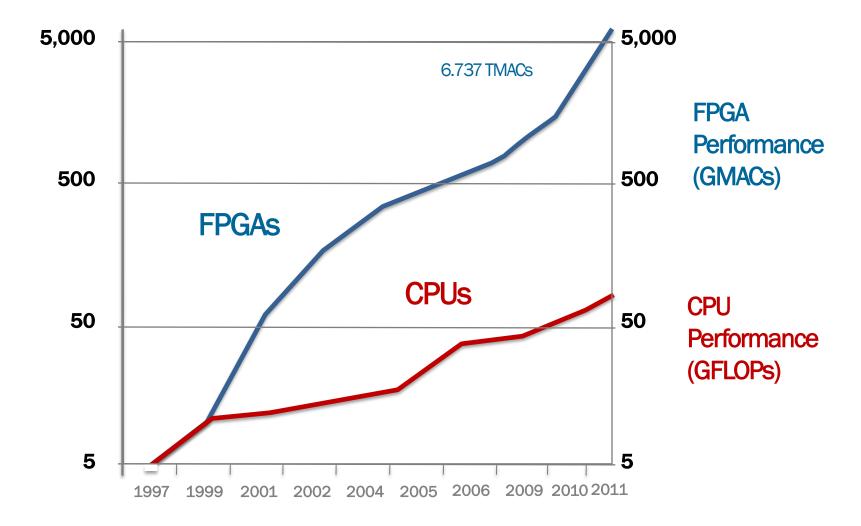


#### Processing Landscape for Real-time Computation





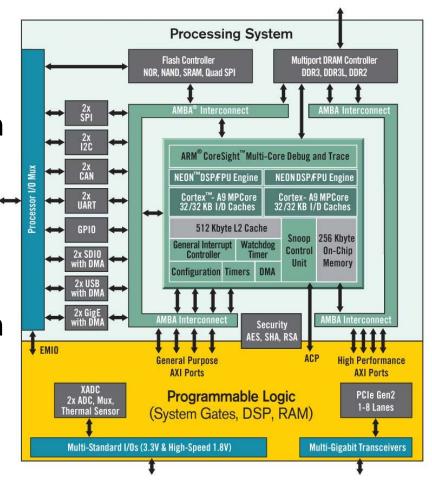
#### Parallel Architectures Drive Performance





# Processing Subsystems on FPGAs

- Xilinx Zynq and Altera Cyclone V with HPS
- High performance application processing system on the same die
- Much higher bandwidth between the processing system and FPGA fabric than traditional architectures
- FPGA fabric offload of computations and custom instruction



Xilinx Zynq-7000 All-Programmable SOC



# IEEE 802 Ethernet Standards Activity

 Efforts driven by 802.1 (bridges/switches) and involve 802.3 (cabling) and 802.11 to enable reliable, high performance control applications over standard and shared Ethernet

Representatives involved from multiple industries





# Key Technical Goals of Standards Activity

- Converged network (control, streaming, "normal" traffic)
- <uS synchronization between all nodes</li>
- Low latency (end-to-end latency of <30uS)</li>
- Network redundancy with 0 fail over time
- Scaling with Ethernet evolution



# **Graphical System Design**

#### A platform-based approach to measurement and control























# Graphical System Design

#### A platform-based approach to measurement and control







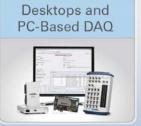












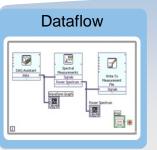


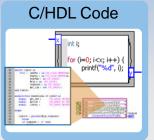


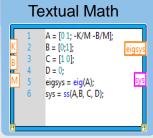


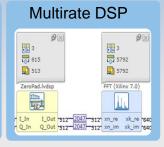


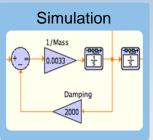
# Multiple Models of Computation

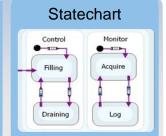




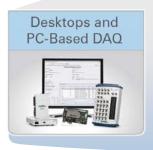




















# Other Relevant Technology Trends in Industry



 Highly Available and Reliable Instrumentation Systems



Hardware monitoring and failure prediction



1. Seamless large scale deployment



2. Tools for Big Analog Data



# **Looking Forward**

- Physics research applications are extremely demanding for measurement and control systems
- Many unique needs can be met with off-the-shelf technology
- A platform-based approach enables use of standard technology in a way that supports
  - Efficient development of highly-customized solutions
  - Extensive collaboration with commercial vendors
  - Long-term support and evolution of systems



# NATIONAL INSTRUMENTS\*\*

