High Level FPGA Programming Framework Based on Simulink

B. Fernandes*, P. Gessler, and C. Youngman
WP76, DAQ & Control Systems, European XFEL GmbH, Hamburg 22761, Germany

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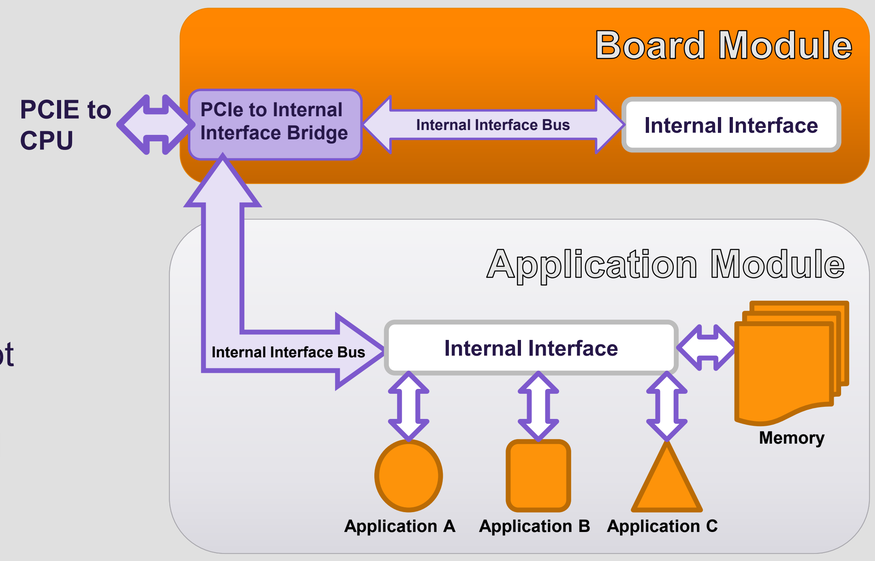
Abstract

A high-level FPGA programming framework is currently under development at the European XFEL in collaboration with the Oxford University within the EU CRISP project. This framework allows for people unfamiliar with FPGA programming to develop and simulate complete algorithms and programs within the MathWorks Simulink graphical tool with real FPGA precision. Modules within the framework allow for simple code reuse by compiling them into libraries, which can be deployed to other boards or FPGAs.

FPGA Projects Structure

Fixed Structure of top FPGA projects:

- **Board module**: everything related and specific to configuration/monitor of board features and provide these IOs to user applications module;
- **Application module**: includes user applications modules which may or may not be board specific;
- Easy porting and update of both board and application code;
- Independent development.



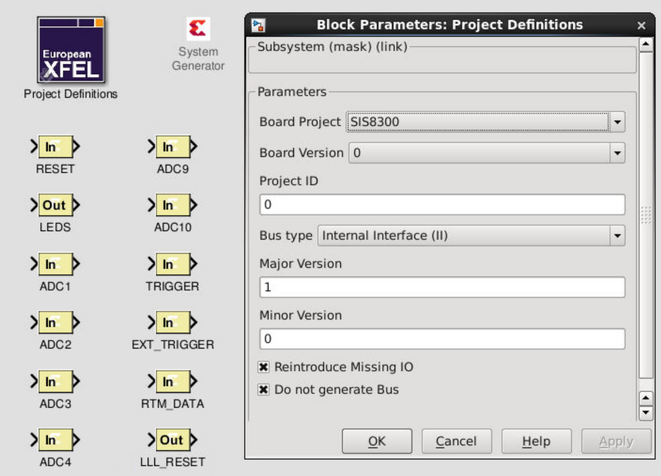
Internal Interface bus protocol:

- VHDL API package that eases register access and definition;
- Applications have a specific set of registers and memories with definition being preformed at the hardware level;
- A XML file for each application is generated which is then used by our software tools to access the defined registers/areas.

High Level FPGA Application Development

- Abstract end user from hardware programming languages and hardware concepts (clock routing, pin placement, etc.);
- User design environment automatically setup for the target board;
- Library with blocks that simulate the behavior of available features;
- Allow user defined registers and memories and generate the necessary logic to later communicate with the bus protocol;
- Easy to port and distribute applications to other projects/boards.

Simulink Framework Workflow

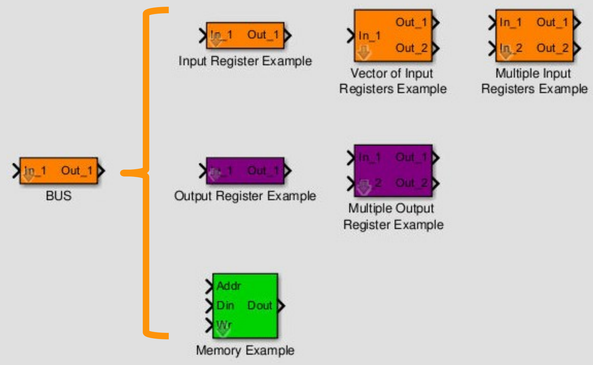


Board Definitions block:

Generates the IO available for the chosen board and examples of expected input signals. Setups the environment for the selected board. User also selects the bus protocol to the PCIe Bridge.

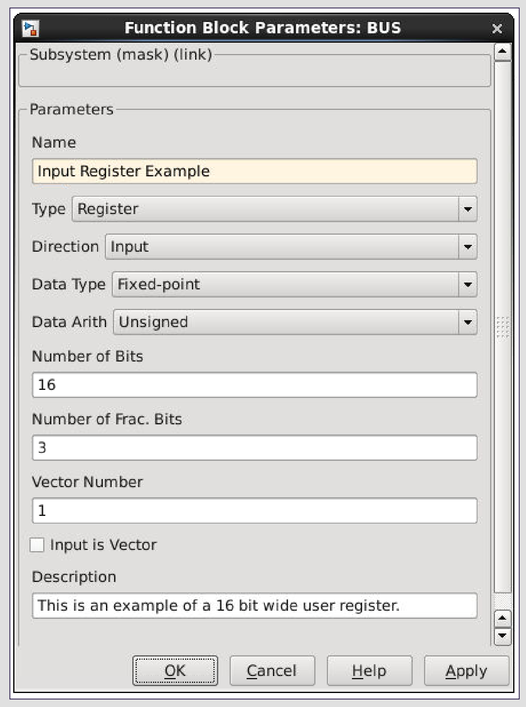
Board Feature block:

Blocks that accurately simulate the behavior of features available on the board.

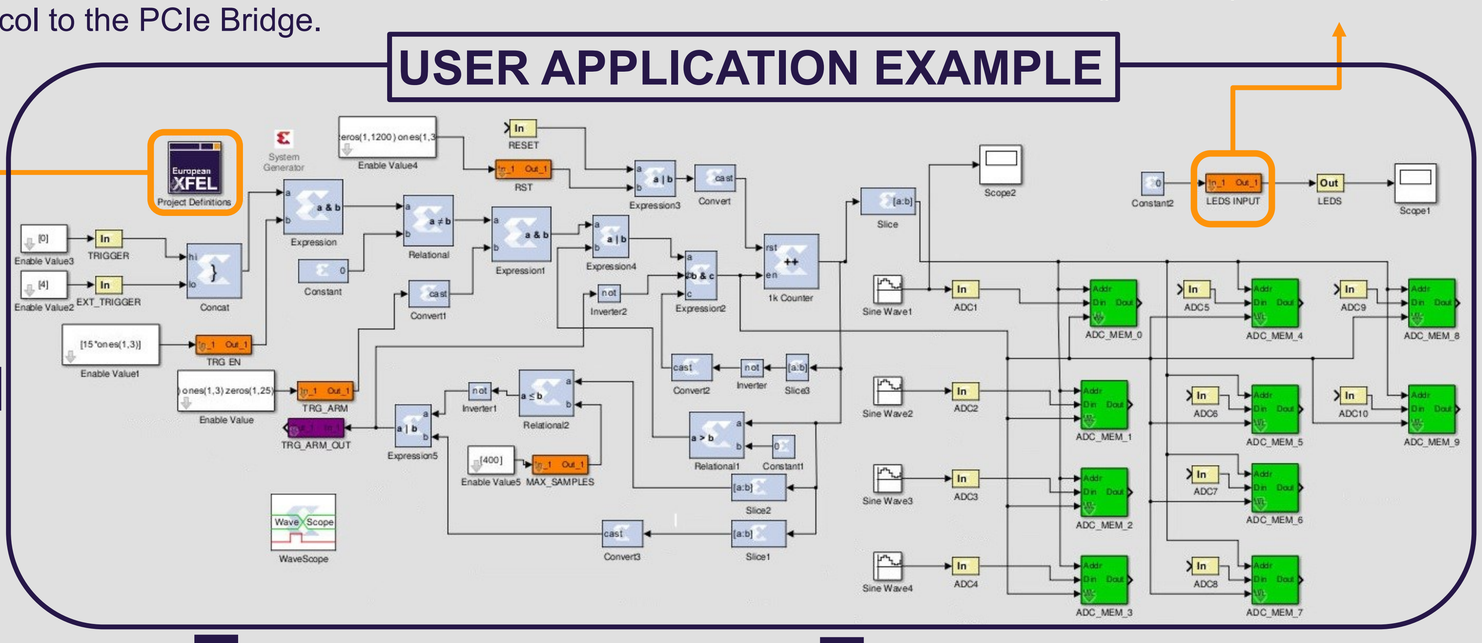


BUS block:

User defined registers/memories which are later accessible by the chosen protocol. A set of parameters are used to regenerate the block properties according to the specified values.



USER APPLICATION EXAMPLE



Standalone Module of User Application to easily include on the library, making it available for other users/projects.

XML FILE

XML File used on software with all properties of user defined registers and memories.

NGC FILE

NGC File of user algorithm with bus protocol logic generated according to the user defined registers and memories. Automatically added to ISE project of chosen board.

Further Development

- Include Simulink projects directly in FPGA top level projects;
- Integrate additional protocols, namely Ethernet, Wishbone and UART;
- Partial reconfiguration in the FPGA projects structure.

*bruno.fernandes@xfel.eu