Development of a Machine Protection System for Fermilab's

ASTA Facility *

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Abstract

Fermilab's Advance Superconducting Test Accelerator (ASTA) under development will be capable of delivering an electron beam with up to 3000 bunches per macro-pulse, 5Hz repetition rate and 1.5 GeV beam energy in the final phase. The completed machine will be capable of sustaining an average beam power of 72 KW at the bunch charge of 3.2nC. A robust Machine Protection System (MPS) capable of interrupting the beam within a macro-pulse and that interfaces well with new and existing controls system infrastructure is being developed to mitigate and analyze faults related to this relatively high damage potential. This paper will describe the component layers of the MPS system including main actuators such as the FPGA-based Laser Pulse Controller, the Beam Loss Monitoring system design and the controls and related work done to date.



Introduction

The ASTA facility will be capable of testing 3 or more ILC-type SRF cryomodules under full ILC beam intensity and bunch structure. In addition, test beamlines and downstream beamlines will provide a venue for advanced accelerator R&D (AARD). Figure 1 shows a plan view of the facility that is divided into low energy and high energy phases. The electron beam is produced by a 1.3 GHz RF photo-injector and then accelerated to ~50 MeV by two 1.3 GHz SRF cryomodules, each containing a single 9-cell cavity, before being injected into the 1st 8-cavity cryomodule. Initial beam commissioning of the cryomodule string will take place with a single Tesla type III+ cryomodule [1] driven by a 5 MW klystron; considered stage 1 [1]. The next stage of commissioning will take place with two Tesla type III+ cryomodules and one ILC type IV cryomodule. This cryomodule string will be driven by a 10 MW multi-beam klystron, with its associated HV power supply, modulator, and waveguide distribution system. The high energy beamlines downstream of the cryomodules will provide transport to an AARD experimental area and to the high energy beam dump.





Figure 1 : Machine Layout of ASTA Facility



Overview



The overall MPS design is divided into 3 layers; a sensor layer to collect sub-system status, a process layer that utilizes the status to generate the permits and an actuator layer to receive the permits and inhibit the beam. The initial stage of this development involves the design of the Laser Pulse Controller.



Figure 2 : ASTA Facility



Figure 4 : Main MPS System setup

Figure 3 : MPS Overview

Laser Pulse Control

This device is designed to control the number and the spacing of bunches in a macro-pulse by picking single laser pulses out of a train; achieved by manipulating the Pockels cell (voltage-controlled wave plates). The LPC basically provides a gate, the length of which determines how many 3MHz laser pulses are accepted. The gate widths (minimum through maximum), delay (relative to RF), and timing for first bunch trigger along with several other parameters are configured via the control system. The maximum allowed duration for the gate is 1ms. Figure 5 and 6 illustrates this scheme diagrammatically.



Fast Protection

The MPS includes a fast protection system that is based on 40 Beam Loss Monitors (BLMs). It is being designed to interrupt the beam within a macropulse and relies heavily on the ability to detect and react to losses within a few nano-seconds; the loss monitors are made from plastic scintillator material and are coupled to photomultiplier tubes. First injector beam test, Figure 9, with these loss monitors indicate that the monitor possess the necessary sensitivity required to detect low charged losses as well as dark current.

Protection System



Figure 5 : LPC Overview

• Block the Pockels cell based pulse kickers as long as the MPS input is in an alarm state. Enforce the limit on the number of bunches as given by the currently selected beam mode. • Close the laser shutter on request of the MPS. This may happen when there is no valid operational mode or when some combination of loss monitors exceed thresholds which trigger a dump condition.

Gate signal Specifications: > < 100 ps jitter > tunable to 100 ps intrinsic litter) Max = 1ms "w" determines no. of bunch Q.E of gun/laser system determined from measured inputs : > Diode (light) > Charge measured (toroid) > number of bunches

Figure 6 : LPC Gate Specification



Figure 7 : LPC hardware in Laser room

Controls Integration

All loss monitor signals will be conditioned and digitized to produce alarm signals based on the integration period of the signals. Thresholds for a single bunch, a macro-pulse and an entire bunch train will be calculated



General Purpose FPGA board (V1495) serves as the backbone of the LPC and MPS systems and provides real time computing.



HV, Anode signal and LED connections



Figure 8 : BLM board electronics



Figure 9 : First Beam results

Daughter card designed for the V1495 board provides 128 MB of SDRAM. Memory extension critical for logging sensor readings around detected fault.



Futures:

- ✓ 8 channels, 14 bit at 6U VME Board
- DC/AC- up to 125MSPS Operation
- Up to *16M* sample per channel DDR2 buffer
- **Different Modes (12) of Operation**
- Hardware & Software onboard data processing
- Smart triggering based on FPGA algorithm

Figure 10 : VME Digitizer

Summary

Significant progress has been made in developing the MPS system with the design of both the LPC and BLM systems. These systems were crucial in enabling and displaying the first photoelectrons produced at ASTA. Additional effort is underway towards collecting subsystem status and developing a reliable MPS for ASTA. System integration into the complex and commission challenges lay ahead



Figure 11 : General Purpose FPGA

Figure 12 : Daughter card design

The data path between the daughter card and the main MPS FPGA board is 32 bits wide. If running at 62.5 MHz, the peak through-put is 250 MB/s

References

[1] M. Church, et al. "Status and plans for an SRF test facility at Fermilab", SRF'11, Chicago, August 2011, MOPO006; http://www.JACoW.org.

A. Warner and Linden Carmichael, "Development of a Machine Protection System for the [2] Superconducting Beam Test Facility at Fermilab", ICALEPCS'11, France, October 2011, WEPMU013; ; http://www.JACoW.org.

M. Church, et al. "Design of the Advanced Superconducting Test Accelerator", Beams-doc-[3] 4212, September 2012