A number of beam position monitors (BPM) are being installed at the Front End Test Stand (FETS) H⁻ ion source at the Rutherford Appleton Laboratory, UK, as part of the 3 MeV medium energy beam transport. The FETS ion source delivers pulses up to 2 ms long at a rate up to 50 Hz and a maximum current of 60 mA, with a 324 MHz micro-bunch structure imposed by the frequency of the FETS RF acceleration cavity. The response of an in-house designed button BPM has been simulated and then characterised on a wire-based test-rig and the results are presented. The output from

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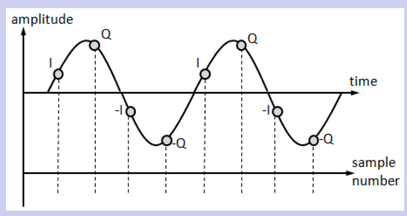
Characterising the Signal Processing System for Beam Position Monitors at the Front End Test Stand

Introduction

A number of beam position monitors (BPM) are to be installed at the FETS H- ion source as part of the 3 MeV medium energy beam transport (MEBT). The response of an in-house designed button BPM has been simulated and characterised on a wire-rig previously. A PXI-based FPGA signal processing system is evaluated using signals from a BPM in the wire-rig to verify the speed and precision of the processing system. The FPGA code can determine the beam position in eight BMs, within one microsecond of the signal sampling being completed.

Position Determination

The signal from each BPM electrode, 32 signals in total, is down-mixed using a single-stage mixer, from 324 MHz to an intermediate frequency (IF) of 10.125 MHz, using a local oscillator (LO) of 313.875 MHz. The electronics has digitally controlled amplifiers and attenuators before the mixer, and again after the low-pass filter. The resulting IF signal is amplified and filtered, with a maximum output level of $2V_{pp}$. The IF is sampled at exactly four times the IF, namely 40.5 MS/s. The peak amplitudes for the positive and negative halves of the cycle are calculated independently allowing any possible offset to be assessed. The position is determined by taking the difference divided the sum of the signals from opposite BPM electrodes as shown below. The constants k_x and k_y are determined empirically using the wire-rig.



IQ Sampling

$$V_{peak} = \sqrt{I^2 + Q^2}$$

IF amplitude

$$Position_x = k_x * \frac{V_{right} - V_{left}}{V_{riaht} + V_{left}}$$

$$Position_y = k_y * \frac{V_{top} - V_{bottom}}{V_{top} + V_{bottom}}$$

Beam position determination

Digitizer and FPGA Code

A PXI-based FPGA card and digitizer FPGA adaptor module (FAM), both manufactured by National Instruments, are used to acquire the IF signals. The FAM is a 32-channel, 12-bit, simultaneously-sampled 50 MS/s digitizer module that is directly controlled by the FPGA card. The FPGA code is written in LabVIEW, specifically using the FPGA module and functions from the *high-throughput maths* palette, allowing determinstic operation on fixed-point numbers.
The FPGA code operates on all 32 digitized signals in parallel, before combining the amplitudes of opposite electrodes into *x* and *y* positions. The table shows the sampling interval (time between successive beam positions) and the number of clock cycles required for the calculation.
The positions are DMA'd to the PXI host controller, running LabVIEW real-time, before being accessed by a viewer client and logged.

PXI-7954R (FPGA) and NI-5752 (Digitizer)

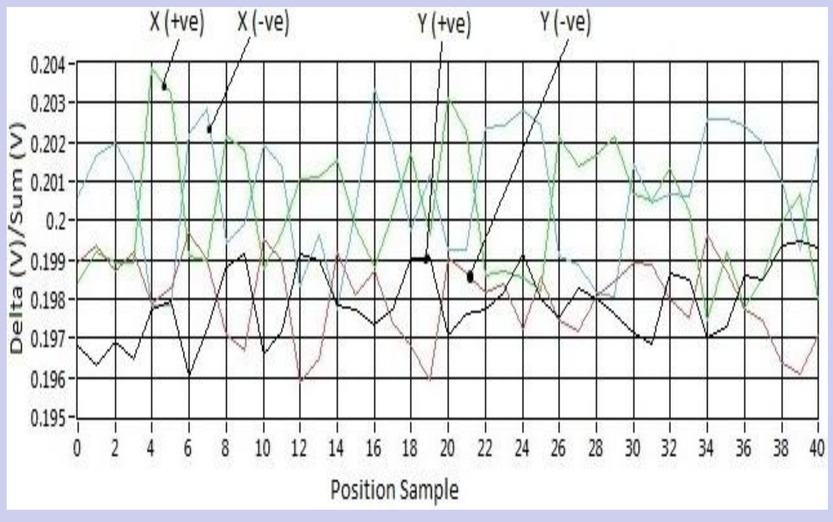
Sampling Interval (µs)	Number of clock cycles	Processing time at 40 MHz (µs)
25.28	46	1.15
12.64	44	1.10
6.32	42	1.05
3.16	40	1.00
1.58	38	0.95

Optimisation

The FPGA code is currently compiled using a 40 MHz internal clock. Using a higher speed clock can decrease the processing time, but makes fitting the compiled code into the FPGA more difficult. A further reduction can be obtained by decreasing the number of bits used to describe the intermediate processed values. Pipelining, starting a subsequent calculation before the previous one has finished, can also speed up the calculation.

Results & Conclusion

A typical result for the wire position as determined by the FPGA is shown, indicating a precision of better than 1%, equivalent to better than 20 µm, a factor five better than required. It is expected that a similar accuracy will be apparent when measuring the H- beam position.
Using the wire-rig and FPGA has produced a very satisfactory and cost-effective system for beam position monitoring.



The Front End Test Stand Collaboration

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