# A NEW ORBIT SYSTEM FOR THE CERN ANTIPROTON DECELERATOR

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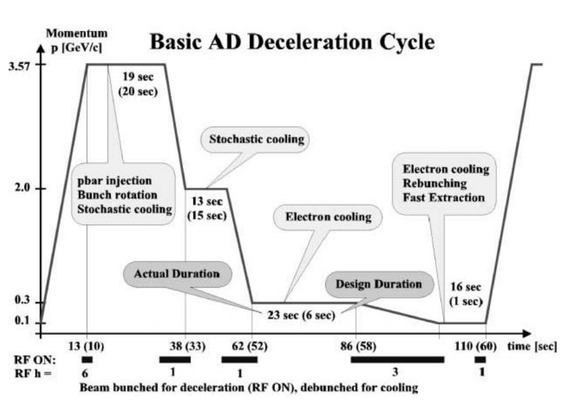
## ABSTRACT

This contribution will describe the new orbit system foreseen for the Antiproton Decelerator (AD) located at CERN. The AD decelerates antiprotons from 3.57 GeV/c down to 100 MeV/c, with an intensity ranging from $1\times10^7$ to $5\times10^7$ particles. The orbit system developed is based on 34 horizontal and 29 vertical electrostatic beam position monitors (BPMs) fitted with existing low noise front-end amplifiers. After amplification, the BPM signals will be digitized and down-mixed to baseband, decimated and filtered before computation to extract the position. The digital acquisition part of the orbit measurement system is based on the VME Switched Serial (VXS) enhancement of the VME64x standard and includes VITA57 standard FPGA Mezzanine Cards (FMC). The system is foreseen to measure complete orbits every 2.55 ms with a resolution of 0.1 mm.

## INTRODUCTION

- AD ring is a synchrotron where ~$3x10^7$ antiprotons are injected at 3.57 GeV/c and extracted at 100 MeV/c.
- The AD revolution frequency ($f_{REV}$) varies from 1.59 MHz down to 174.5 kHz.
- Present orbit system is a multiplexed system with limited timing performance (complete orbit measurement every 1.2 s).
- New requirement of orbit measurement on deceleration ramps involves a parallel acquisition of BPM signals.
- New system will use the same 63 BPMs and head amplifiers of the present orbit system.
- The aim is to measure complete orbits every 2.55 ms with a resolution of 0.1 mm.



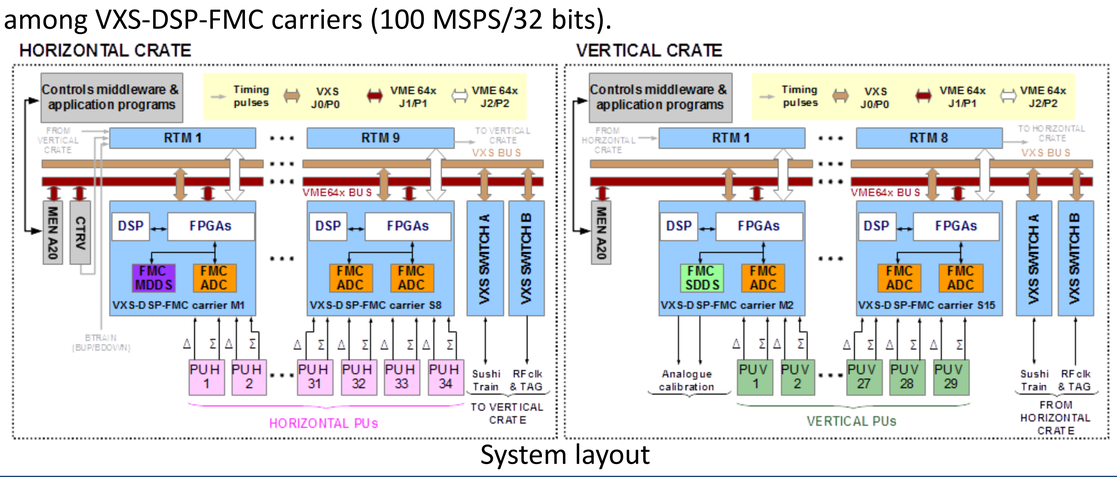

AD deceleration cycle

## FRONT-END ELECTRONICS

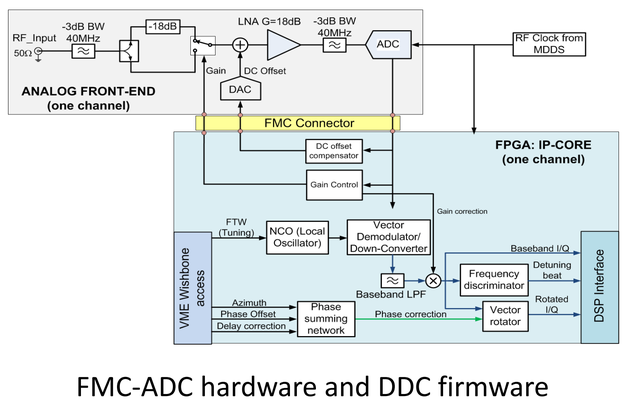
- **BPMs around the AD ring.**
  - 34 horizontal BPMs and 29 vertical electrostatic BPMs.
  - The sigma (Σ) signal is provided by a specific annular electrode.
  - The delta (Δ) signals are derived from two semi-sinusoidal electrodes.
  - BPM differential sensitivity of 0.1 µVp/mm.
- **Head amplifiers close to the BPMs.**
  - Differential Δ and Σ outputs.
  - Equivalent input noise of 0.6 nV/√Hz for the Δ inputs.
  - Feature a differential amplifier of 2 times 6 parallel Junction Field Effect Transistors (JFETs).
  - Δ outputs gain of 47dB. Bandwidth 10 kHz-20 MHz. CMRR better than 66 dB.
  - Calibration digital control signals to simulate maximum positive/negative beam displacement and centred beam.
- **Reception amplifiers close to the digital acquisition system.**
  - Differential inputs to single-ended Δ and Σ outputs.
  - Gain of 0 dB and bandwidth of 560 Hz-80 MHz.

## DIGITAL ACQUISITION SYSTEM

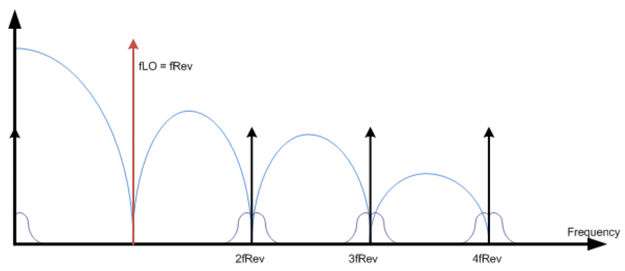
- Two VME-VXS crates with 17 VXS-DSP-FMC carriers.
- A timing module (CTRV) provides the triggers related to the AD cycle.
- Digitization of the BPM signals by 32 FMC-ADC boards.
- Generation of analogue calibration signals by a FMC-SDDS board.
- Common RF clock (programmable higher harmonic of $f_{REV}$) and a pulsed TAG signal ($f_{REV}$) synchronise all boards in the system.
- RF clock/TAG generation by a FMC-MDDS board from $f_{REV}$.
- M1 carrier DSP calculates $f_{REV}$ during the AD cycle from the value of the magnetic field (Btrain) of the main dipoles.
- VXS switch boards used to distribute the RF clock/TAG signal and for the communication among VXS-DSP-FMC carriers (100 MSPS/32 bits).




System layout




FMC-ADC hardware and DDC firmware




Digital down conversion principle

- Each VXS-DSP-FMC carrier accommodates a DSP (ADSP-21368) and two FPGAs.
- The DSP implements the core data treatment and overall system control. Three different DSP roles (M1, M2 and S1-S15).
- The Main FPGA (XC5VLX110T) implements the essential infrastructure for the system communication and data exchange.
- The FMC FPGA (XC5VSX95T) performs data processing such as the Digital Down Conversion (FMC-DDC) for the FMC-ADC.
- The DDC firmware converts the selected beam revolution harmonic into a baseband I/Q signal.

## ORBIT MEASUREMENTS

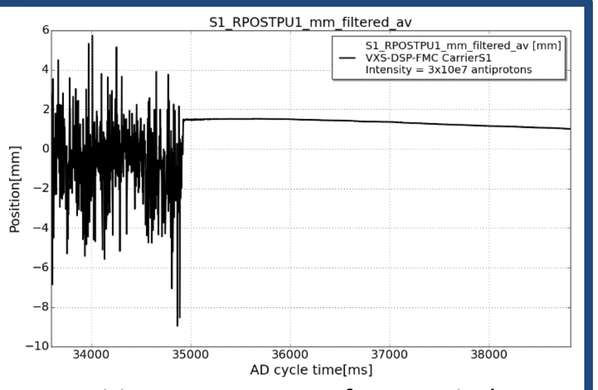
- The analogue front-ends will deliver RF difference and a sum signal for each BPM, i.e. 126 signals, which will be digitized and down converted to baseband.
- Depending on the level of RF induced EMI, the measurements will be carried out using the first or second harmonic of the bunched beam signal.
- After low pass filtering and decimation of the complex I/Q data the positions are calculated according to:

$$Pos(\mathrm{t}) = k \cdot \left( \frac{1}{\frac{\Delta}{\Sigma}_{cal}} \right) \cdot \left( \mathrm{Re}\left\{ \frac{I_\Delta(t) + jQ_\Delta(t)}{I_\Sigma(t) + jQ_\Sigma(t)} \right\} - \frac{\Delta}{\Sigma}_{zero} \right) + BPM_{off}.$$

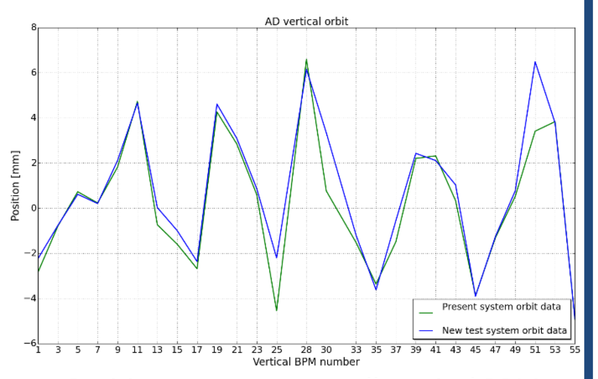
- The digital acquisition system includes a calibration procedure to obtain the calibration parameters required to calculate the position ($\Delta/\Sigma_{cal}$ and $\Delta/\Sigma_{zero}$) .

## SYSTEM STATUS AND TESTS

- Most of the hardware required for the system is already produced, tested and installed.
- New AC-coupled low-noise version of the FMC-ADC board under development (noise density level below 10 nV/√Hz).
- DSP firmware for each VXS-DSP-FMC carrier is already developed.
- FPGA firmware upgraded to allow communication of up to 32 VXS-DSP-FMC carriers via the VXS.
- The specifications for the software have been written and the final software is currently being developed.
- A prototype version of the system is currently being tested in AD with beam.
  - A VXS-VME crate holding the M1 carrier, the M2 carrier, another six (S1-S6) slave carriers and a CTRV timing module.
  - The aim is to acquire data from all vertical BPMs and test all the features of the final system in real conditions.
- A position signal with a resolution better than 0.1 mm is obtained during the first flat top/deceleration ramp in the AD cycle (from 35 s onwards) corresponding to the time when the beam is bunched.
- A position measurement for the vertical plane of all BPMs during the first flat top (37.72 s) has been acquired (blue line) and agrees with the measurement from the current orbit system (green line).
- The discrepancies between the two systems are currently being investigated.




Position measurement for a vertical BPM




Position measurement all vertical BPMs

## CONCLUSIONS

The design of the new orbit system for AD has been presented. It will use the same 63 BPMs and the head amplifiers than the current orbit system. A new digital acquisition system based on in-house developed hardware will digitize and process the BPM signals to obtain an orbit measurement with a resolution of 0.1 mm every 2.55 ms. The 17 VXS-DSP-FMC carriers and the 34 FMC daughter boards used will be accommodated in two VME-VXS crates for acquiring the horizontal and the vertical BPM signals. The majority of the hardware is already produced and tested, with a new low noise FMC-ADC board under development. Tests with a prototype version of the final orbit system are currently being carried out with beam in the AD, with the final orbit system foreseen to be commissioned by the end of 2015.