OVERVIEW OF APPLICATIONS AND SYNERGIES OF A GENERIC FPGA-BASED BEAM DIAGNOSTICS ELECTRONICS PLATFORM AT SwissFEL

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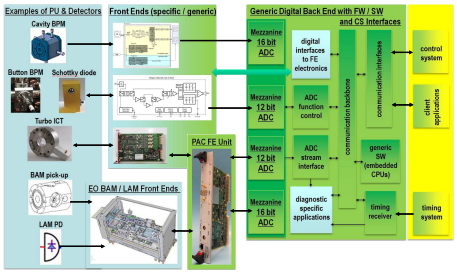
Abstract

For SwissFEL electron beam diagnostics we combine application-specific detectors and front-end electronics with a common solution for digitization, interfacing and FPGA-based digital signal processing. Many key components and standards we use were initially developed by PSI for the European XFEL BPM system, but are equally suited for a broad range of SwissFEL diagnostics systems with little or no modifications. Examples are the FPGA signal processing hardware and firmware/software, ADC and DAC boards, interface boards or peak detection front-end electronics. By following a modular generic hardware and firmware/software design approach, we can cover a larger number of different monitor types with moderate development effort. Applications of our generic platform include BPMs, bunch length monitors, beam arrival time monitors, beam loss monitors. This paper gives an overview of the design, present and future applications of our generic platform, discussing the synergies and differences of the required hardware, firmware and embedded software solutions.

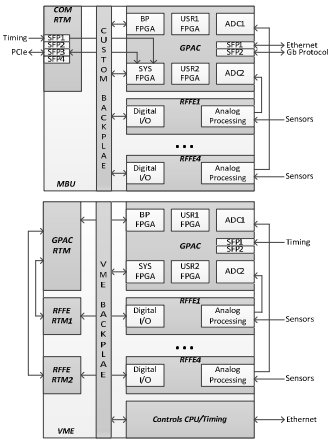
Overview of the Hardware and Software Platform

In a SwissFEL diagnostic systems the detector signals are connected to front-end electronic cards (RFFE). Due to various nature of detector signals there are dedicated RFFEs as well as generic PAC board with dedicated mezzanine cards for analogue signal processing and conditioning. The analogue signals are digitized by ADC cards. Currently two types of ADC cards cover all diagnostics applications. The data from ADCs are processed digitally in FPGA firmware and embedded CPUs. The processed data is read by control systems over communication interfaces.



The generic FPGA-based diagnostics platform is a composition of modular hardware components and generic firmware and software which is common for all diagnostics applications. The generic firmware provides unified interfaces to ADC data and communication interfaces. The embedded CPUs run software for data processing, debugging, maintenance of the systems.

Hardware configuration variants

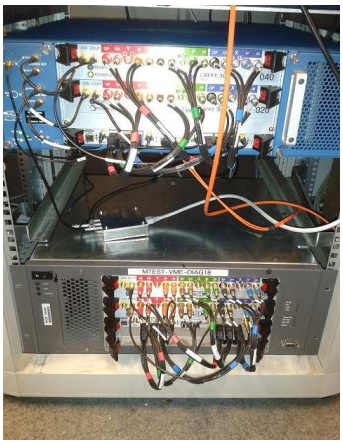


MBU

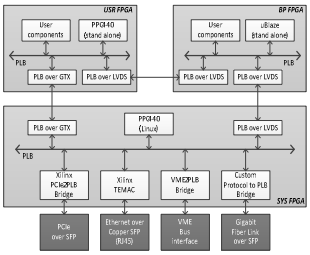
- Stand-alone solution for distributed systems
- Communicates with control system over PLB bridge or PCIe
- Links to RFFEs included in the custom backplane
- Communication transition card (COM RMT) for additional interfaces

VME Crate

- Complete VMEbus based solution
- Includes controls CPU and timing receiver
- Communication with control system over VME
- Many GPACs and RFFEs in a single crate
- Needs dedicated transision modules for communication with RFFEs

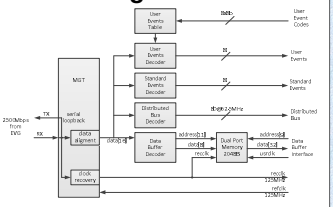


GPAC Communication Infrastructure



- Each FPGA has embedded system with PowerPC or uBlaze CPU and is built around Processor Local Bus
- All FPGA chips are connected by PLB to PLB bridge with two types of physical layers: RocktetIO or LVDS lines
- The PLB to PLB bridge is transparent and maps part of address space from one system to the other
- There are four types of external interfaces for communication with control system

SwissFEL Embedded Timing Receiver



- Used in stand-alone system where hardware timing receiver is not present
- Connected to timing system by fibre optic link
- Decodes timing events and generates configurable triggers for local electronics
- Clock recovery from serial data stream and synthesis of local clocks
- Receives 2048B buffer with machine parameters
- Regenerates distributed bus signals

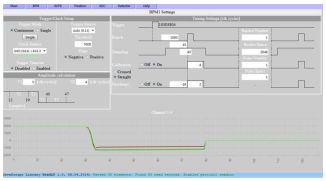
Linux Based Generic Software

Xilinx PetaLinux distribution running on PowerPC in SYS FPGA on GPAC and it provides:

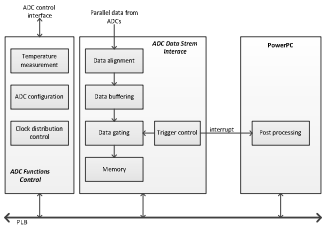
- File transfer protocol for remote firmware updates
- Configuration, test and debug software
- Universal web server for user applications

Web server:

- Generic JavaScript library for embedding user data in the web page, special string in property title of any HTML tag is used
- Automatic waveform plots
- New HTML web page created without changing the web server



ADC Based Oscilloscope



- ADC data stream interfaces deals with ADC specific interface, aligns data to single clock, buffers pre-trigger samples, and provides unified stream interface to user applications
- Trigger modes: single, auto, normal, external
- The ADC data is stored in dual port memory for post processing
- ADC functions control provides board specific configuration settings
- The software in PowerPC calculates standard waveform parameters such as min, max, mean, standard deviation, etc.

Applications

The above described digital platform is a base for application specific extensions. If the diagnostic application deploys specific front-end electronics, the developer has to prepare in firmware RFFE specific control components. The firmware library of the digital platform already provides basic VHDL components for typically implemented interfaces such as I^2C, UART, SPI, and1-Wire. In next step the developer implements applications specific ADC data processing. Depending on the latency requirements this can be done either in VHDL or in software in PowerPC. The digital platform is base for the following digital applications being under development: Beam Position Measurement (BPM), Beam Loss Monitors (BLM), Bunch Compression Monitor (BCM), Bunch Arrival Monitor (BAM).

Conclusion

The FPGA based digital platform besides common hardware has common firmware and software platform for all diagnostics applications. Deploying of the common firmware/software as a base for specific applications significantly reduces the development effort. The digital platform has been already deployed in various digital applications for SwissFEL which are under development.