

# TIME MEASUREMENT METHOD BASED ON CPLD FOR BEAM LOSS POSITION MONITOR\*

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## Abstract

Beam loss position is of great concern at SSRF. Time measurement is one of the key technologies for beam loss position monitor. This paper introduces a time measurement method based on Complex Programmable Logic Device (CPLD). Simulation has been done to verify the performance of this method.

## INTRODUCTION

SSRF is the 3.5GeV electron storage ring facility operated at the Pudong New District of Shanghai. During accelerator operation ionising radiation is detected outside the vacuum chamber, mainly caused by electromagnetic cascades, generated by beam loss electrons hitting the chamber. The total dose is predominantly located at only a few positions of the storage ring, especially at the position of transverse feedback system [1-3]. Optical fiber radiation dosimetry from Cherenkov principle offers the possibility to measure the position of beam loss.

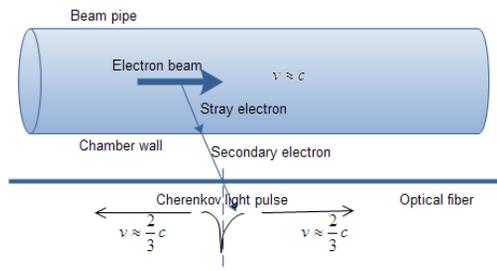


Figure 1: Beam loss position measuring principle.

Figure 1 shows the measuring principle. If some stray electron impact at the vacuum chamber, secondary electron will be excite. The movement of those secondary electron in the optical fiber will bring Cherenkov light pulse. The refractive index of optical fiber (quartz) is 1.5. So the speed of the light pulse in the optical fiber is  $0.6666c$ , where  $c$  is the speed of light in vacuum. The Cherenkov light pulse will transmit along the fiber to the both ends [4,5]. The position of the original light pulse can be calculated from the time difference of the light pulse reaching between both ends.

Figure 2 shows an available measurement scheme. The PMT transforms the light pulse to electrical signal, high speed data acquisition card obtains the waveform, and then IOC calculates the time difference by complicated time orientation algorithm from PMT waveform. To

measure time accurately, the data acquisition card must be high speed and has enough effective number bits [6,7].

This paper introduces a direct time measurement method to replace the high performance data acquisition card and IOC calculator algorithm.

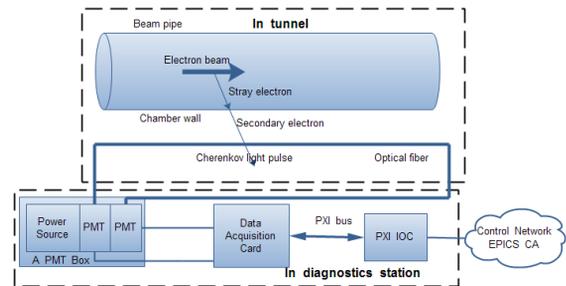


Figure 2: An available measurement scheme for beam loss position.

## ARCHITECTURE

In the general purpose CPLD from Altera, there are many dedicated carry lines, which connect adjacent basic logic elements. These dedicated carry lines are normally used to form dedicated carry chains to implement arithmetic functions such as fast adders, counters, and comparators. The delay of each carry line is short and can be considered fixed for a particular physical technology, rail voltage, and temperature range. Using these carry lines as delay cells, a high-resolution time measurement equipment can be implemented in an CPLD [8].

To verify our idea of time interpolation within one clock period using dedicated carry lines, a time measurement equipment based on counter and time interpolation methods was implemented in an CPLD. The block diagram of the time measurement equipment is shown in Figure 3.

### Fine Time Measurement

One of the simplest forms used to combine the dedicated carry lines into a carry chain is a multibit adder [9]. The Boolean equations of each adder cell are:

$$Sum = A \oplus B \oplus Ci$$

$$Co = AB + (A + B)Ci$$

where  $A$  and  $B$  are inputs for the adder,  $Ci$  is a carry-in bit,  $Co$  is a carry-out bit, and  $Sum$  is a sum bit.

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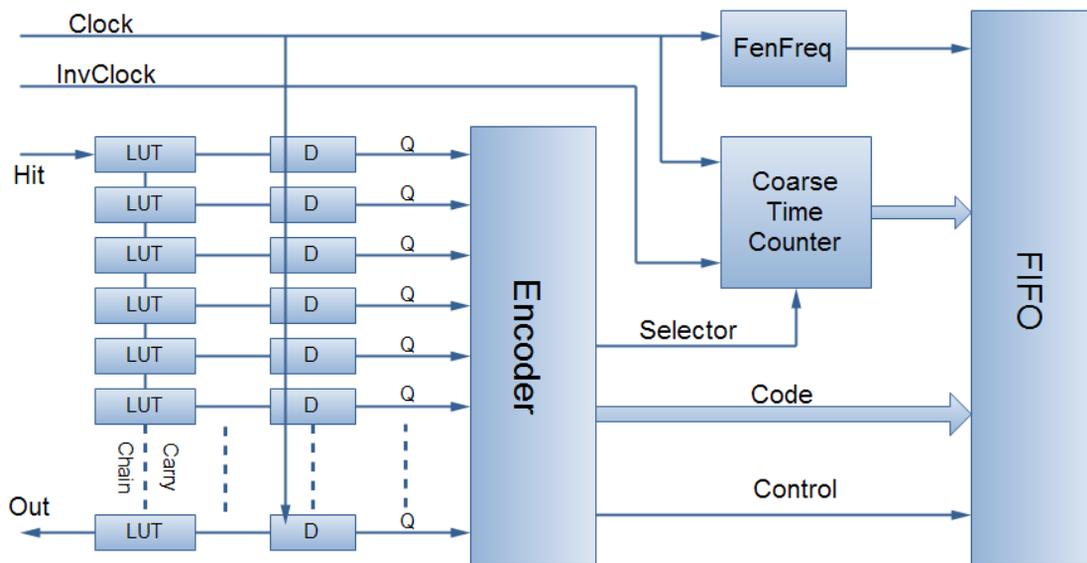


Figure 3: Block diagram of the time measurement equipment.

The delay time of the whole chain must be longer than one period of the system clock. We set all A to logic one and all B except the least significant bit (LSB) to logic zero. The LSB of B is the hit signal. If there is no hit signal, all Sum would be logic one. When there is a hit signal, each bit of the sum, from the LSB to the most significant bit (MSB), will change to logic zero step by step. The changed bits indicate the elapsed time of the hit signal passing along the carry chain. At the next rising edge of the system clock the sum bits will be latched. This is the fine time measurement in a thermometer code.

While trying to latch the adder's output bits at the rising edge of the system clock, we use dual synchronizers to reduce the probability of metastability. There are many kinds of conversion schemes to convert a thermometer code to a natural binary code for the fine time measurement. The binary-search encoder is chosen for its simplicity and easy implementation.

In the fine time measurement, it is very important to keep a uniform delay between the bits of the sum to the input of their corresponding register. A basic logic element that contains a look-up table (LUT) and a programmable register is used to form the 1-bit adder which generates the sum bit and the register for latching the sum bit. In addition, constraints must be set in the design tool and sometimes logic cells must be placed manually.

### Coarse Time Counter

A synchronous counter is designed to realize the coarse time measurement. The counter may change its state while the hit arrives. To avoid ambiguous states, two Gray-code counters running at the system clock rate (one in phase and another out of phase) are used. Depending on the phase of the system clock at the arrival moment of the hit signal, one of the two counter's outputs is selected

and encoded with a binary code as the coarse time measurement code. If the hit arrives in the first half ( $0\sim\pi$ ) of the system clock period, the output of the 'in phase' counter is selected. Otherwise the output of the 'out of phase' counter is selected. The result of the fine time measurement reflects the phase of the system clock. Using the result of the fine time measurement, a stable coarse time count value is always obtained.

### Read-Out Buffer

The result of the complete time measurement (the fine time and the coarse time measurement) is written into a first-in first-out (FIFO) buffer along with a channel identifier. The total time measurement can be expressed as follows:

$$T_{out} = T_{coarse} + T_{fine} = T_{sys} * N_c + T_{bin} * N_e$$

Where  $T_{out}$  is the result of the complete time measurement,  $T_{coarse}$  is the result of the coarse time measurement,  $T_{fine}$  is the result of the fine time measurement,  $T_{sys}$  is the period of the system clock,  $N_c$  is the coarse time measurement code,  $T_{bin}$  is the bin size (the LSB value) of the fine time measurement, and  $N_e$  is the fine time measurement code.

## SIMULATION RESULT

The delay time of a dedicated carry line is different in CPLD's from different series, capacity and speed-grade. An EPM1270T144C5N MAX II CPLD device from Altera was selected to implement this time measurement equipment design.

Figure 4 shows the simulation result. The horizontal ordinate is the input relative delay time and the vertical ordinate is the code from the read-out buffer in CPLD. The slope of the fit curve is 8.8403. And so the resolution of this time measurement equipment design is 113.1ps.

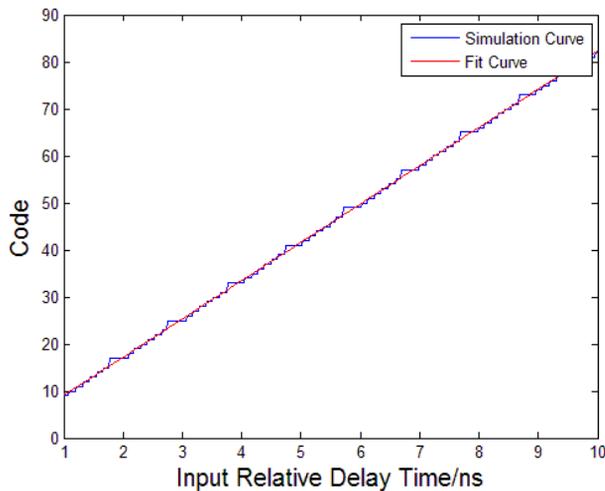


Figure 4: Simulation result and the resolution of this time measurement equipment design is 113.1ps.

## CONCLUSION

To monitor the beam loss position in SSRF, a high-resolution time measurement equipment implemented in a general purpose Complex Programmable Logic Device (CPLD) is presented. Dedicated carry lines of an CPLD are used as delay cells to perform time interpolation within the system clock period and to realize the fine time measurement. Two Gray-code counters, working on in-phase and out-of-phase system clocks respectively, are designed to get the stable value of the coarse time measurement. The fine time code and the coarse time counter value are then written into a first-in first-out

(FIFO) buffer. Simulation has been done to verify the performance of the equipment design. The resolution is better than 120ps.

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