Status of the Sirius RF BPM Electronics IBIC2014, Monterey

Sérgio Rodrigo Marques

(on behalf of the beam diagnostics group)

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Brazilian Center for Research
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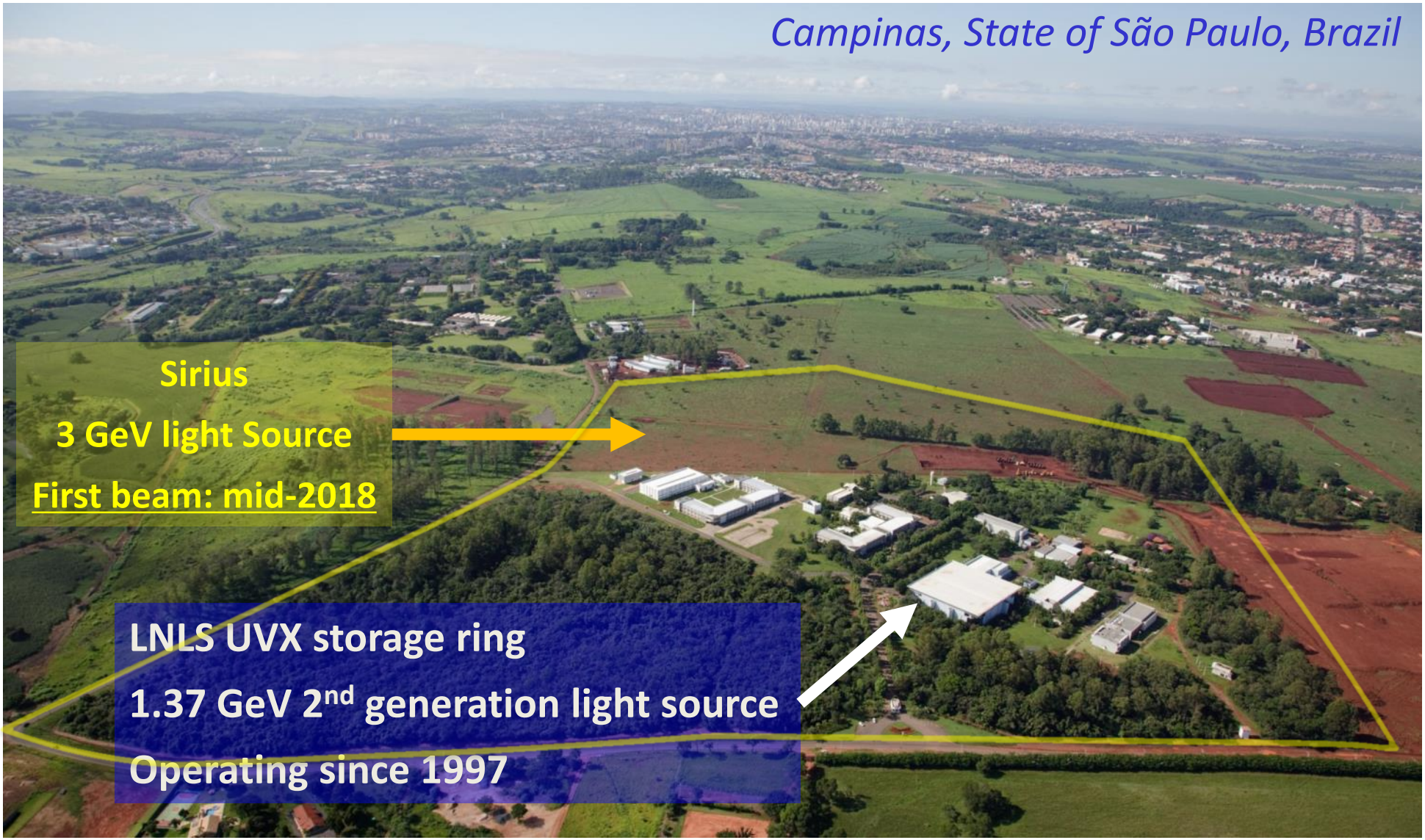
Outline

- Introduction
- Stability Requirements
- General System Requirements
- FOFB Strategy
- Hardware Overview
- Performance Tests: Laboratory Bench
- Performance Tests: SPEAR3 Beam (SLAC/SSRL)
- Final Remarks

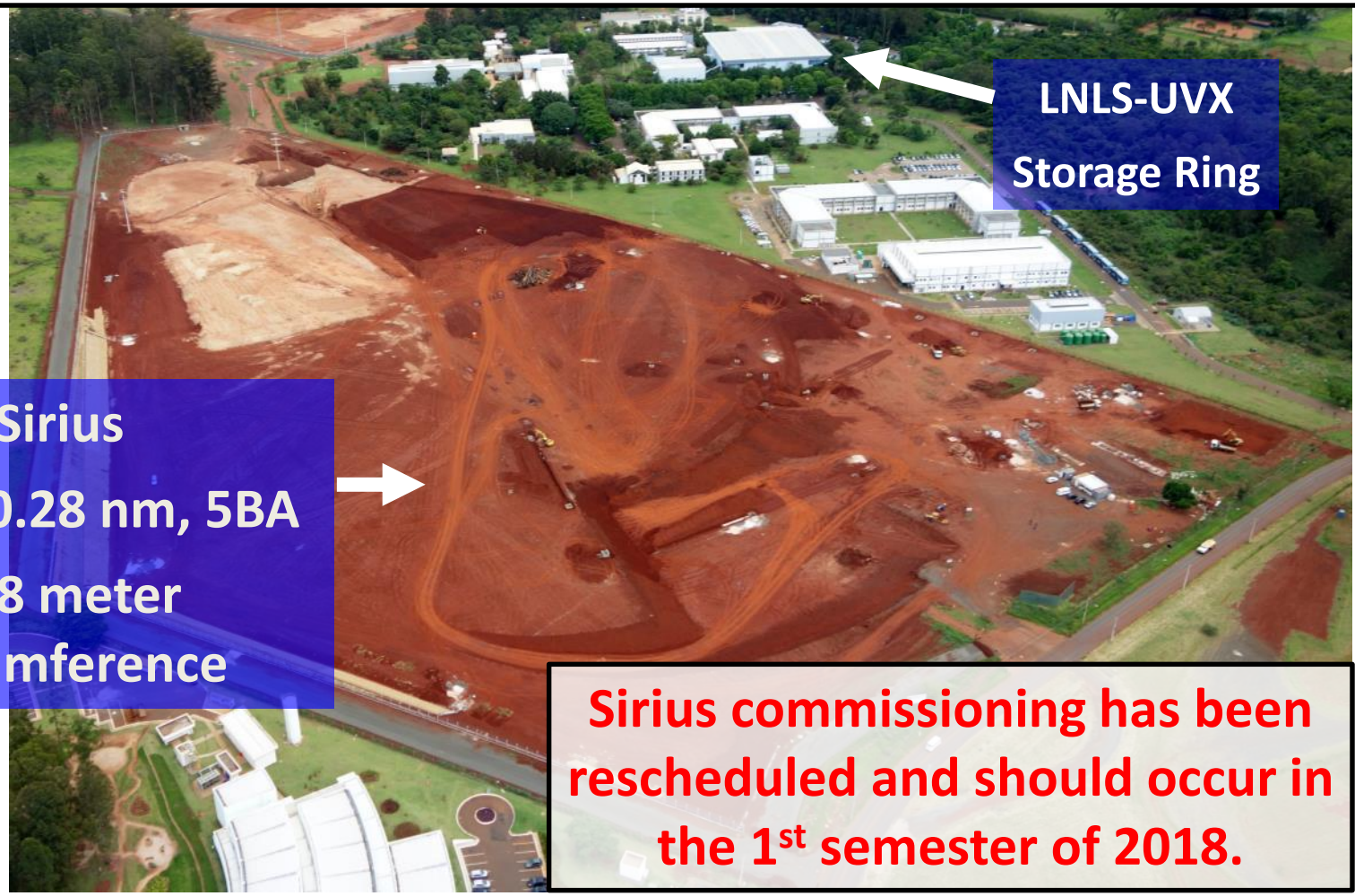
Introduction



Brazilian Center for Research in Energy and Materials

Introduction

Picture – December 2013
March 2014: Earthwork finalized
October 2014: Construction companies selection



Sirius commissioning has been rescheduled and should occur in the 1st semester of 2018.

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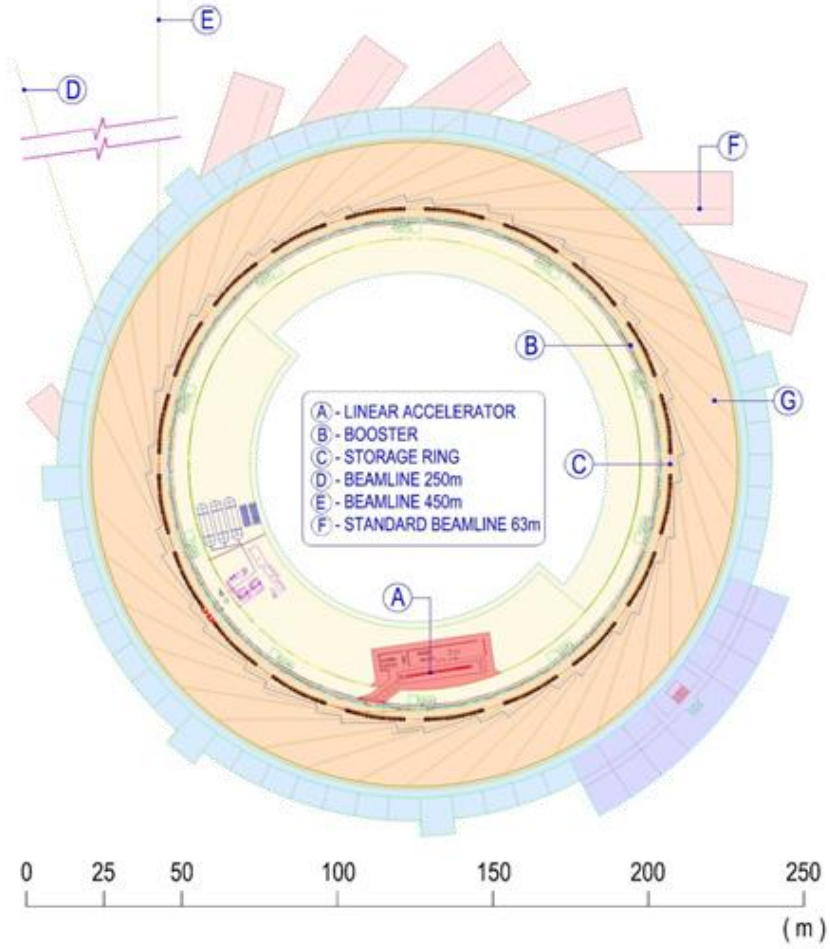
Stability Requirements

Requirements for Sirius RF BPM electronics

Requirements of Sirius RF BPM electronics.

Parameter	Value	
Resolution (RMS) @ 0.1 Hz to 1 kHz	< 80 nm	
Resolution (RMS) @ turn-by-turn full bandwidth	< 3 μm	
1 hour position stability (RMS)	< 0.14 μm	*
1 week stability (RMS)	< 5 μm	
Beam current dependence (decay mode)	< 1 μm	*
Beam current dependence (top-up mode)	< 0.14 μm	*
Filling pattern dependence	< 5 μm	



Energy: 3GeV

Natural emittance: 0.28 nm.rad

RF frequency: ~500 MHz

Natural bunch length: ~ 8.8 ps

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General System Requirements

- Electron and photon **beam position monitoring** from accelerator's control system
- Storage ring **Fast Orbit Feedback** control: stabilizes beam orbit at sub-micron level
- **Orbit interlock:** prevents machine from damage due to mis-steered high power photon beams
- Machine studies: **turn-by-turn readouts** provide valuable information of machine behavior
- Failure diagnostics: beam loss analysis (**post-mortem**)
- General **diagnostics**

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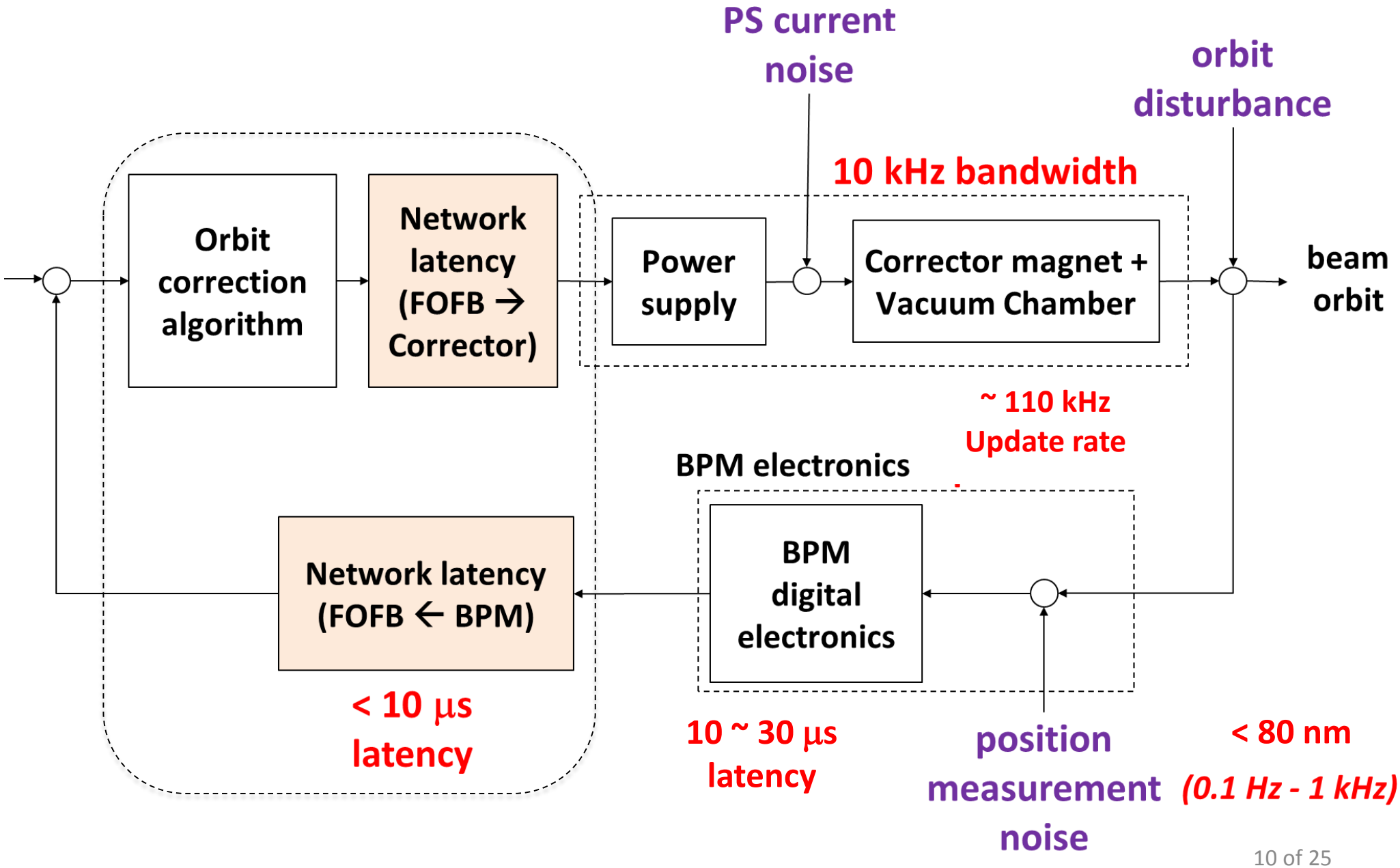
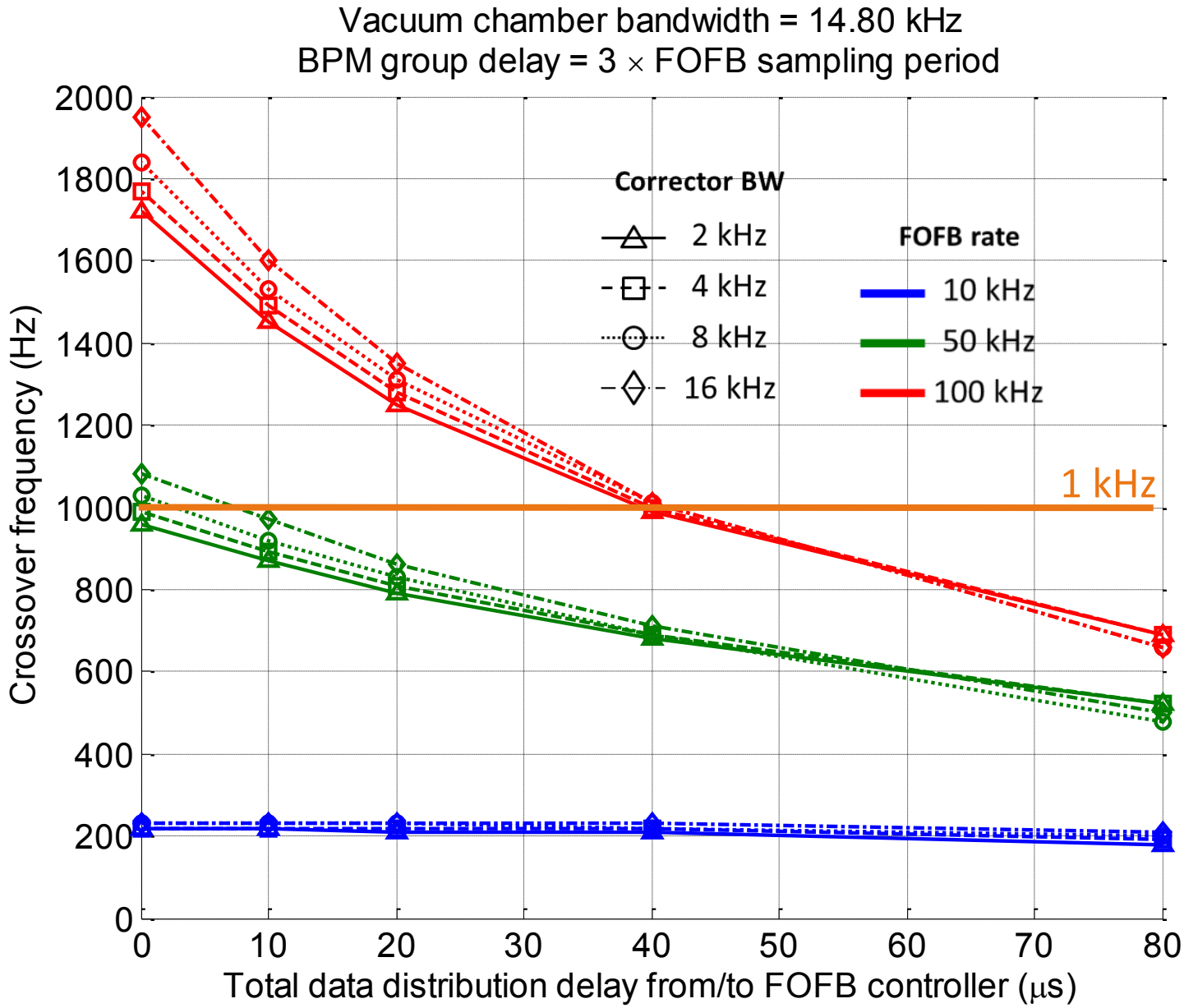
FOFB Strategy



FOFB Strategy



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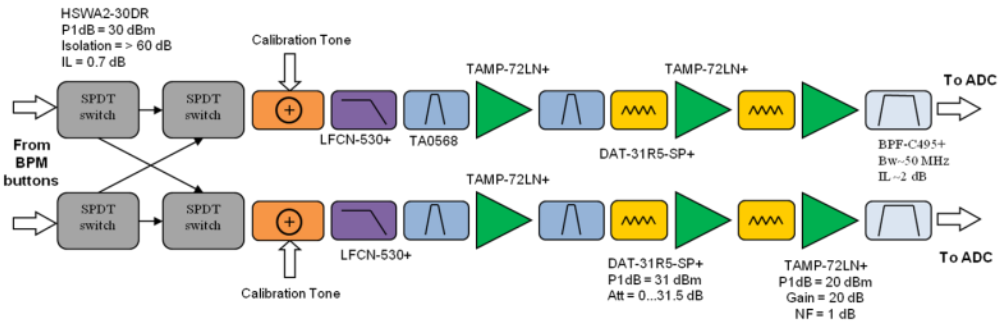
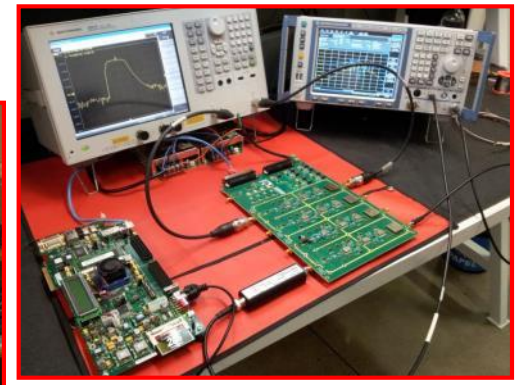
Hardware Overview

RFFE v1 (block diagram and tests)

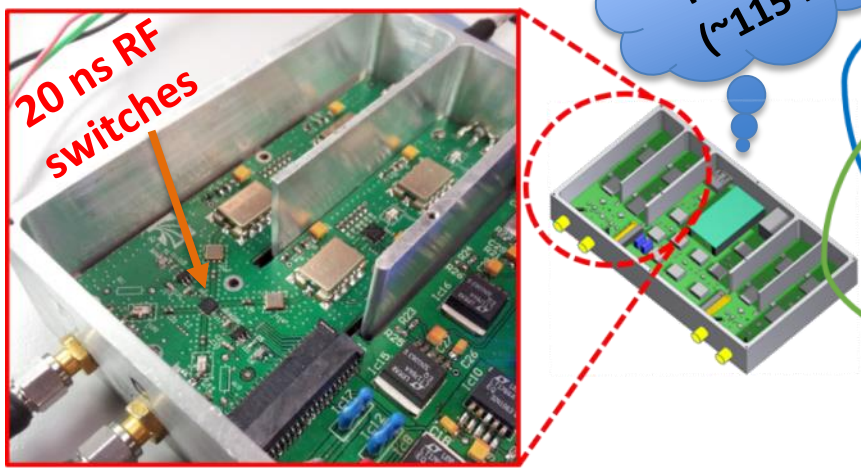




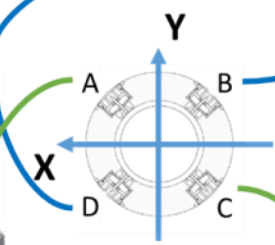
B. Keil et al., "Development of New BPM Electronics for the Swiss Light Source, IBIC' 2012

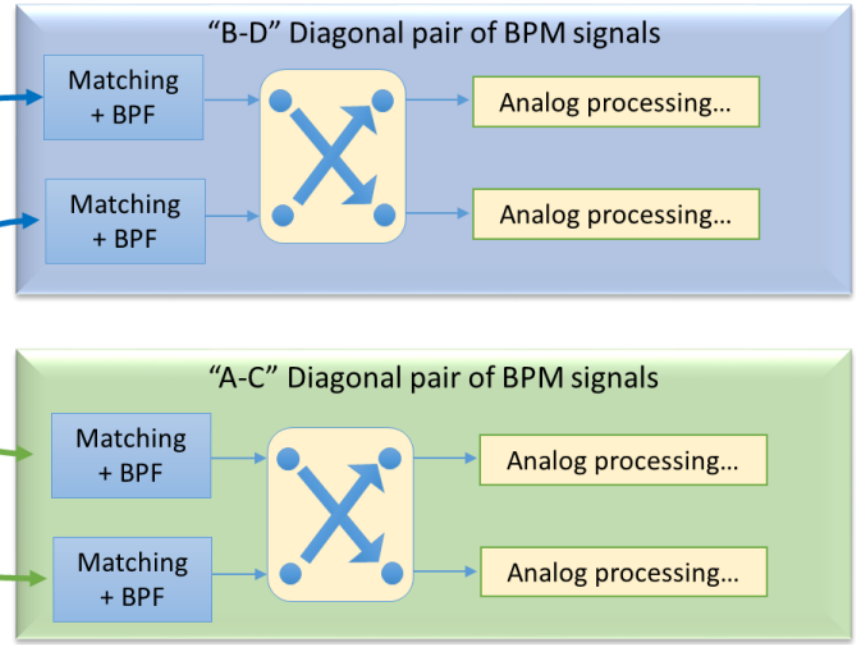
R. Biscardi, J. W. Bittner, "Switched Detector for Beam Position Monitor", PAC'1989

RFFE v2: (diagonal channels)



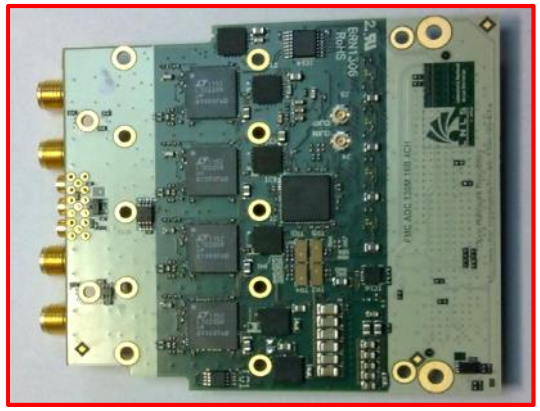
Switching @ FOFB rate (~115 kHz)

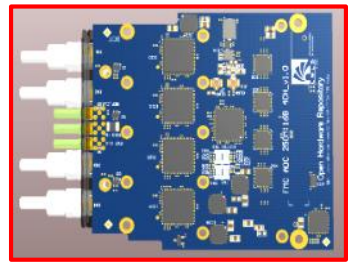


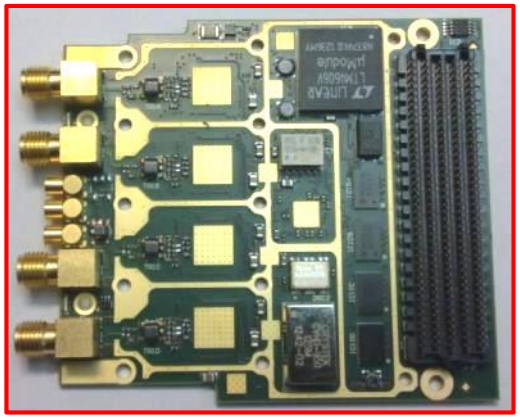


Hardware Overview

FMC standard 130 MSP/s 16-bit ADC board



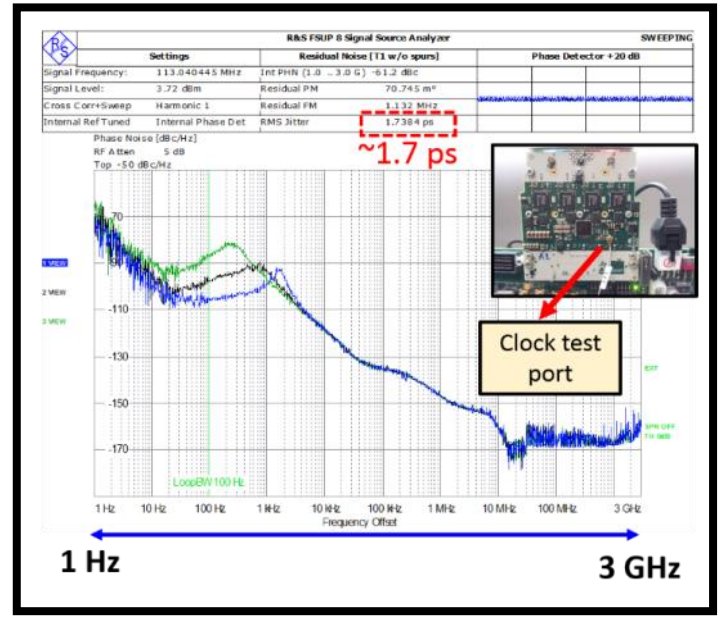




Optimized for undersampling

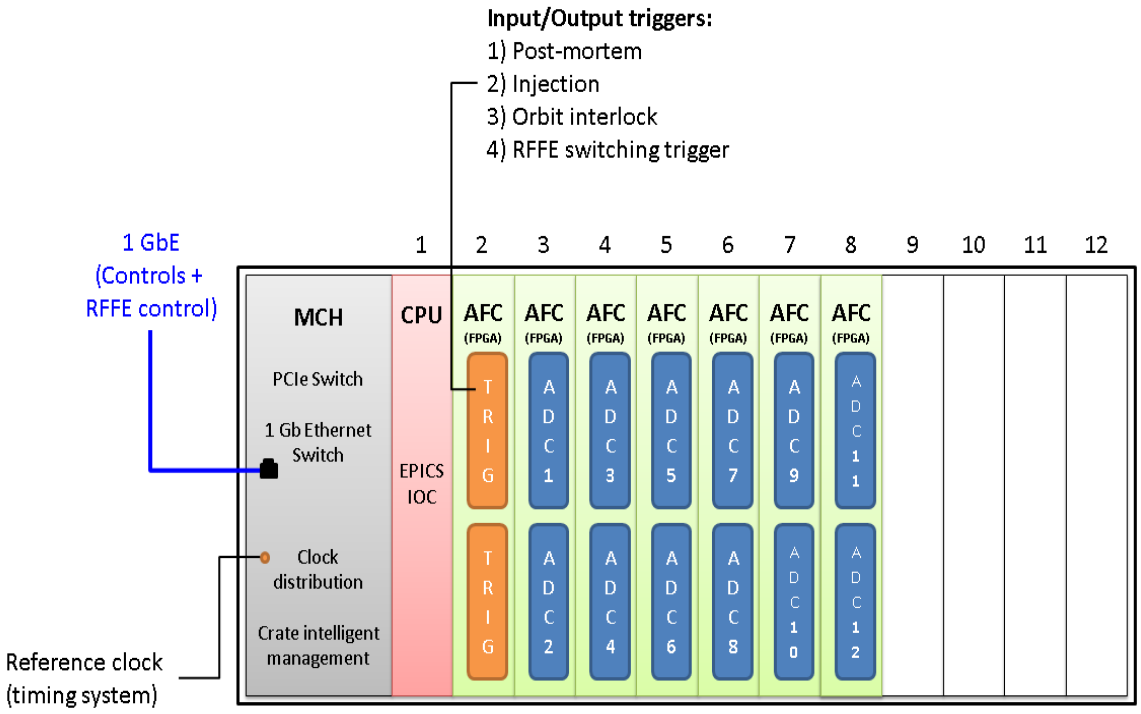
"Standard" features

- External clock input
- Adjustable oscillator's frequency for internal clock
- FMC standard (FPGA Mezzanine Card)



PLL tuning for internal clock

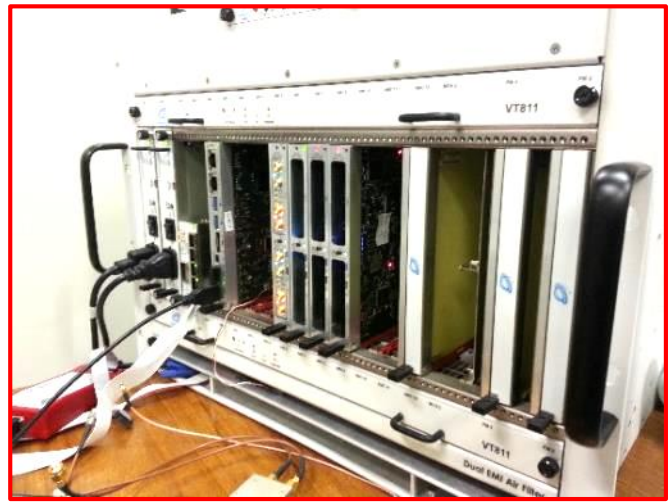
Hardware Overview



More info online at:

6th meeting of the xTCA interest group
"A MicroTCA system for Sirius BPM"
Daniel Tavares (LNLS)

Commercial crate



Designed by Warsaw University of Technology (WUT) for LNLS

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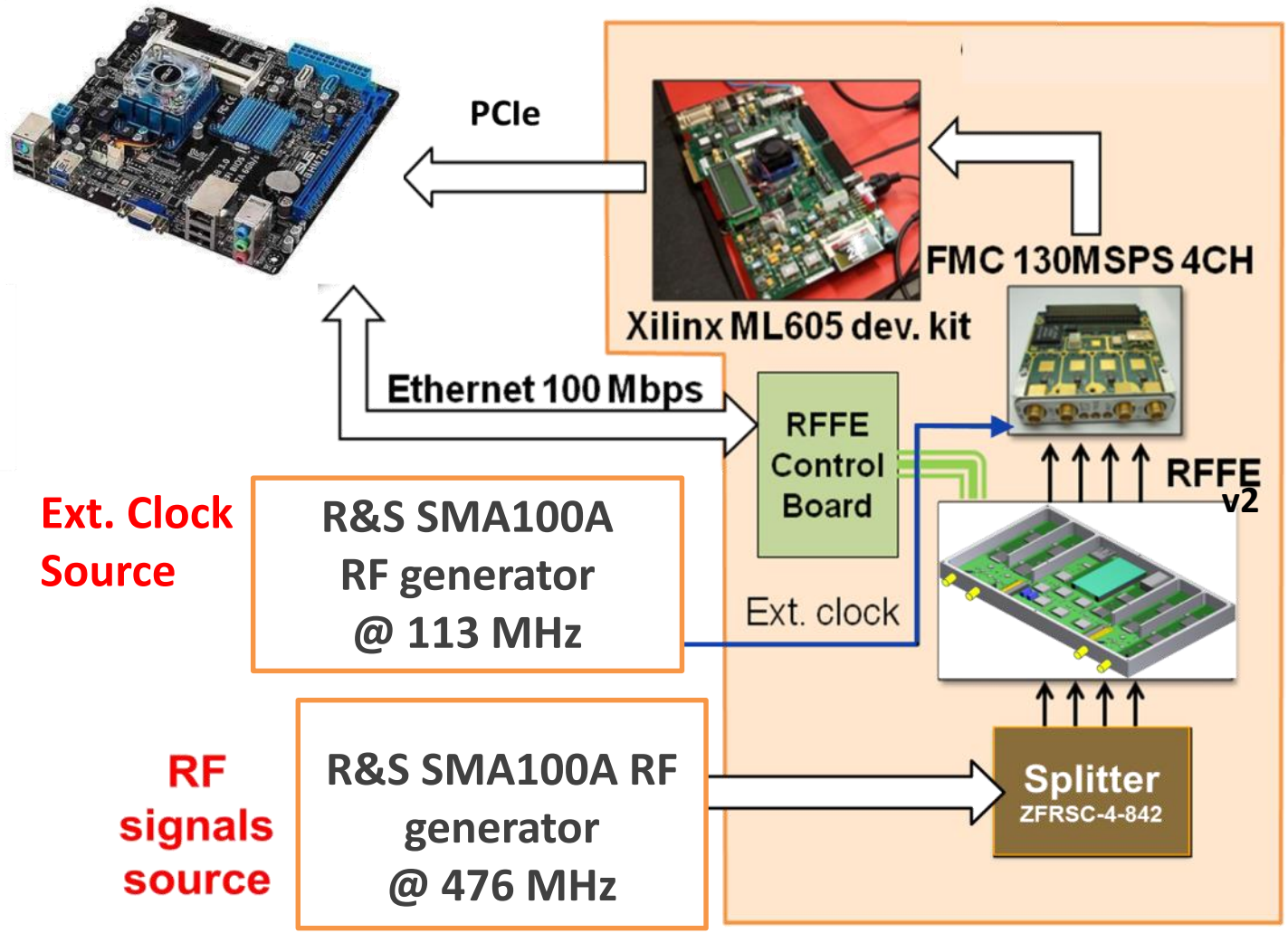
Performance Tests: Bench

Block diagram of the setup used for the BPM electronics test



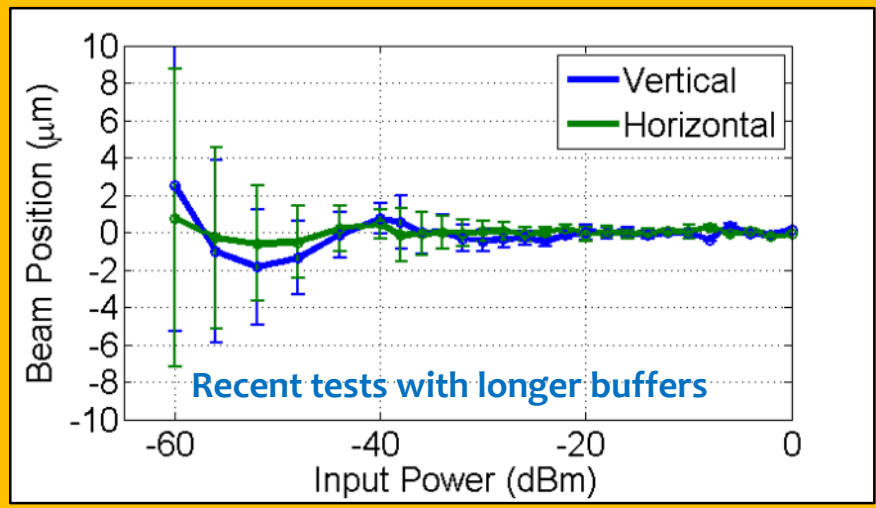
ADC clock / RF signals freq.:

UVX: 476 / 113 MHz
Sirius: 500/ 117 MHz

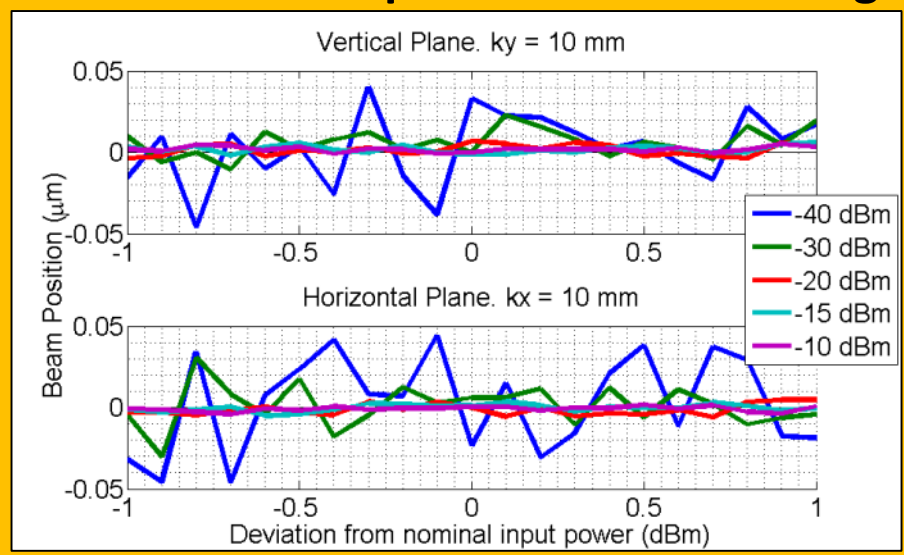
BPM geometric factor:
$K = 10$ mm

Performance Tests: Bench

Beam Current Dependence – long range

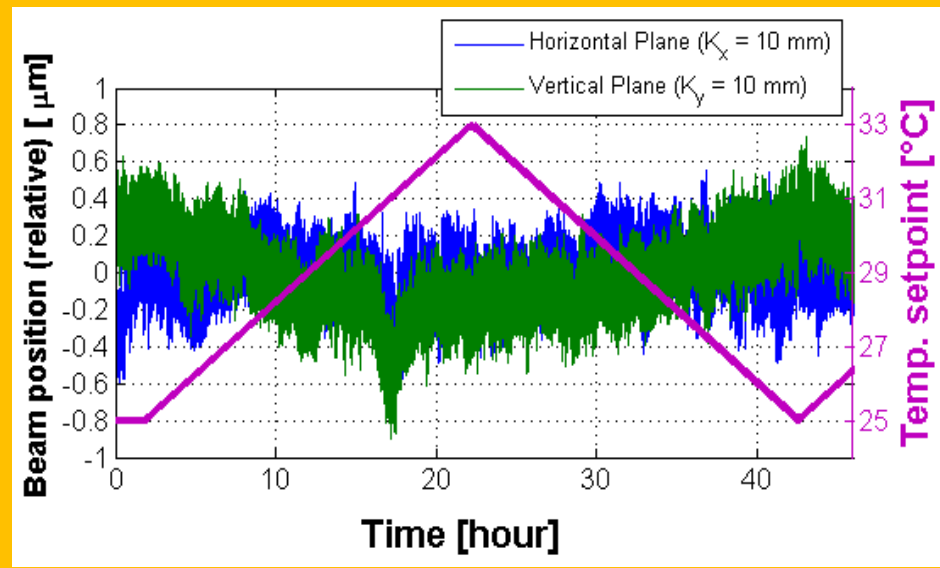


Beam Current Dependence – short range



IBIC'2013 (MOPC09)

The temperature dependence was kept below 140 nm under a 8 C degrees temperature variation.



~2 days test

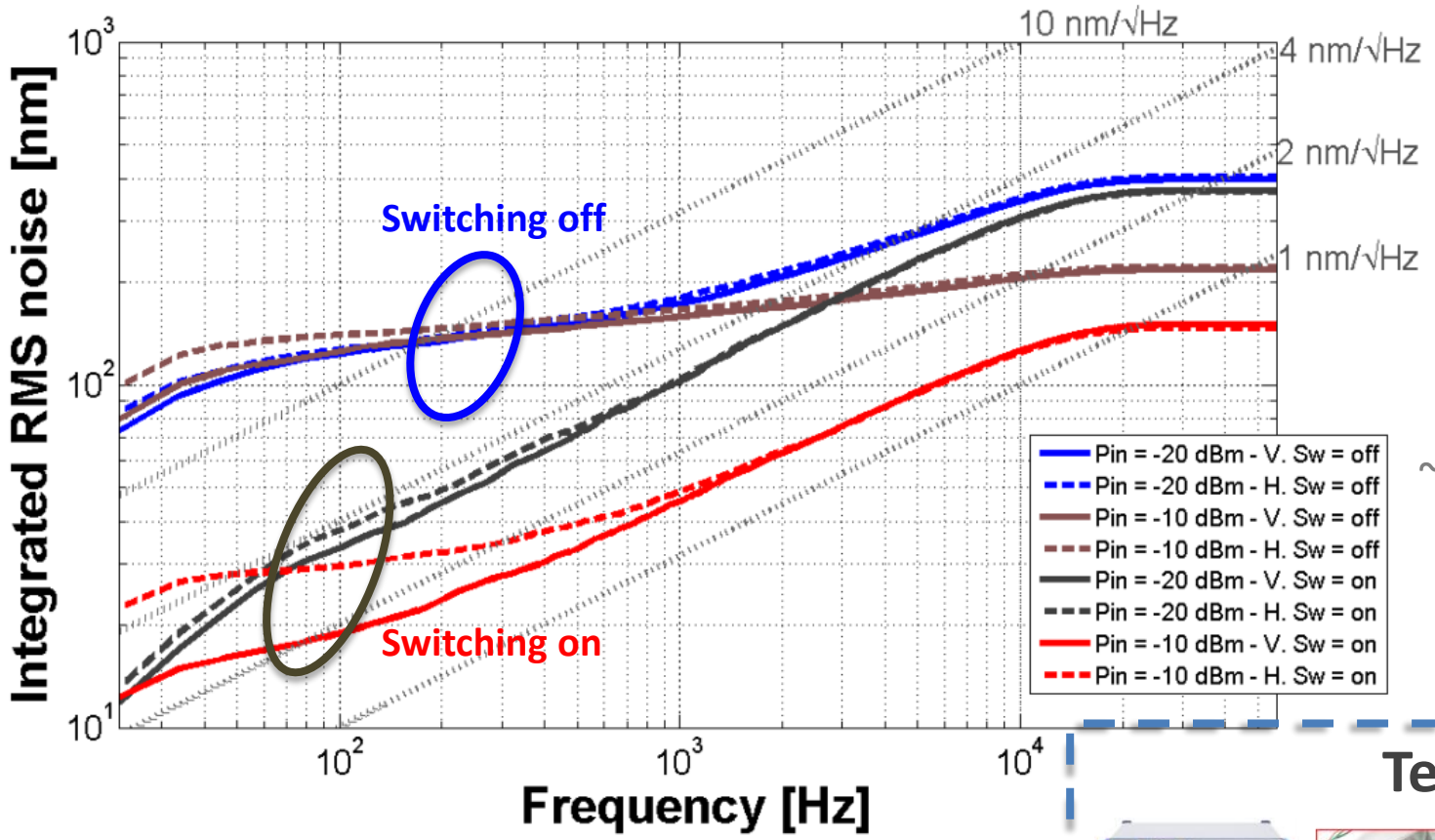
RMS X, Y < 140 nm

Data rate: ~10 Hz

Bandwidth: ~2 Hz

Performance Tests: Bench

Diagonal switching scheme virtually eliminates electronic noise originated in the RF chain downstream of the switches up to a certain frequency...

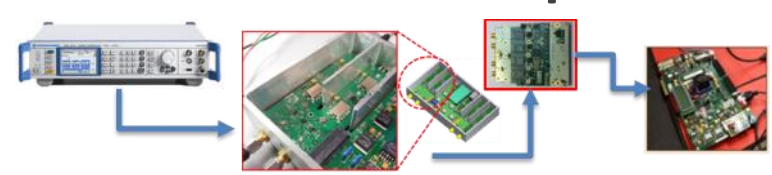


-10 dBm ~ 500 mA
-20 dBm ~ 160 mA

Switching frequency
~ 110 kHz (complete cycle)

Compare
Red vs Brown and/or
Blue vs Black

Test setup

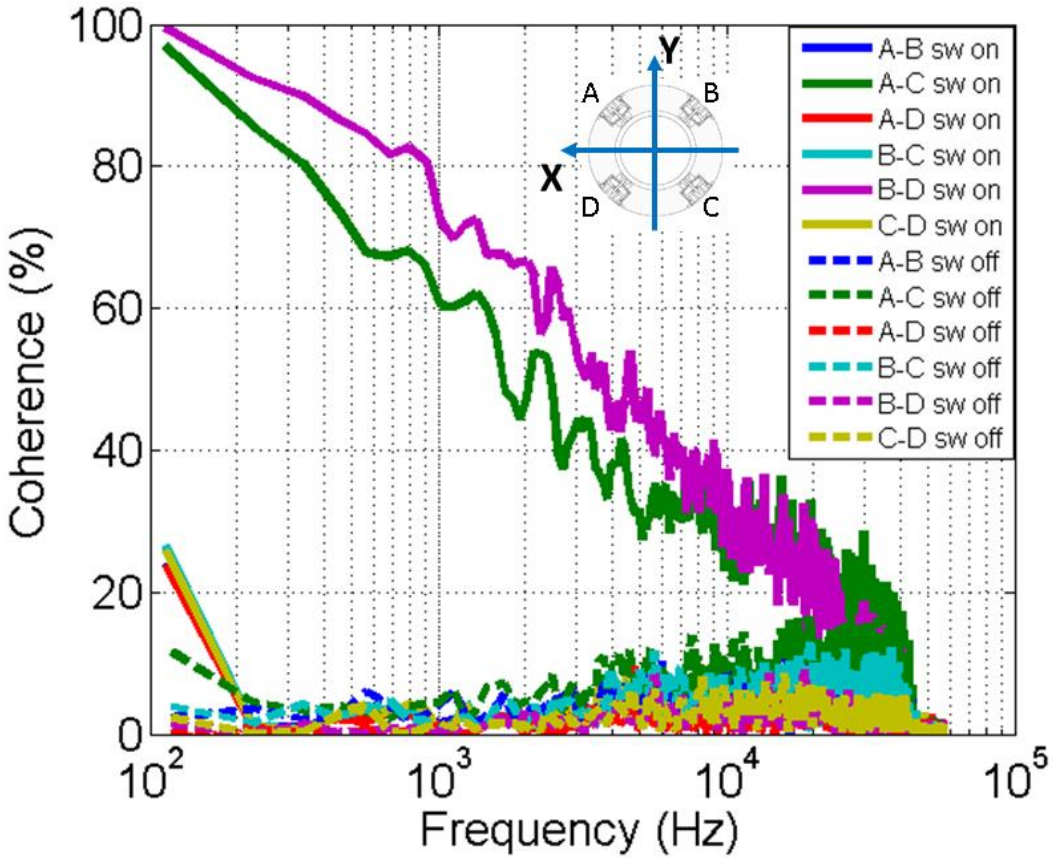


RF generator > RFFE v2 > 130 MSP/s ADC > FPGA kit

Performance Tests: Bench

The switching scheme introduces coherence between the diagonal channel pairs (A-C and B-D) from DC to approximately 40 kHz.

$$C_{xy}(f) = \frac{|P_{xy}(f)|^2}{P_{xx}(f)P_{yy}(f)}$$



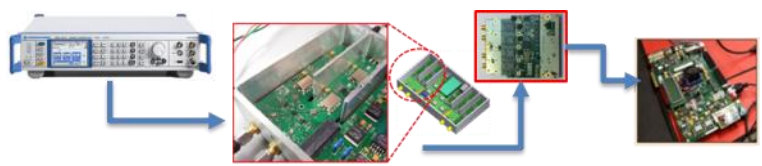
Switching @ ~ 110 kHz

Low frequency range:
High coherence (DC-100 Hz)

Medium frequency range:
Decreasing coherence
(100 Hz - 40 kHz)

High frequency range:
No coherence
(40 kHz - few GHz)

Test setup



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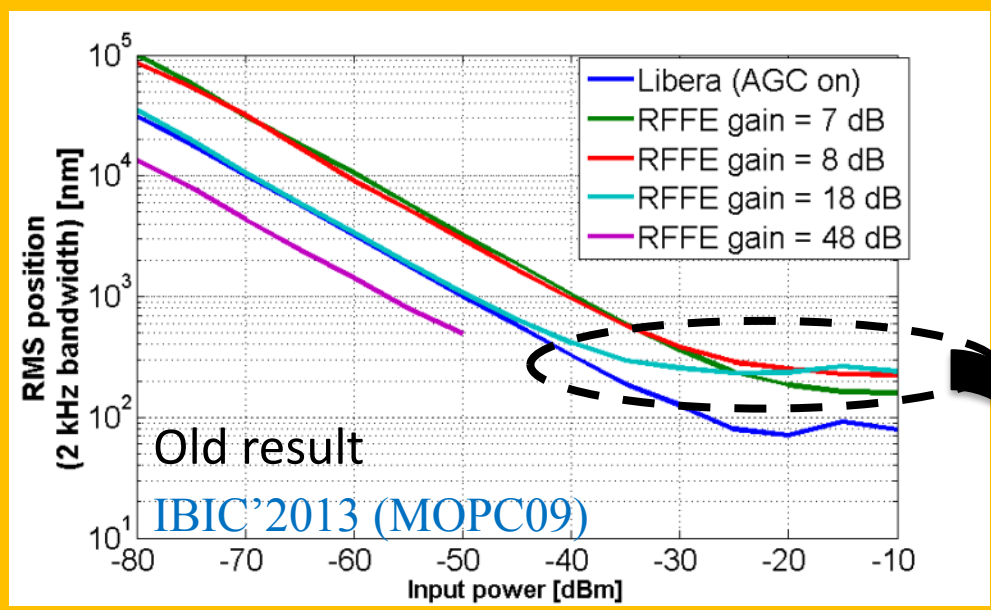
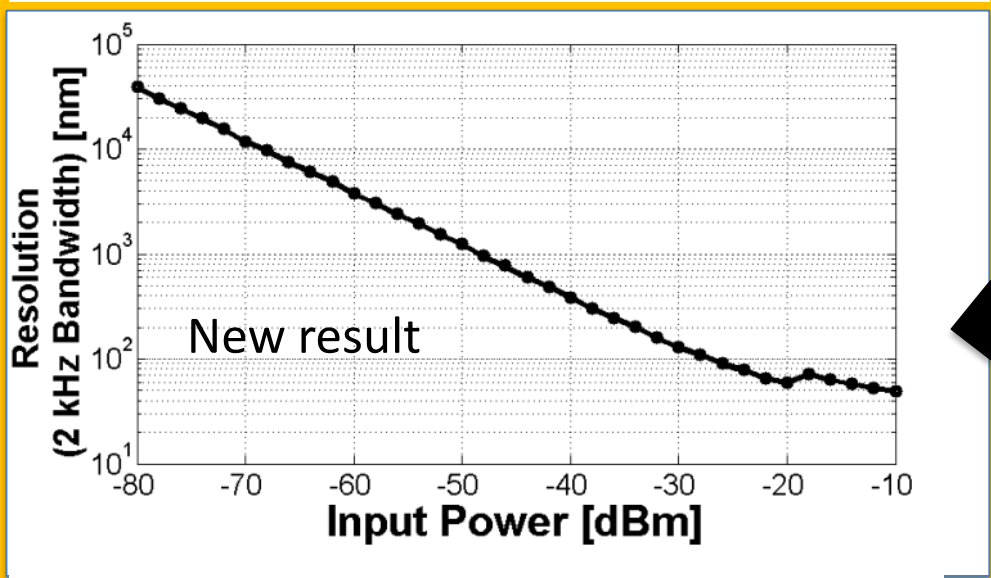
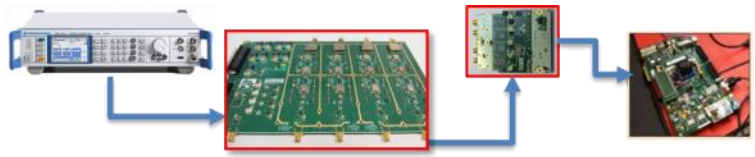
Performance Tests: Bench





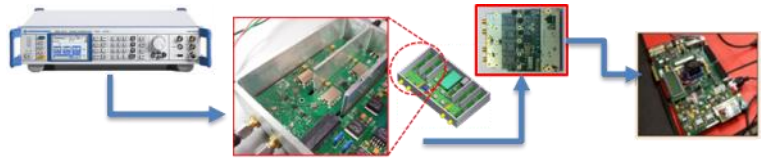
Test setup



RF generator > RFFE v1 > 130 MSP/s ADC > FPGA kit

Wrong FPGA calibration of delays between ADC clock and data paths caused the problem!

Test setup



RF generator > RFFE v2 > 130 MSP/s ADC > FPGA kit

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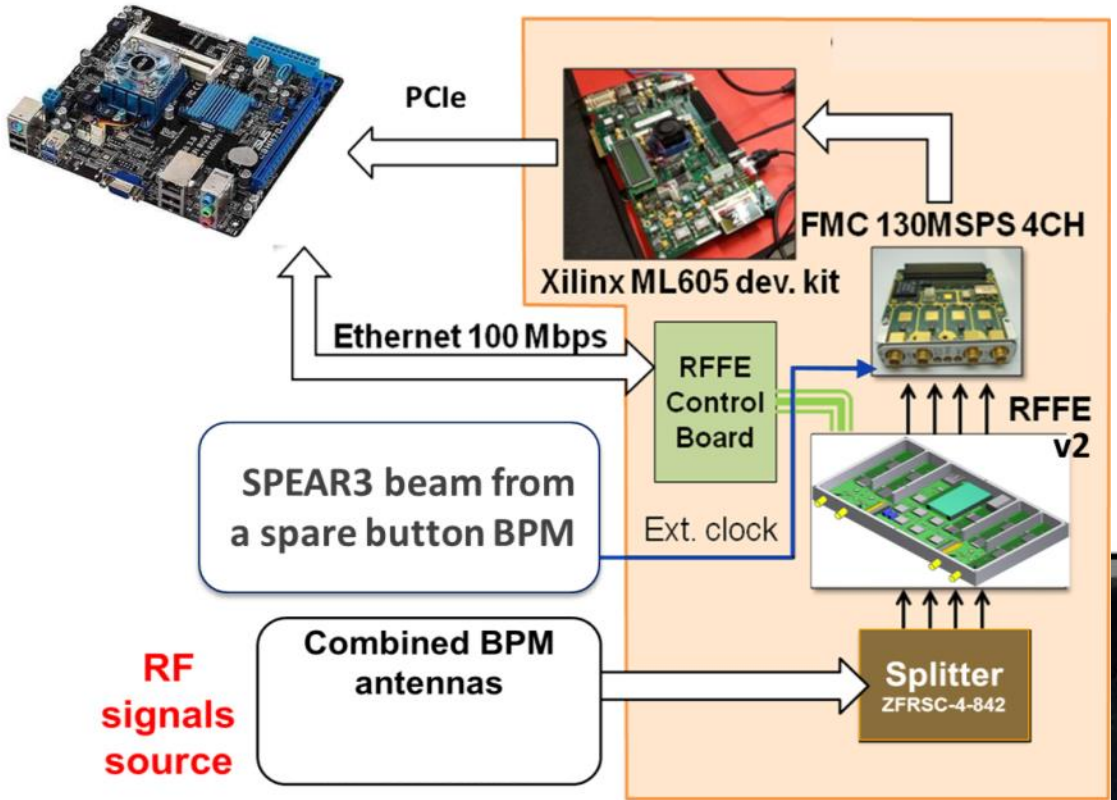
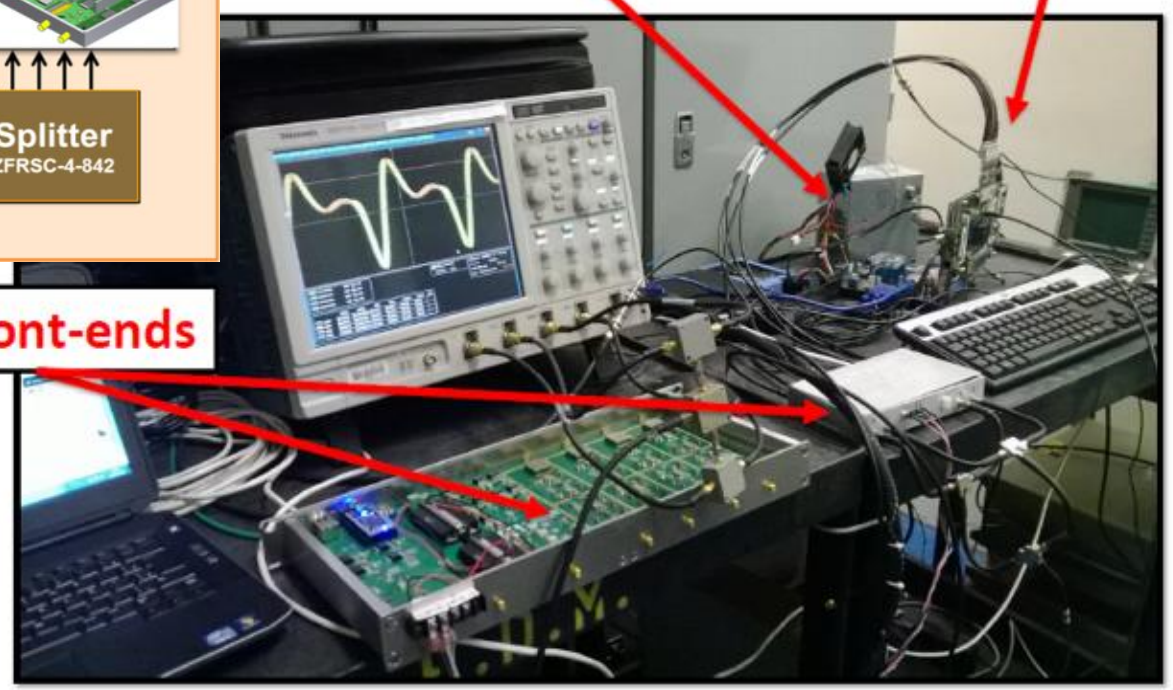
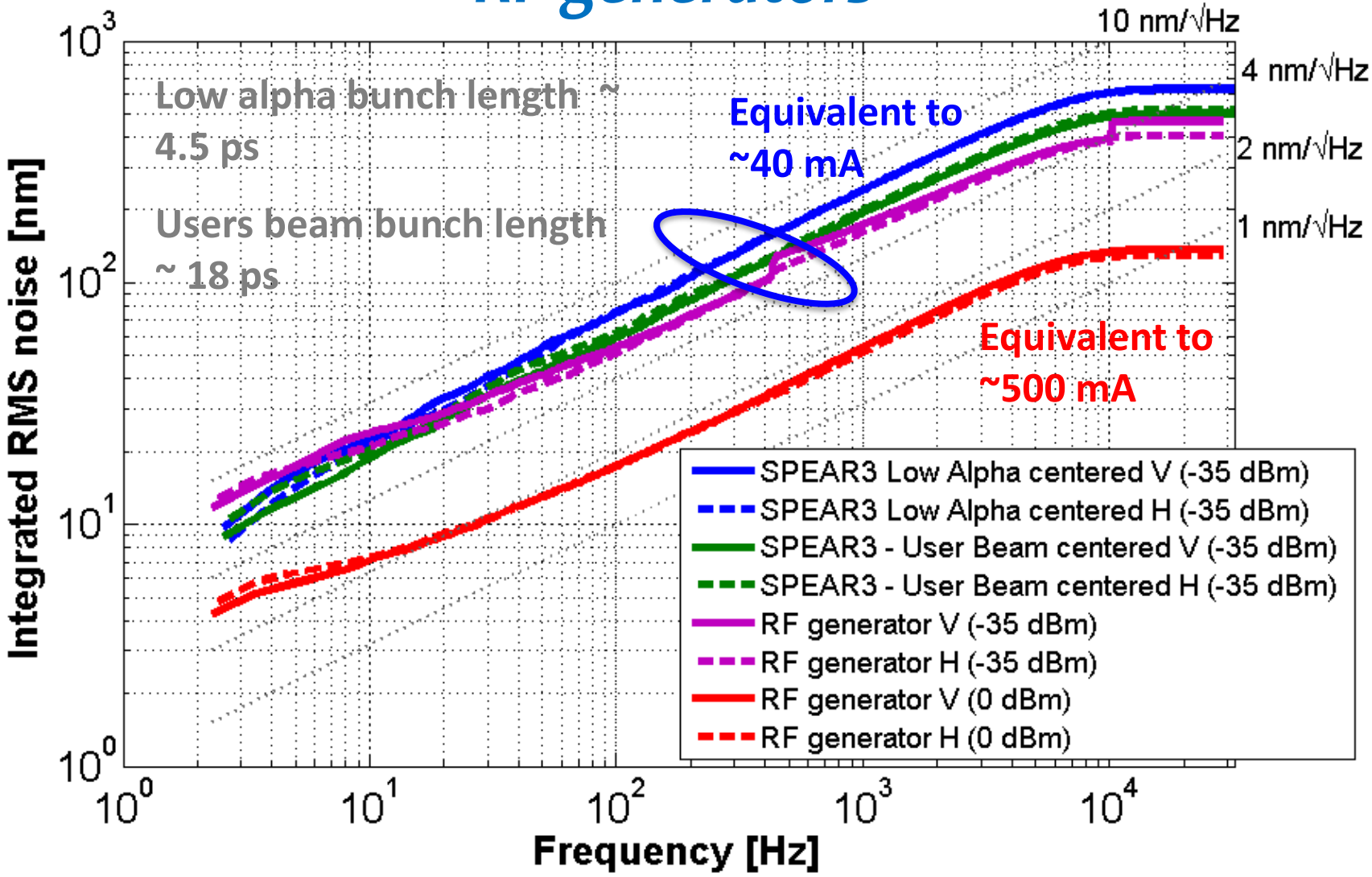




Testes performed at SPEAR3 (SLAC/SSRL)

Performance Tests: Beam

Comparing real beam, real beam @ low alpha mode and RF generators



Final Remarks

- Open Hardware repository: www.ohwr.org/projects
- Substantial integration work on the digital back-end will take place in 2015
- The performance of the Sirius BPM electronics “analog” hardware was improved
- Critical specifications are now met with exceeding performance
- BPM electronics design was performed in order to not limit the FOFB performance
- Efforts will be redirected to pre series production of RFFE and ADC boards in the 1st semester of 2015

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Thank you for your attention!

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