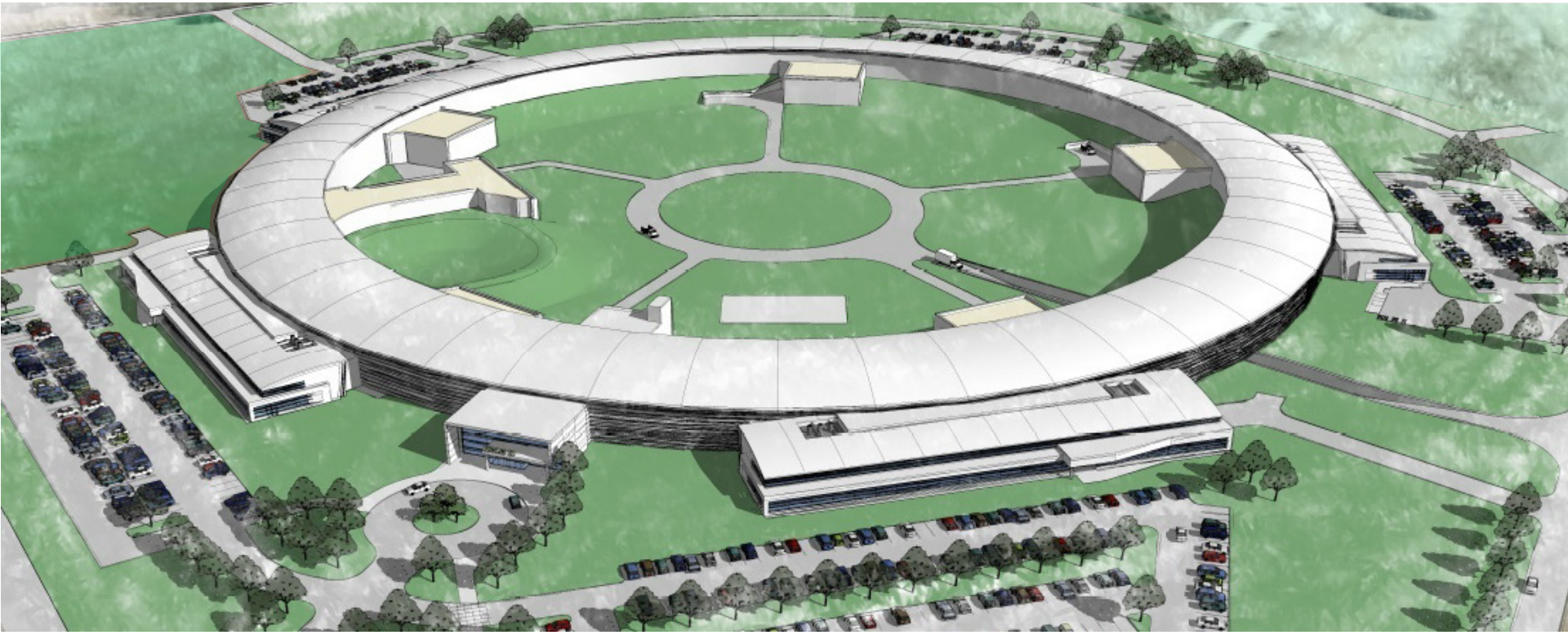
NSLS-II RF BPM Commissioning Update



Joseph Mead, on behalf of NSLS-II diagnostic group

International Beam Instrumentation Conference 2014
Monterey, California, USA, Sept. 14-18, 2014

Outline

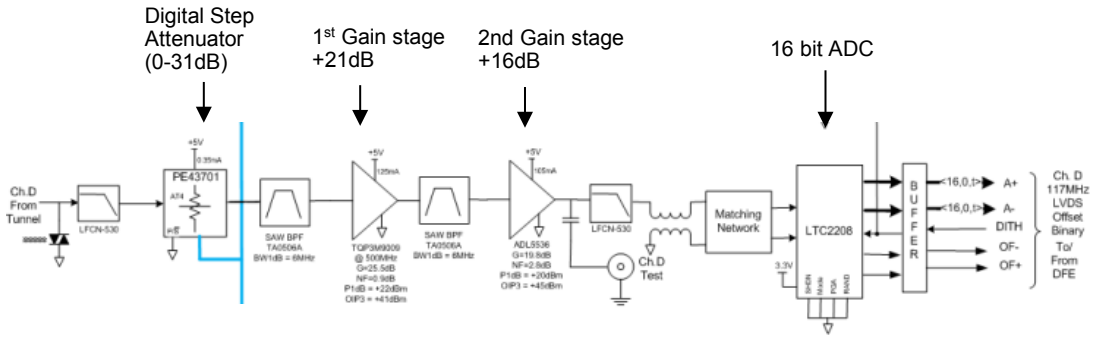
- Hardware
  - AFE – Analog Front End
  - DFE – Digital Front End
- Final Acceptance Testing
  - Pre-commissioning testing.
- Software: Control System Studio (CSS) Panels and Matlab Scripts
- Resolution Measurements with Beam
  - Storage Ring Commissioning ran from March 26 – May 12 and then again from Jun 30 – Jul 12. We had ½ shift for dedicated bpm measurements.

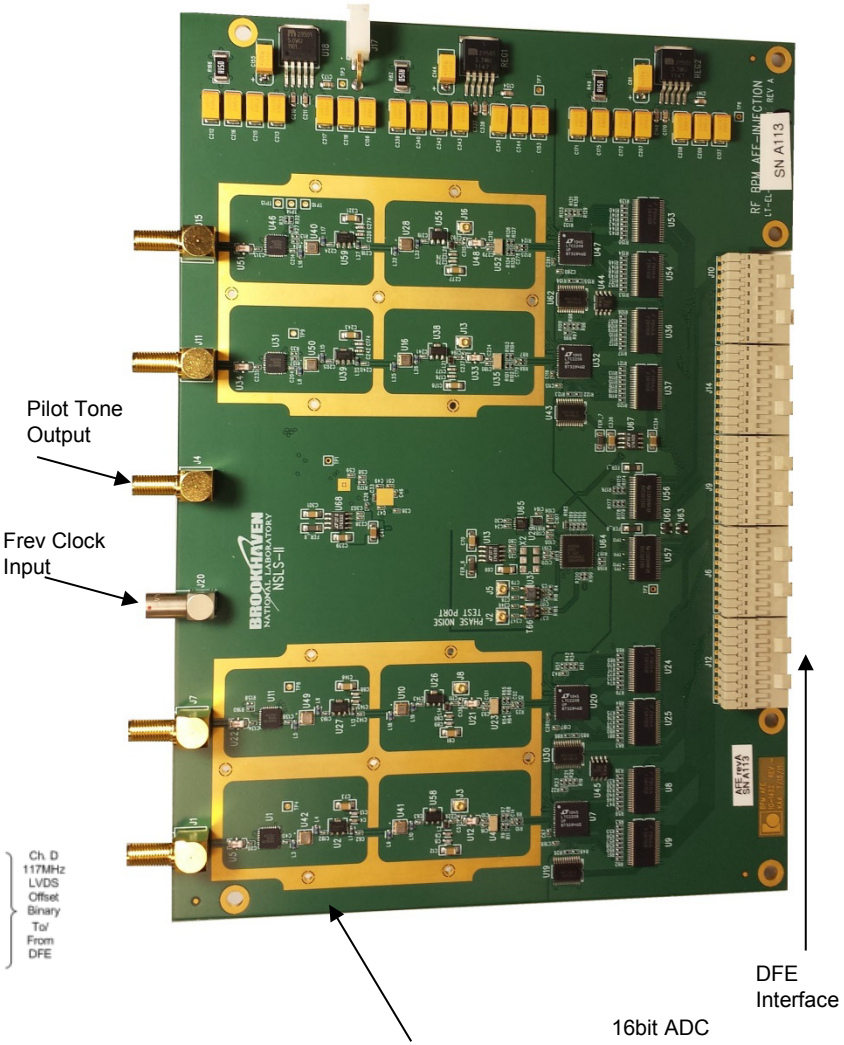
Analog Front End Board (AFE)

- Architecture is based on under-sampling the 500MHz impulse response of band-pass filter.
- Coherent signal processing – ADC clock is locked to Frev.
  - 310 ADC samples per turn
  - Signal Processing is “single-bin” DFT calculation at TbT rate to calculate magnitude of each channel.

- Performance Features
  - P1dB = +19dBm (at ADC Input)
  - IP3 = +43dBm (at ADC input)
  - NF = 5.3dB (dominated by LPF and SAW Filter)
  - Channel to Channel Isolation = 60dB

Single Channel Signal Chain

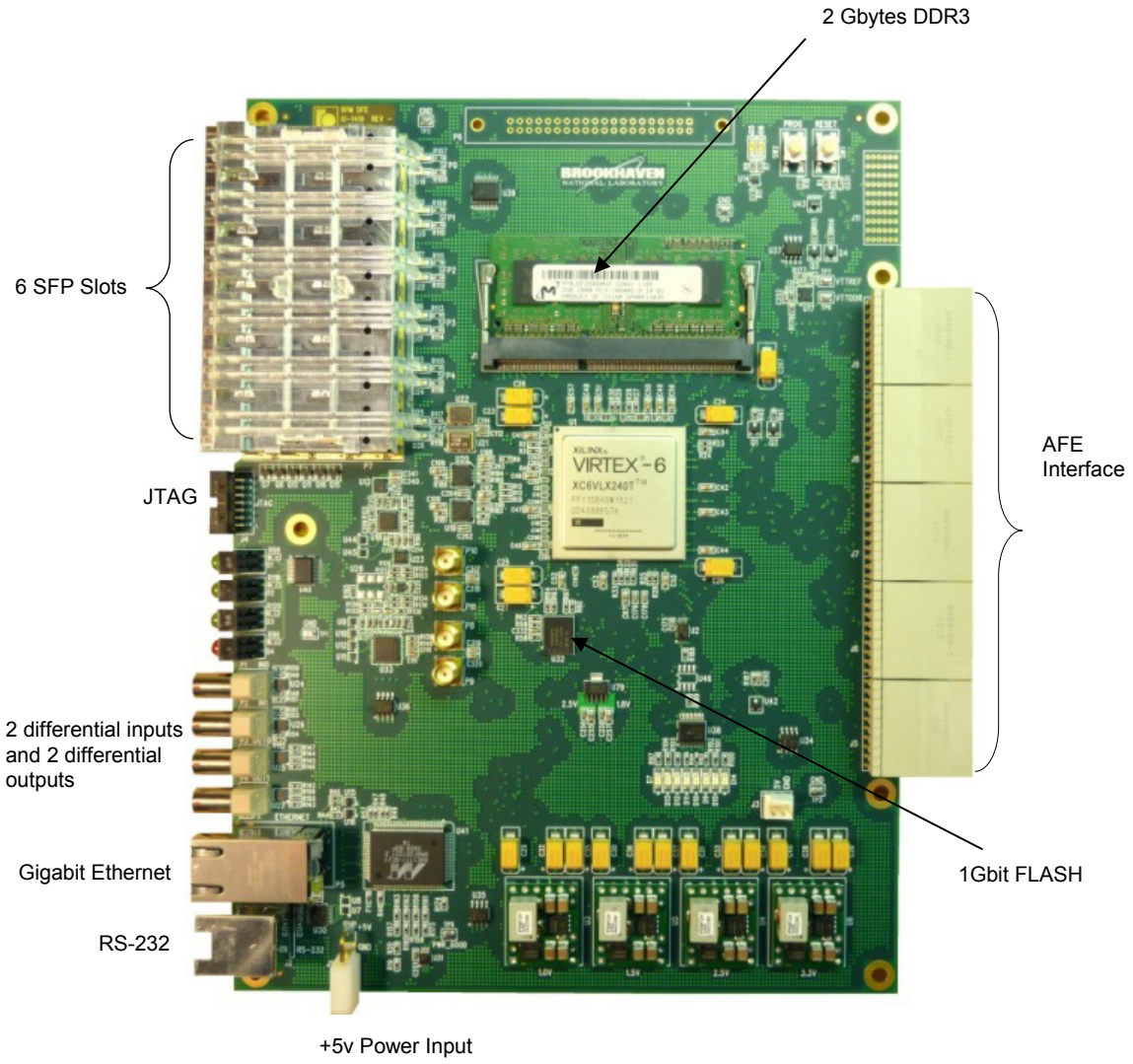




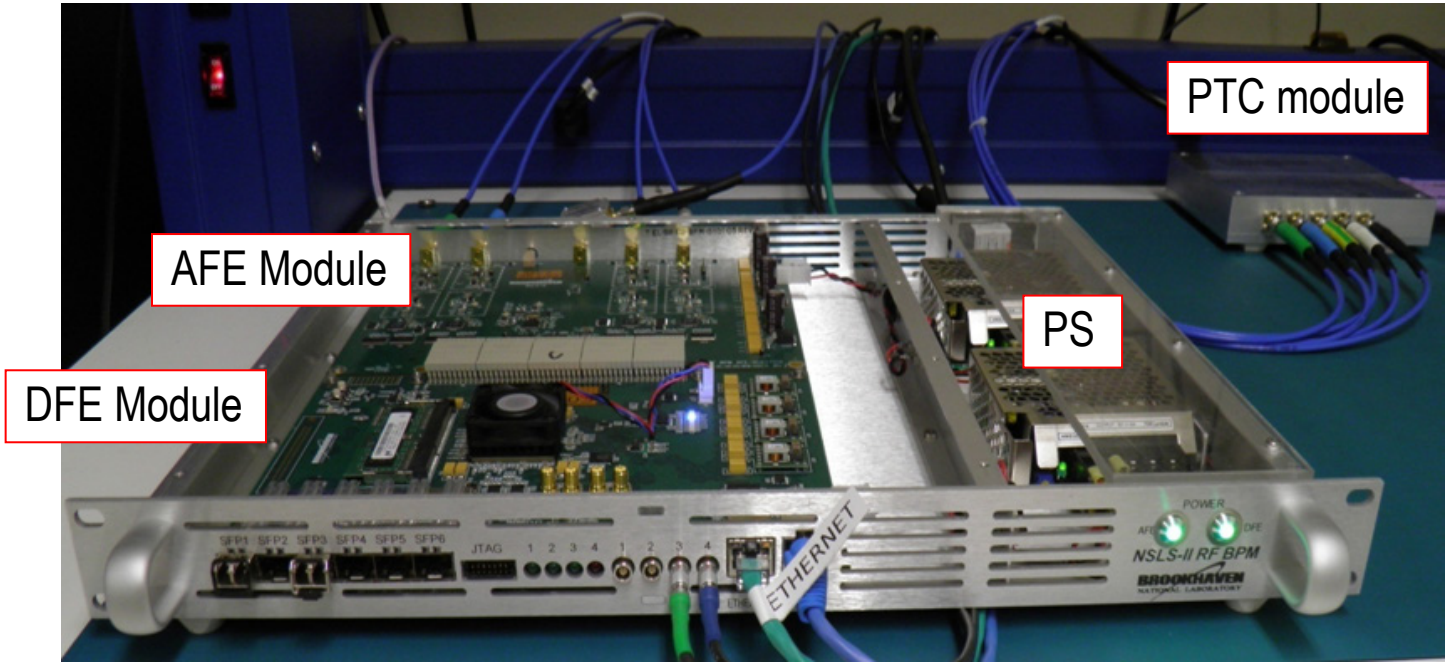
Digital Front End Board (DFE)

Features:

- Xilinx Virtex-6 FPGA (LX240T)
- Embedded MicroBlaze soft core µP
  - Xilkernel OS and lwIP TCP/IP stack
- Gigabit Ethernet
- 2Gbyte DDR3 Memory (SO-DIMM Module)
  - Local storage for ADC, TbT, FA waveforms.
  - Memory throughput = 6.4 GBytes/sec, which is fast enough to support streaming raw ADC data.
- Six 6.6Gbps SFP modules
  - Embedded Event Receiver
  - Fast Orbit Feedback
- 768 Hard Multipliers in FPGA fabric – Used for FIR filters, position calculations, etc.
- 1Gbit FLASH memory
- Also used as 'cell controller' processor for Fast Orbit Feedback
- Currently upgrading to 7-Series Zynq part for Photon BPM
  - Hard 1GHz Dual Core ARM Cortex A9 Processor

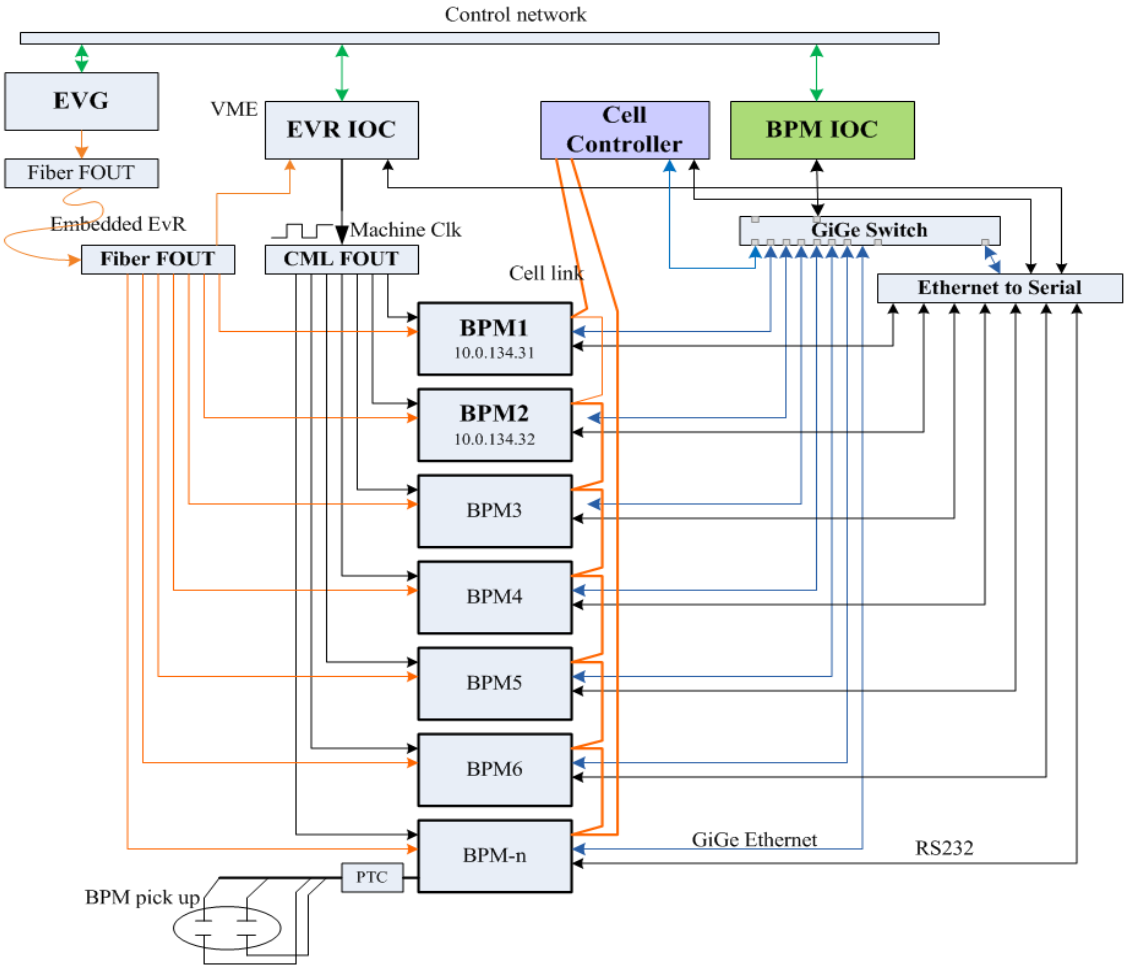


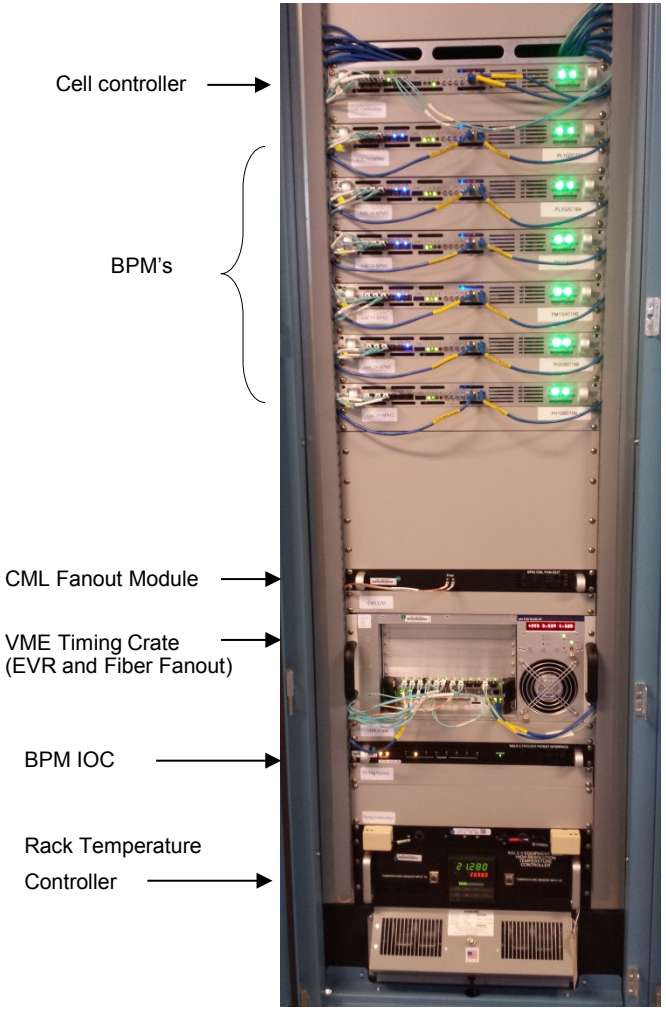
RF BPM Chassis



Data Type	Mode	Max Length
ADC Data	On-demand	256Mbytes or 32M samples per channel simultaneously
TBT	On-demand	256Mbytes or 5M samples Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
FOFB 10KHz	Streaming via SDI Link and On-demand	Streaming - X,Y,SUM ; For On-Demand: 256Mbytes or 5M samples Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
Slow Acquisition 10Hz	Streaming and On-demand	80hr circular buffer Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
System Health	On-demand	80hr circular buffer; AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status

Cell Level


Control network
EVG
VME
EVR IOC
Cell Controller
BPM IOC
Fiber FOUT
Embedded EvR
Machine Clk
GiGe Switch
Fiber FOUT
CML FOUT
Cell link
Ethernet to Serial
BPM1
10.0.134.31
BPM2
10.0.134.32
BPM3
BPM4
BPM5
BPM6
BPM-n
GiGe Ethernet
RS232
PTC
BPM pick up


Cell controller
BPM's
CML Fanout Module
VME Timing Crate
(EVR and Fiber Fanout)
BPM IOC
Rack Temperature
Controller

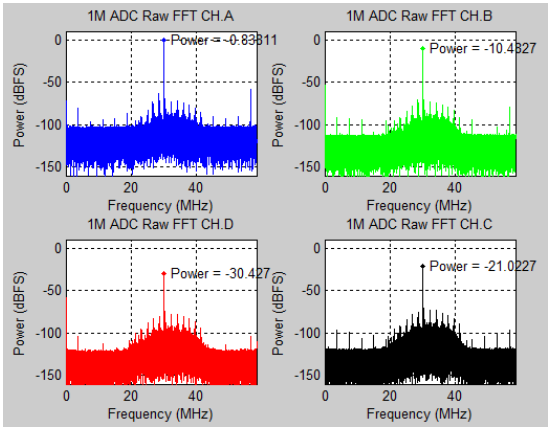
Final Acceptance Testing

- Developed a suite of tests prior to commissioning to fully test all functionality.
- Using command line python scripts
  - Verify all networking and serial port connections are working
  - Verify latest firmware software versions are installed.
  - Verify all flash settings are correct (network, kx, Ky, gains, timing, etc)
  - Update Firmware remotely
- Using Matlab scripts and pilot tone generator on BPM
  - Cable Orientation tests : Installed different attenuators on each of the 4 inputs to the PTCM and read out ADC results.
  - Static Gain Calibration : Calibrated out gain variations of the 4 RF channels for 20 different attenuator settings. Results are stored on each BPM in FLASH
  - Intensity Dependence scan : Vary intensity of pilot tone signal check for resulting position offsets.
- For more information, please see poster TUPF01 for more details

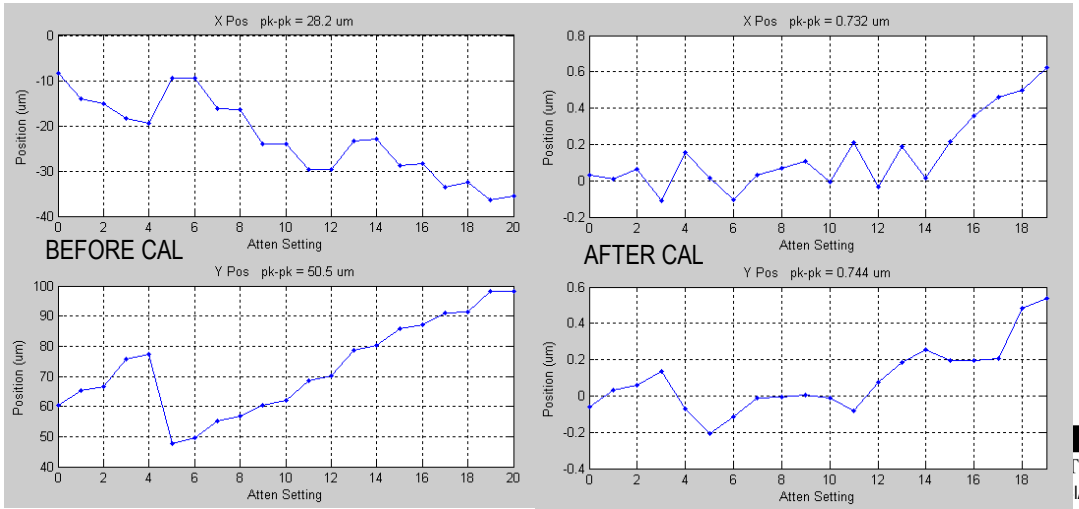
```
mead@box32:/home/cdanneil/python$ ./bpm_status.py booster
Area = booster

bpm     ip              moxa              mode     fgga_ver  ublz_ver PLL Lock
-------------------------------------------------------------------------------
 1   ip=10.0.142.12   moxa=10.0.133.250:4001   app      490071113       4990    T
 2   ip=10.0.142.13   moxa=10.0.133.250:4002   app      490071113       4990    T
 3   ip=10.0.142.14   moxa=10.0.133.250:4003   app      490071113       4990    T
 4   ip=10.0.142.15   moxa=10.0.133.250:4004   app      490071113       4990    T
 5   ip=10.0.142.16   moxa=10.0.133.250:4005   app      490071113       4990    T
 6   ip=10.0.142.17   moxa=10.0.133.250:4006   app      490071113       4990    T
 7   ip=10.0.142.18   moxa=10.0.133.250:4007   app      490071113       4990    T
 8   ip=10.0.142.19   moxa=10.0.133.250:4008   app      490071113       4990    T
 9   ip=10.0.142.20   moxa=10.0.133.250:4009   app      490071113       4990    T
10   ip=10.0.142.21   moxa=10.0.133.227:4010   app      490071113       4990    T
11   ip=10.0.142.22   moxa=10.0.133.227:4011   app      490071113       4990    T
12   ip=10.0.142.23   moxa=10.0.133.227:4012   app      490071113       4990    T
13   ip=10.0.142.24   moxa=10.0.133.227:4013   app      490071113       4990    T
14   ip=10.0.142.25   moxa=10.0.133.227:4014   app      490071113       4990    T
15   ip=10.0.142.26   moxa=10.0.133.227:4015   app      490071113       4990    T
16   ip=10.0.142.27   moxa=10.0.133.227:4016   app      490071113       4990    T
17   ip=10.0.142.28   moxa=10.0.133.227:4017   app      490071113       4990    T
18   ip=10.0.142.29   moxa=10.0.133.227:4018   app      490071113       4990    T
19   ip=10.0.142.30   moxa=10.0.133.227:4001   app      490071113       4990    T
20   ip=10.0.142.31   moxa=10.0.133.227:4002   ???      -1      -1      F
21   ip=10.0.142.32   moxa=10.0.133.227:4003   app      49071013        4990    T
22   ip=10.0.142.33   moxa=10.0.133.227:4004   app      49071013        4990    T
23   ip=10.0.142.34   moxa=10.0.133.227:4005   app      490071113       4990    T
24   ip=10.0.142.35   moxa=10.0.133.227:4006   app      49071013        4990    T
25   ip=10.0.142.36   moxa=10.0.133.227:4007   app      490071113       4990    T
26   ip=10.0.142.37   moxa=10.0.133.227:4008   ???      -1      -1      F
27   ip=10.0.142.38   moxa=10.0.133.227:4009   app      490071113       4990    T
28   ip=10.0.142.39   moxa=10.0.133.250:4010   app      490071113       4990    T
29   ip=10.0.142.40   moxa=10.0.133.250:4011   app      490071113       4990    T
```

Python script to check BPM connectivity and firmware versions

Cable Orientation test results



Static Gain Calibration results

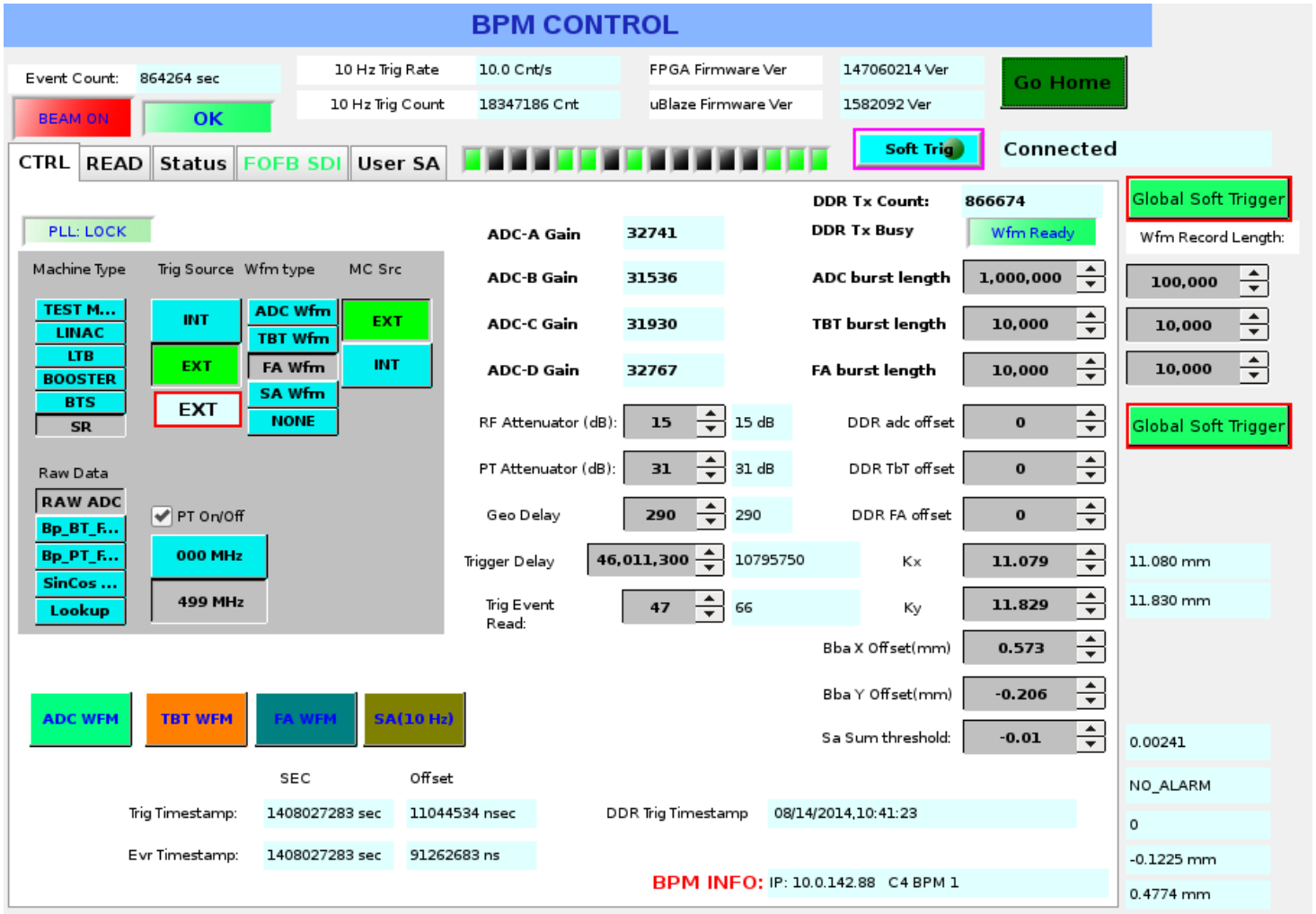


BPM SR Main CSS OPI screen

- The Main BPM CSS Summary page provides a quick overview of the system's health. Different colors indicate different fault conditions and help identify if problems are at the individual bpm level, cell level, or global level.
- Each cell has 6 arc BPM's and up to 3 ID BPM's. (Injection straight BPM's are located in Cell 30)
- Green = OK
- Blue = ADC Saturated
- Orange = Pilot Tone On
- Pink = IOC disconnected
- Red = BPM communication problem

- 5 different Alarm Conditions
  - 1. PLL Not locked – BPM ADC clock is not locked to the RF
  - 2. BPM Communication Failure - IOC and BPM have stopped communicating (10 Hz heartbeat)
  - 3. Pilot Tone On
  - 4. FPGA Over Temperature
  - 5. Frev Heartbeat Fail – Frev clock is not present

BPM Top Level Engineering Panel



Other diagnostic Matlab Scripts

- Matlab scripts have been developed for system experts to help quickly determine system health at a global level.
- For example, the application shown here was very useful during early commissioning, shows pertinent information for all SR BPM's on a single screen, which updates at 1Hz.

WCM, ICT, FCT information from linac and booster

Current Fill Pattern, from fill pattern monitor

X,Y position information

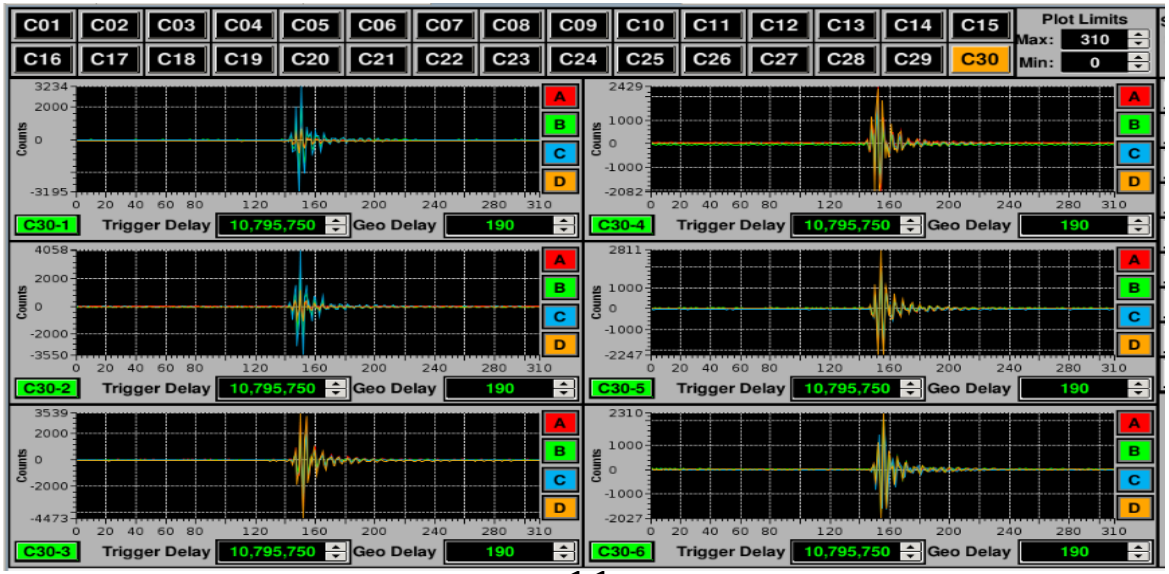
TbT Sum signal : especially useful during commissioning 1st turn to see where beam loss was occuring

Max ADC value : helps determine if gain settings are optimal or if ADC's are saturating

ADC Timing : displays location in the turn where the maximum ADC value occurred, helps determine if BPM is timed in correctly

BPM Timing

- The Beam Position Monitor Electronics calculates a single horizontal and vertical position for every revolution. To function correctly the electronics needs to have its timing signals properly adjusted. This involves the adjustment of two different delay values, one being a fine adjustment and one a coarse adjustment.
  - Trigger Delay is the course adjustment. It has the resolution of a turn and tells the system when to start storing data to DDR memory.
  - Geo Delay is the fine delay adjustment. It provides a delay of the machine clock (Frev) signal which is received from the timing system. The delay resolution is approximately 8.5ns, which is the ADC sampling clock period, and the range of the delay is a single revolution, which is 2.6us. This delay permits compensation for various cabling delays and beam transit delays between BPM's, thus allowing all BPM's in the ring to perform their position calculation on the same bunches
- As of now, the “timing in” of the BPM’s is a manual process, but with the help of the CSS panel shown below, 2 people were able to time in all BPM’s in under 2 hours.



NSLS-II BPM Performance Requirements

Injection System

- Frev = 1.89MHz
- Bunch Spacing = 2ns
- Rep Rate = 1Hz

Parameters/ Subsystems	Conditions	Vertical	Horizontal
Injector single bunch single shot	0.05 nC charge	300 μm rms	300 μm rms
	0.50 nC charge	30 μm rms	30 μm rms
Injector multi bunch single shot (80-150 bunches;)	15 nC charge	10 μm rms	10 μm rms

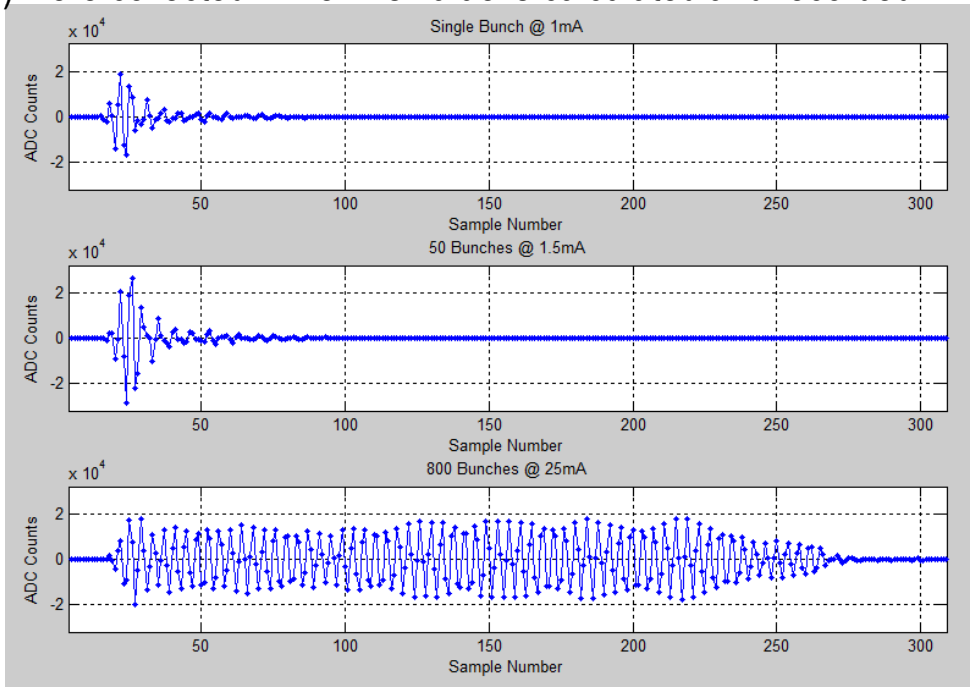
Parameters/ Subsystems			Conditions	*Multipole chamber RF BPM Resolution Requirement	
				Vertical	Horizontal
50 mA to 500 mA Stored beam resolution – 20% to 100 % duty cycle	BPM Receiver Electronics	Turn by Turn (80% fill)	Data rate = 378 kHz	3 μm rms	5 μm rms
		Assuming no contribution from bunch/ fill pattern effects	0.017 Hz to 200 Hz	0.2 μm rms	0.3 μm rms
			200 Hz to 2000 Hz	0.4 μm rms	0.6 μm rms
			1 min to 8 hr drift	0.2 μm rms	0.5 μm rms
		Bunch charge/ fill pattern effects only	DC to 2000 Hz	0.2 μm rms	0.3 μm rms
	Mechanical motion limit at Pick-up electrodes assembly (ground & support combined)	Vibrations	50 Hz to 2000 Hz	10 nm rms	10 nm rms
			4 Hz to 50 Hz	25 nm rms	25 nm rms
			0.5 Hz to 4 Hz	200 nm rms	200 nm rms
		Thermal	1 min to 8 hr	200 nm peak	500 nm peak

Storage Ring

- Frev = 378KHz
- Frf = 499.68MHz

Initial BPM TbT and FA Resolution Tests

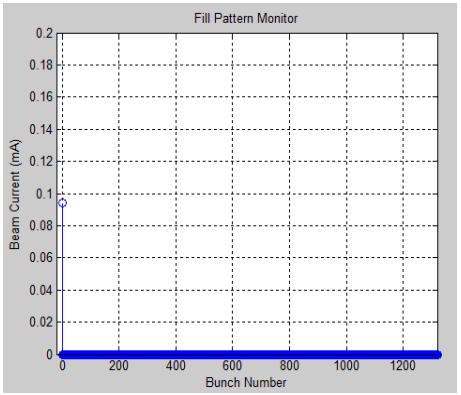
- A single BPM electronics module located in Cell 28 was connected via a combiner/splitter to measure electronics performance independent of beam motion. Buttons are in Cell 28 immediately before first bending magnet
- Storage Ring was filled with a particular fill pattern.. TbT data and FA data records were collected as the beam decayed to measure noise performance as a function of beam current. Scrapers were inserted to speed up of the decay of the beam
- Approximately every 5 seconds, BPM is triggered and raw ADC waveform (2,000pts), TbT waveform (100,000pts) and FA waveform (9000 pts) were collected. The rms value is calculated and recorded.
- Three different fill patterns were used
  - Single Bunch
  - 50 bunches
  - ~60% fill

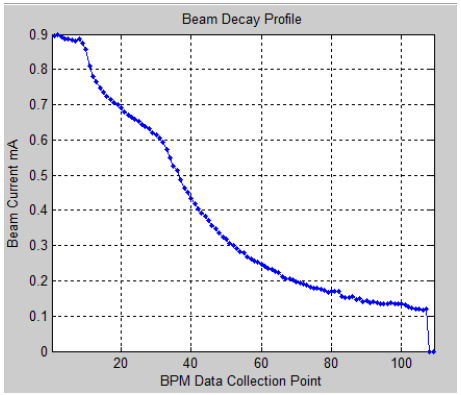


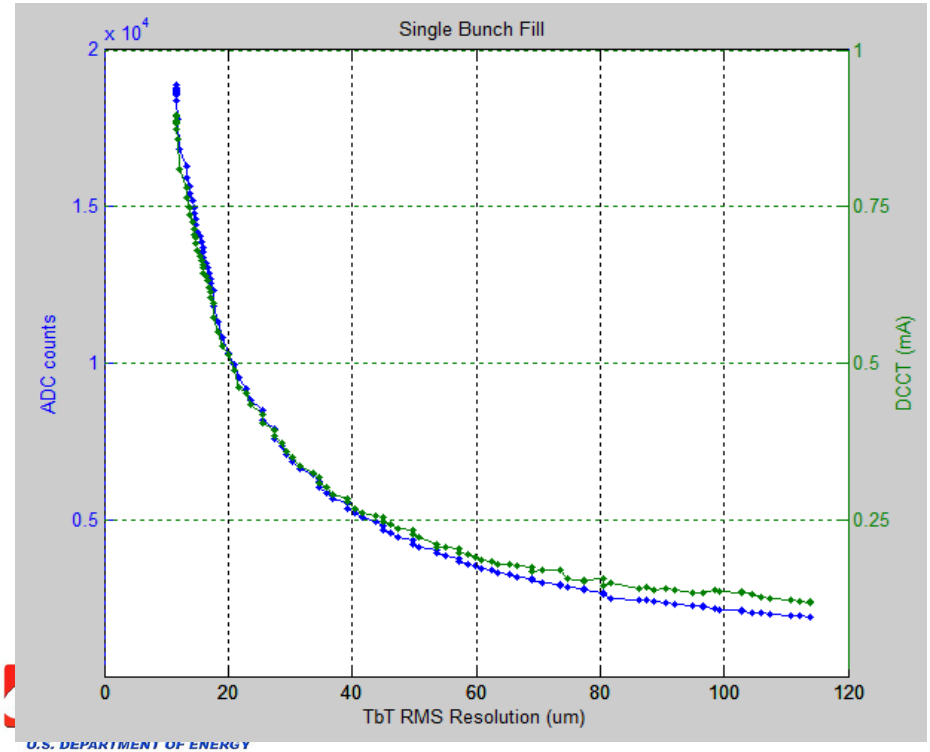
ADC data for different fill patterns.

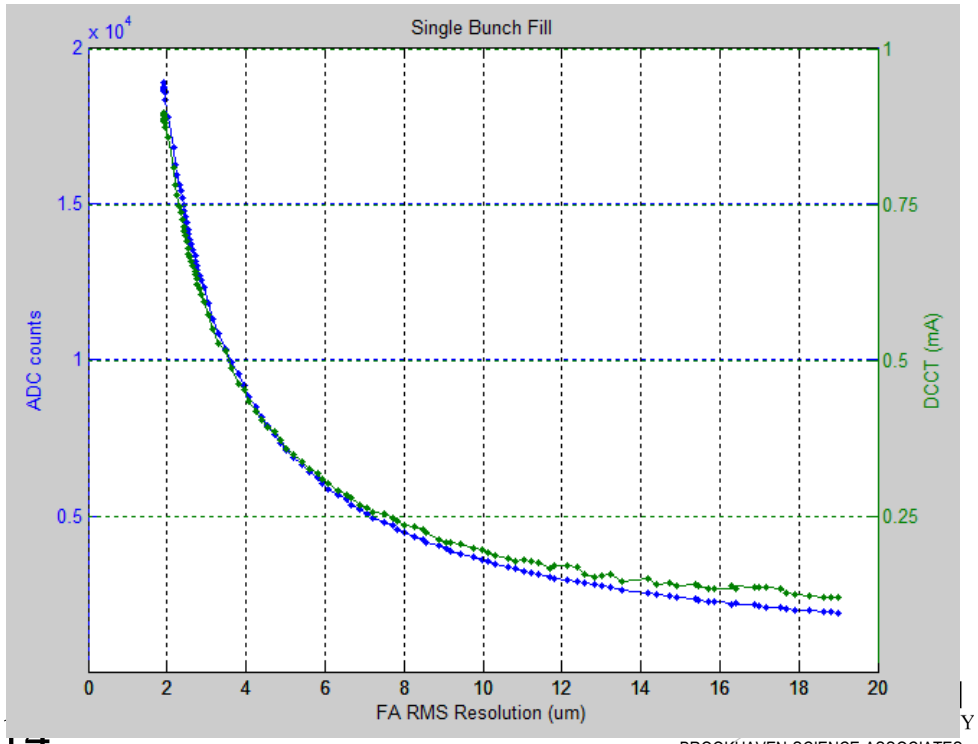
Single Bunch : TbT and FA Performance

- Single Bunch beam current was limited to 1 mA, which corresponds to about ½ full ADC scale.
  - TBT Resolution at 1mA ~ 12um
  - FA Resolution at 1mA ~ 2um
  - Expect a factor of 6 improvement between TbT and FA resolution because bandwidth is reduced by a factor of 38.



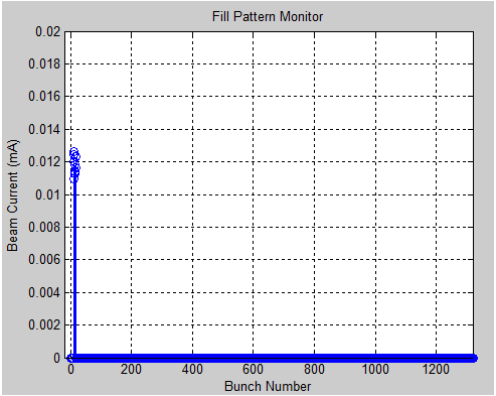


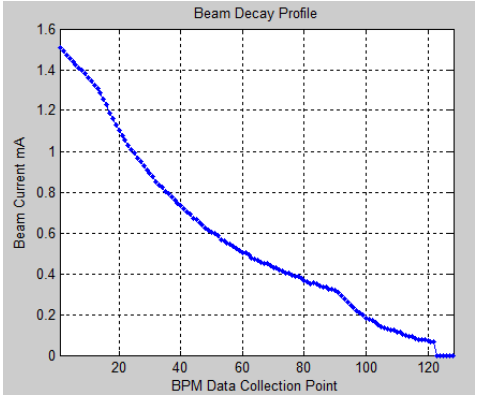


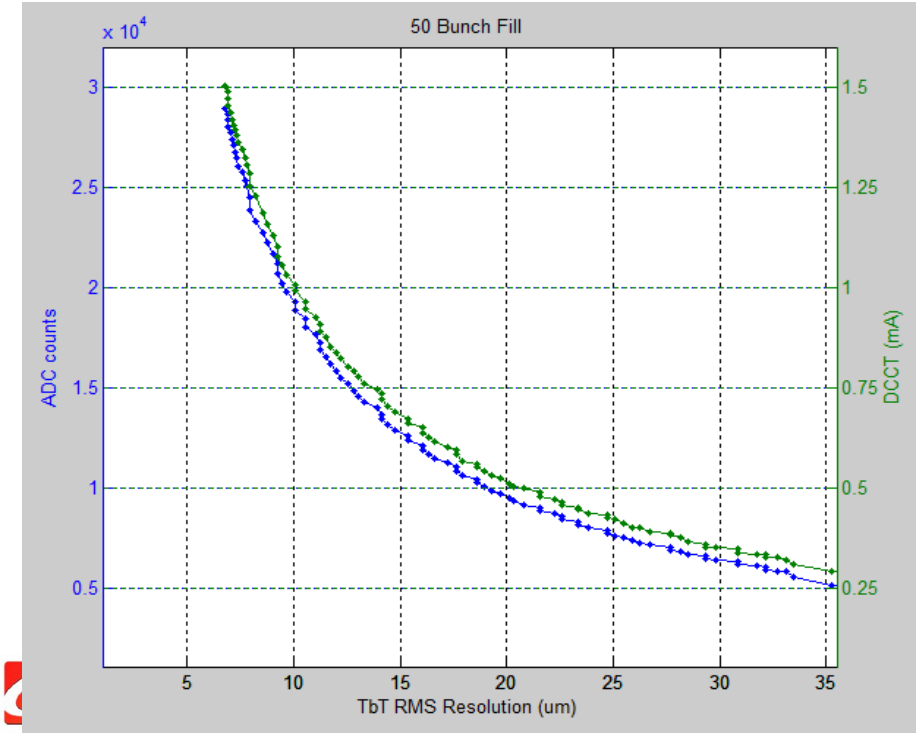


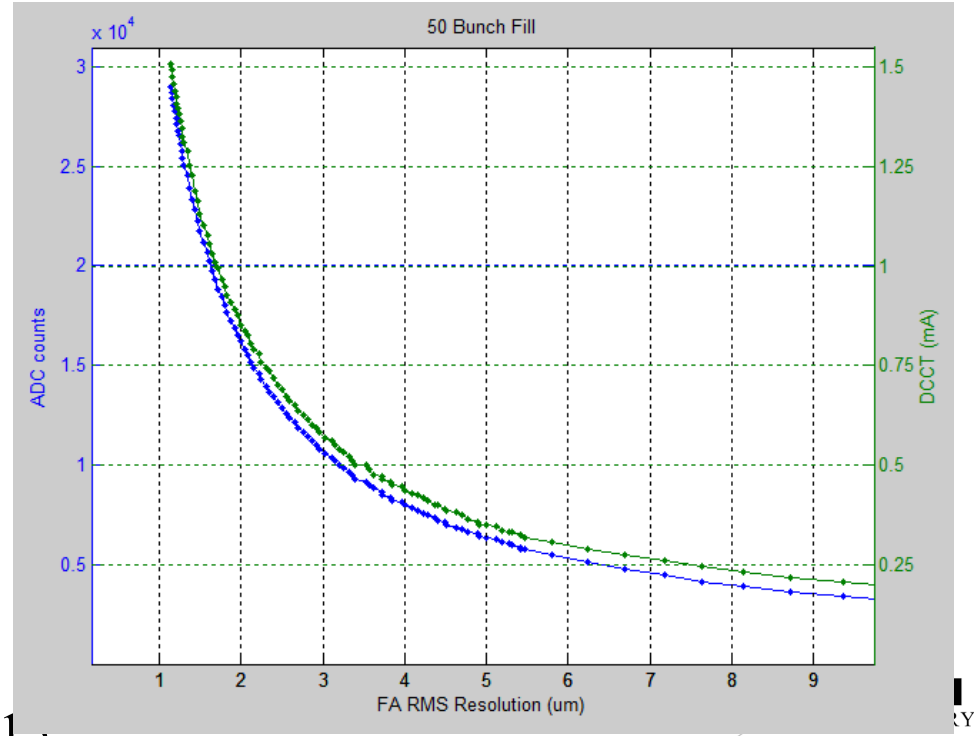
50 Bunch : TbT and FA Performance

- 50 bunches, beam current was limited to 1.5 mA, which corresponds to almost full ADC scale.
  - TBT Resolution at 1.5mA ~ 7um
  - FA Resolution at 1.5mA ~ 1.2um



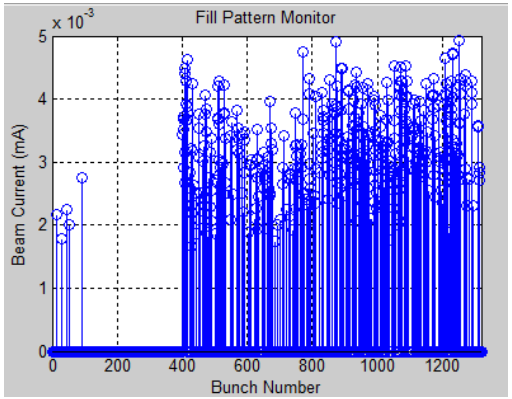


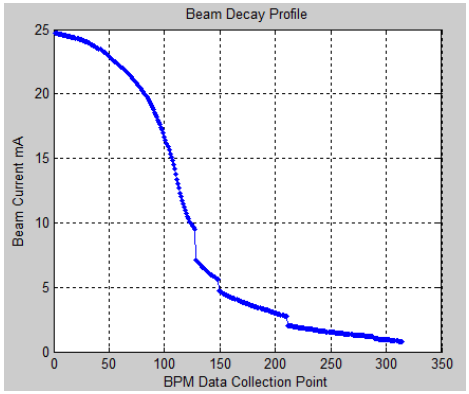


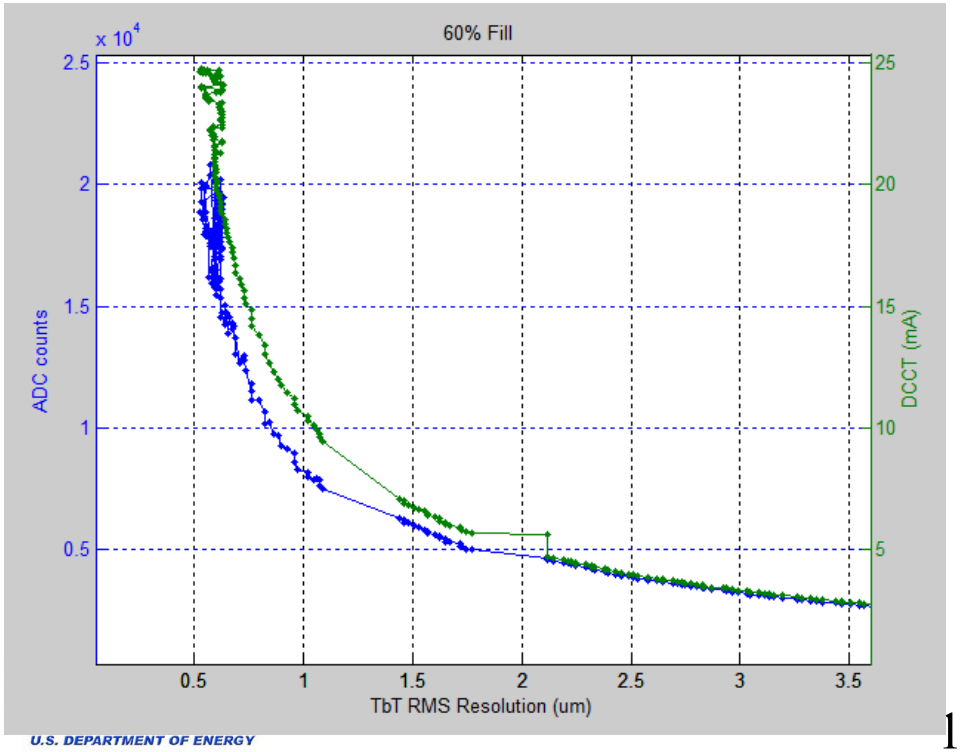


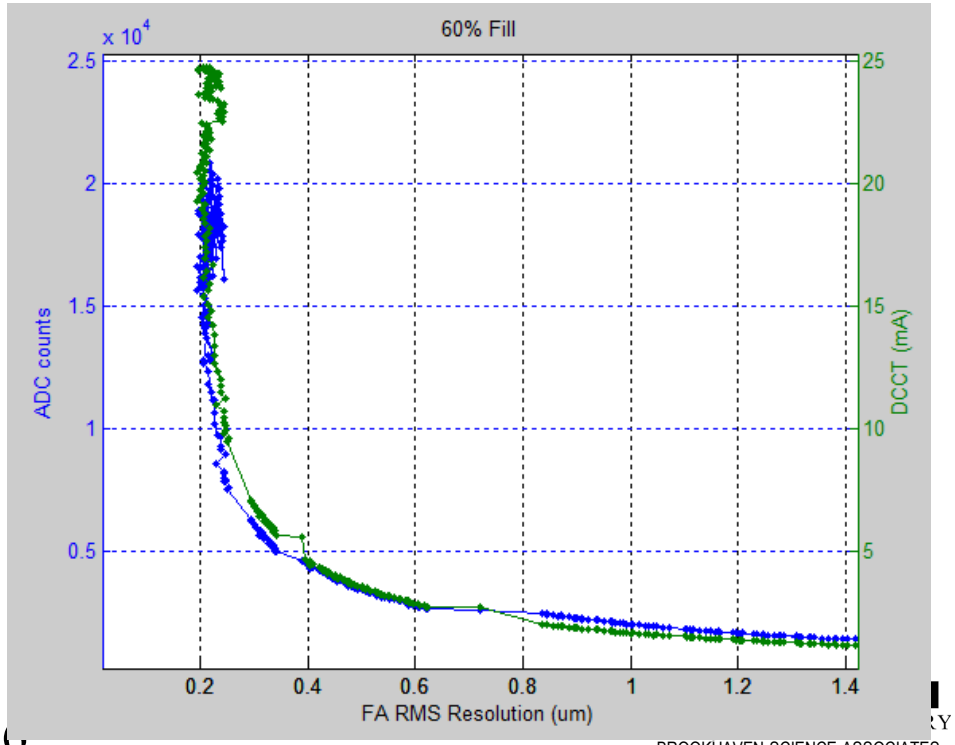
60% Fill : TbT and FA Performance

- 60% fill pattern, beam current was limited to an administrative limit of 25 mA, which corresponds to almost full ADC scale.
  - TBT Resolution at 15mA ~ 700nm
  - FA Resolution at 15mA ~ 200 nm
- Above 15mA, BPM peak ADC signals becomes blurred, most likely do to longitudinal instabilities.



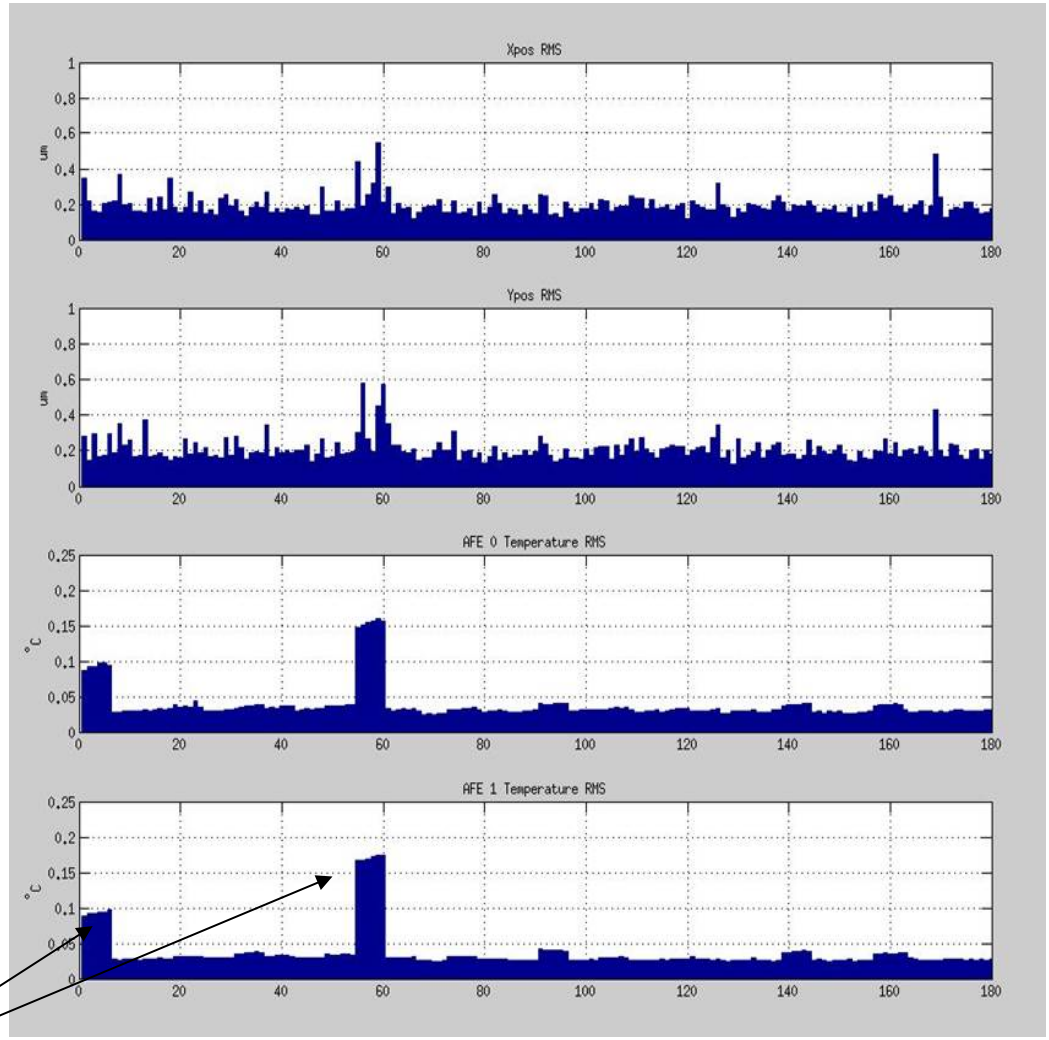






Long Term Drift BPM Data (using Pilot Tone)

- Due to a lack of time, no long term drift studies have been performed with beam yet.
- Tests were performed using integrated Pilot Tone Synthesizer.
  - 10Hz BPM Data was collected from all 180 Storage Ring BPM's for 8 hours along with corresponding temperature sensors on AFE board.
  - RMS value of the 8 hours of data is computed and plotted for X,Y, and 2 temperature sensors on the AFE.
  - Pilot Tone Synthesizer was used to generate CW signal, ADC scale was near ½ full scale
- Data was collected during a major shutdown, so optimal conditions may not have been in place (i.e. tunnel temperature stability)
- For most BPM's the 8 hour drift specification of 0.2um RMS vertical and 0.5um RMS horizontal are met.

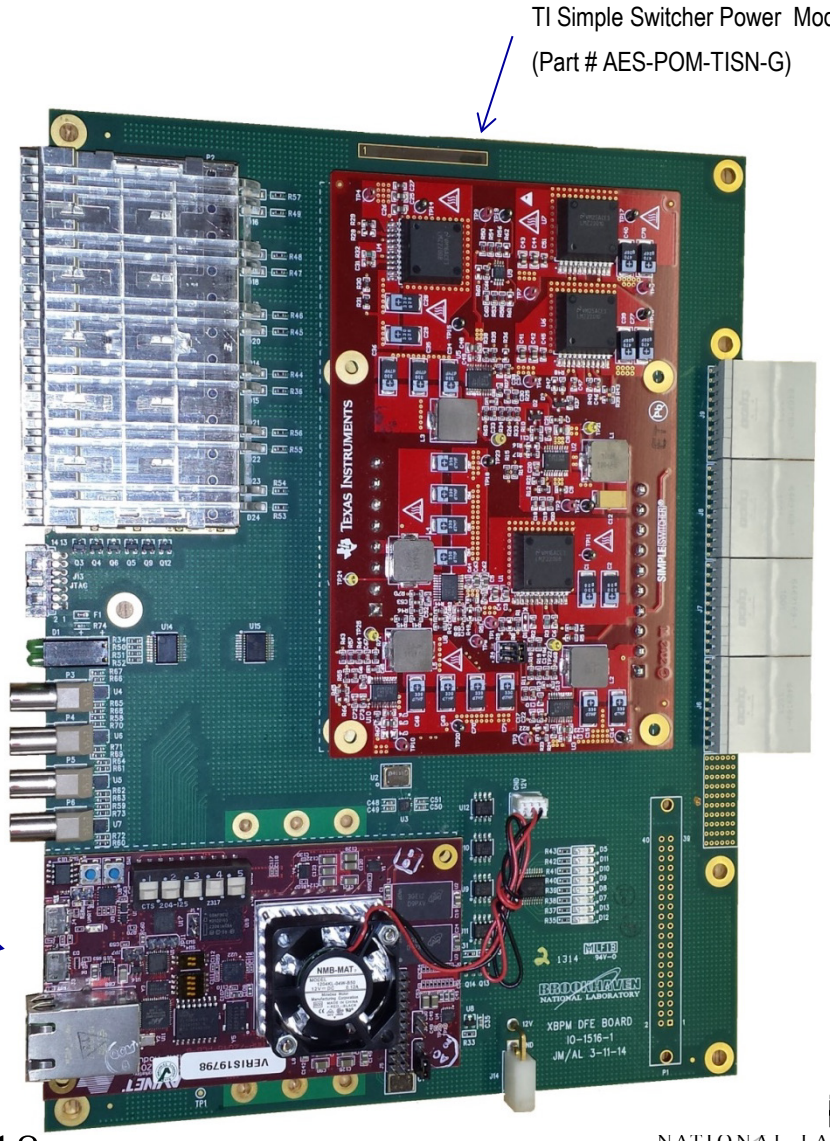


Issue with cell 9 and cell 30 temperature controllers

Next Generation Zynq DFE

Features:

- Xilinx Zynq 7045 FPGA (LX240T)
  - Uses Avnet Zynq Mini Module
- Hard Dual-Core ARM Cortex A9 processor
  - Linux OS
- Gigabit Ethernet
- 2Gbyte DDR3 SO-DIMM
  - Memory throughput = 6.4 GBytes/sec
- Six 6.6Gbps SFP modules
  - Embedded Event Receiver
  - Fast Orbit Feedback
- Fixed Point DSP Engine
- 1Gbit FLASH memory
- Also used as 'cell controller' processor for Fast Orbit Feedback
- Currently using this DFE for Photon BPM's and cell controller upgrade.



Conclusions and Future Plans

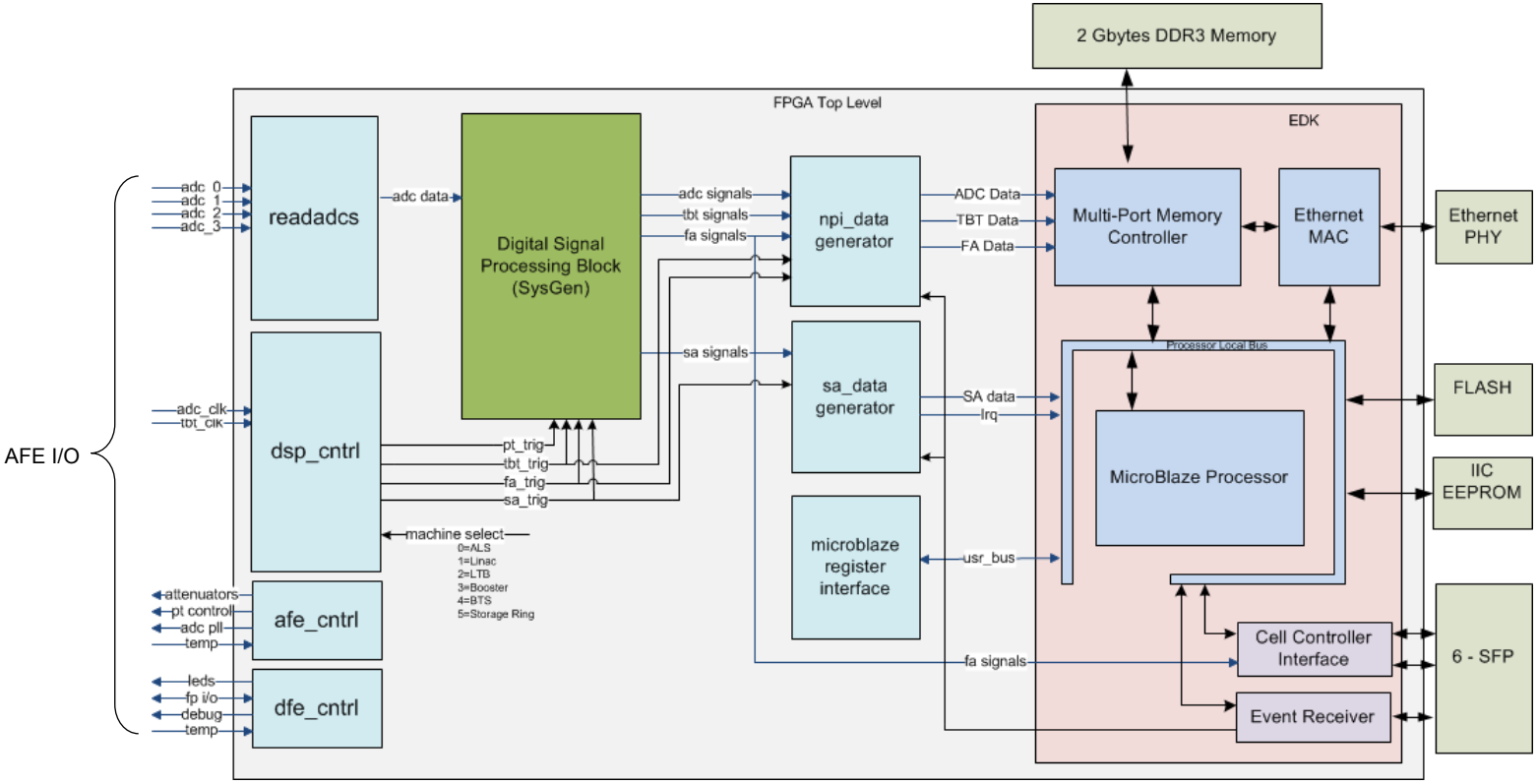
- Performance Testing
  - Even though the initial BPM resolution measurement results are very encouraging, to fully verify the compliance with the specs, similar measurements should be repeated at higher currents, as well as with long bunch trains (when stable).
  - When larger amounts of dedicated beam time are provided, long term drift studies should also be performed.
  - Also, plans to study to characterize orbit sensitivity to the fill pattern changes and as well as to the changes of BPM attenuation should be performed.

- Future Hardware/Software Plans
  - As time permits, plan to look more closely at using pilot tone signal to help with long term drift. Other plan is to further investigate thermo-electric cooling to even better control ADC temperature stability.
  - Upgraded DFE module to provide more computational power / better networking performance. Also can move to a more standard operating system such as Linux. Currently using for photon BPM electronics.

- Backup

Architecture : DFE FPGA

- FPGA Implemented using a combination of VHDL, Verilog, System Generator (for DSP block) and EDK for Microblaze processor.
  - Digital Signal Processing implementation using Matlab-Simulink Model Based design flow.
- External DDR3 Memory permits long simultaneous storage of different data streams
  - 32 Msamples Raw ADC, 5Msamples TbT data, 5Msamples FA data, 80 Hrs of 10Hz data

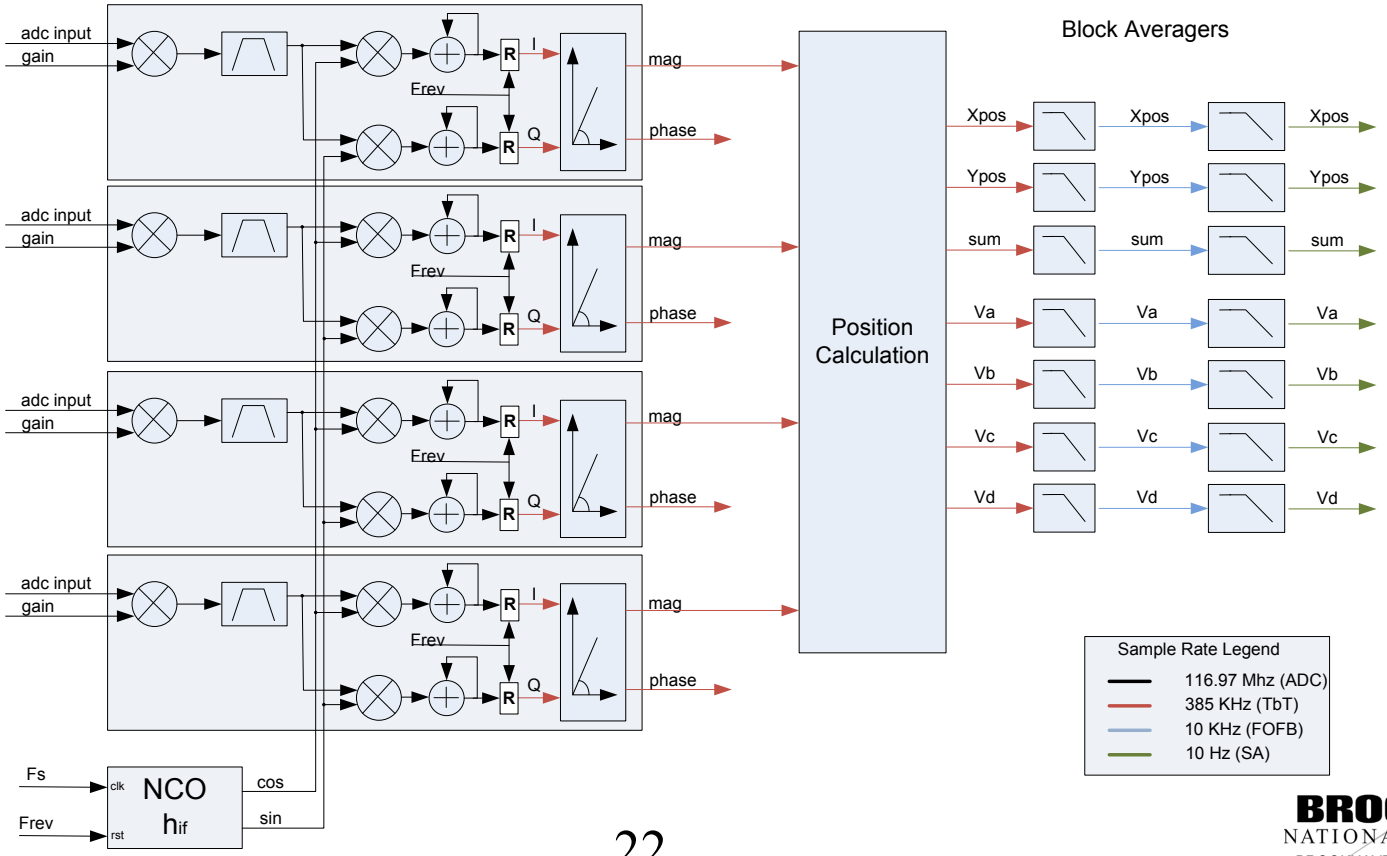


Architecture : Signal Processing

- Coherent Signal Processing – phase locked to Frev
- “Single bin” DFT position processing at TbT rate

$$X[h_{IF}] = \sum_{n=0}^{hSample-1} x[n] \cdot e^{\frac{-i \cdot 2\pi \cdot h_{IF} \cdot n}{h_{Sample}}} \qquad , n = 0..h_{Sample} - 1$$

Parameter	NSLS-II Storage Ring	NSLS–II Booster	ALS Storage Ring
F_{rf}	499.68 MHz	499.68 MHz	499.6398 MHz
h	1320	264	328
h_{sample}	310	62	77
h_{IF}	80	16	20



Architecture : Control System

- One soft IOC for each cell of BPM's
- 3 different TCP/IP sockets between BPM and IOC
  - 10Hz position and status update
  - Control (Set parameters, etc)
  - Waveform records (ADC, TbT, FA)
- Microblaze application uses XilKernel OS and LWIP TCP/IP stack
  - Very limited TCP/IP performance ~2MBytes/sec throughput