Upgrade Development Progress For The CERN SPS High Bandwidth Transverse Feedback Demonstration Processor

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Abstract

A high bandwidth feedback demonstrator system has been developed for proof of concept transverse intra-bunch closed loop feedback control studies at the CERN SPS. This system contains a beam pickup, analog front end receiver, signal processor, back end driver, power amplifiers and kicker structure. The main signal processing functions are performed digitally, using very fast (4GSa/s) data converters to bring the system signals into and out of the digital domain. The digital signal processing function is flexibly implemented in an FPGA allowing for maximum speed and reconfigurability for testing different control algorithms. The signal processor is a modular design consisting of commercial and custom components. This approach allowed for a rapidly-developed prototype to be delivered in a short time with limited resources. Initial beam studies at the SPS using the system prior to the CERN long shutdown one (LS1) have been very encouraging. We are planning several key upgrades to the system, including the signal processor.

Introduction and Background

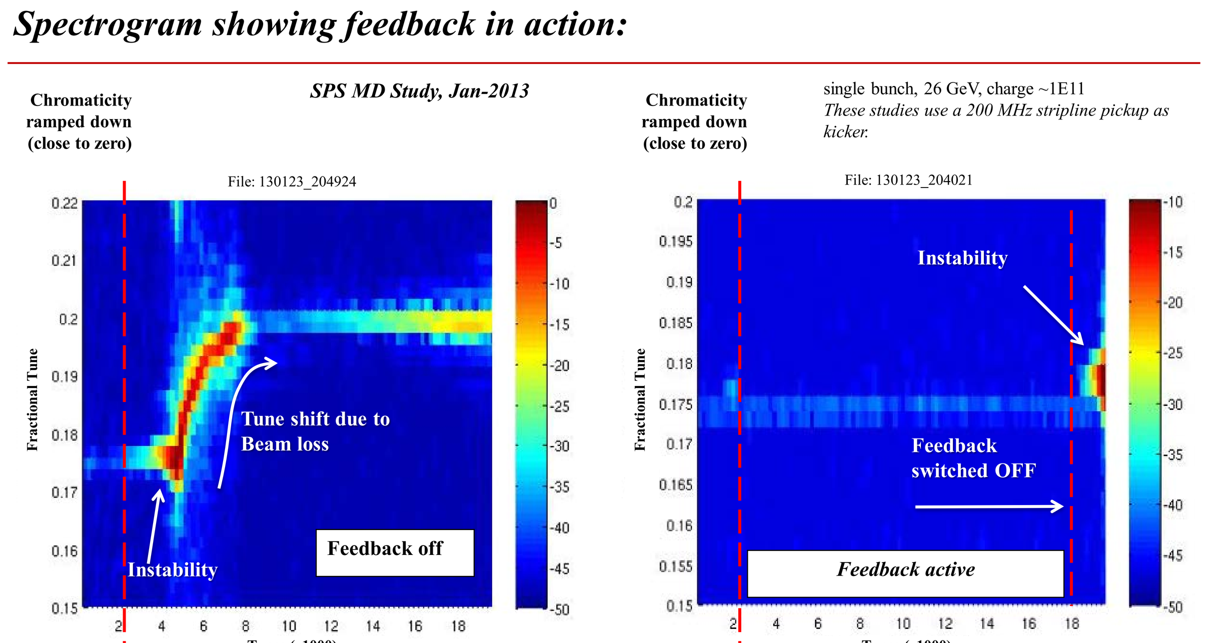
Introduction and Motivation:

- High Intensity LHC beam is known to cause transverse instabilities driven by the electron cloud effect and Transverse Mode Coupled Instabilities (TMCI) in the SPS. This adversely affects operation of the SPS, especially for the planned high-luminosity upgrade where beam intensities increase.
- A research and development effort has been undertaken between CERN and SLAC under the auspices of the US LHC Accelerator Research Program (LARP) to develop techniques for mitigating the instabilities using a wide-bandwidth transverse closed-loop feedback system. Goal: Achieve feedback control of intra-bunch instabilities
- This work involves simulation and modeling of the beam and bunch dynamics along with the controller, research and development of high sampling rate digital signal processing electronics (along with low-noise analog front and back ends) and feedback control techniques and development of a wide bandwidth kicker structure (to apply correction fields to the beam).

Work to Date:

- A rapidly developed single-bunch demonstrator system was conceived and developed in 2012. This system was used in Machine Development (MD) studies at the SPS prior to Long Shutdown 1 (LS1).
- The simulation and modelling effort is progressing with work towards developing more detailed models including non-linear effects and system identification formalisms and optimal controller topologies.
- The pre-LS1 MD measurements were performed using the existing low bandwidth kicker (200MHz), allowing control of only lower-order modes (0, 1).
- The system results demonstrated control of mode 0 instabilities for a single bunch:

Spectrogram showing feedback in action:



- **Feedback stabilizes the bunch** !
- clearly working for dipole mode
- confirms high sensitivity of receiver circuit
- confirms feedback possible with the very small kick strength of ~1 kV [transverse]

W. Hofle, CERN

Upgrades:

With this initial success, we are planning to upgrade the system with additional functions and for higher performance. For the immediate future, we are focusing on four areas:

1) Feedback Demo Processor Upgrades

2) RF Power Amplifier Upgrades

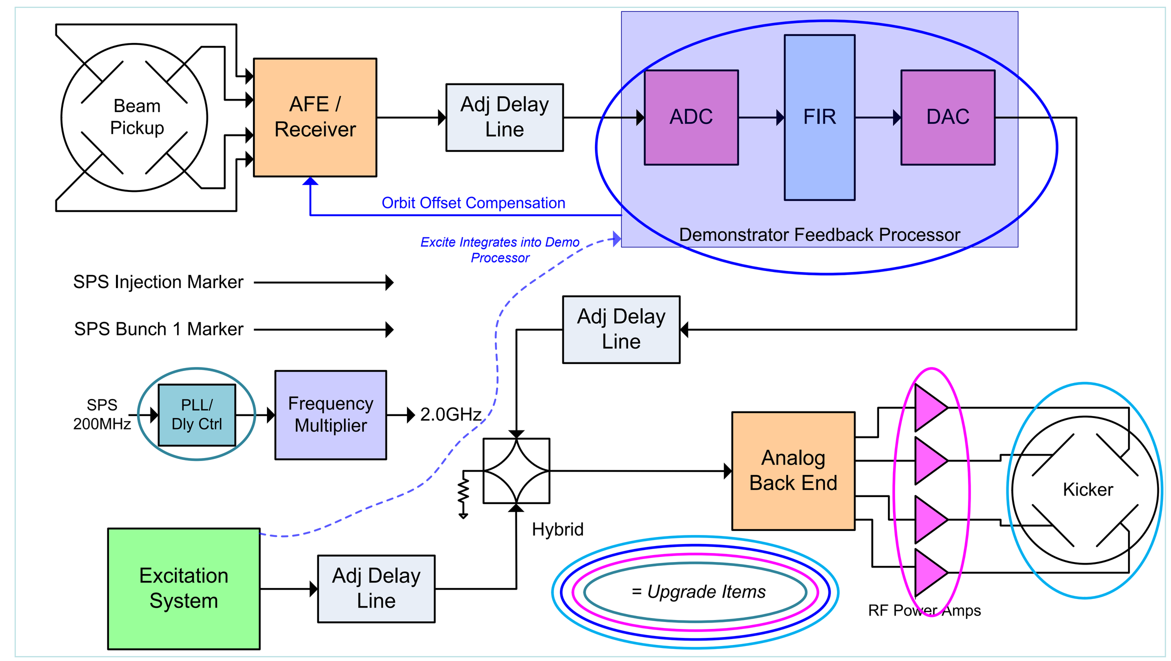
3) Beam Kicker Structure Upgrades

4) Demo Processor Support Hardware Upgrades

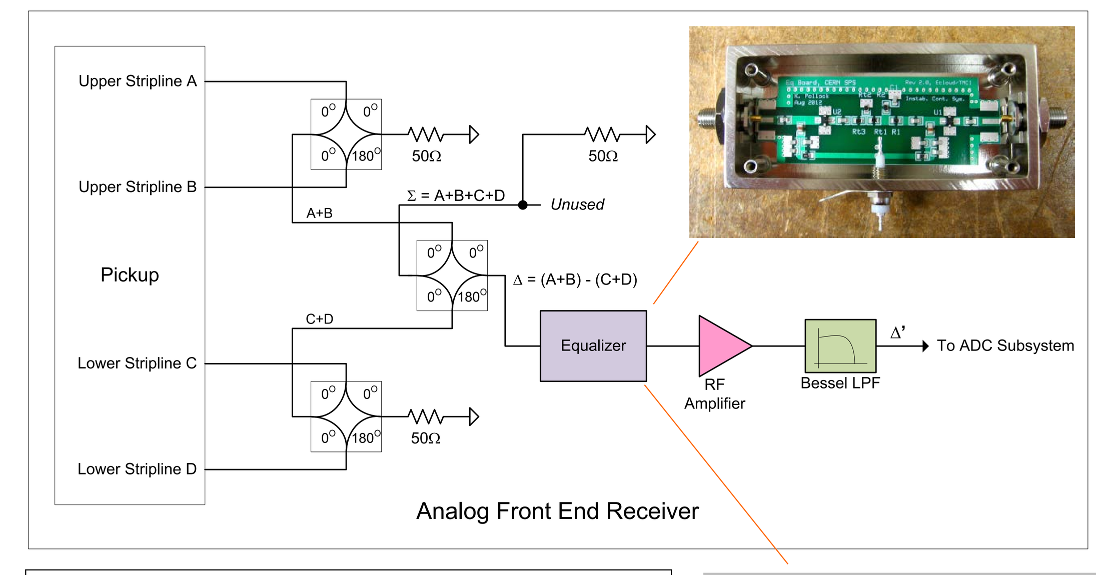
Longer-Term/Ongoing Work:

► Higher sampling rate processing (8GSa/s)
► MISO Control Techniques (use of multiple beam pickups)
► Multiple Bunch Processing
► Different Digital Filter Structures (IIR, FIR)

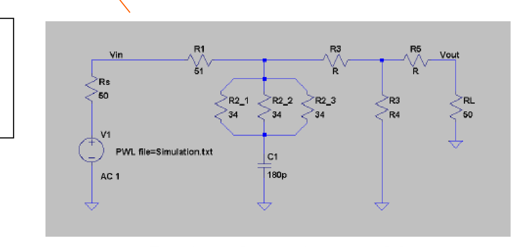
System Overview



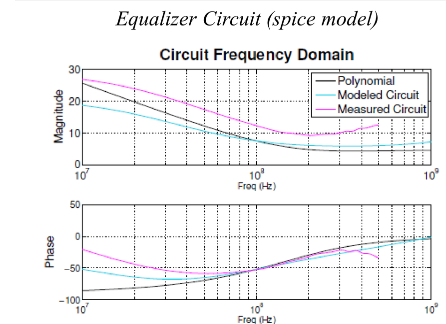
Overall System Block Diagram: Feedback and Excitation Systems



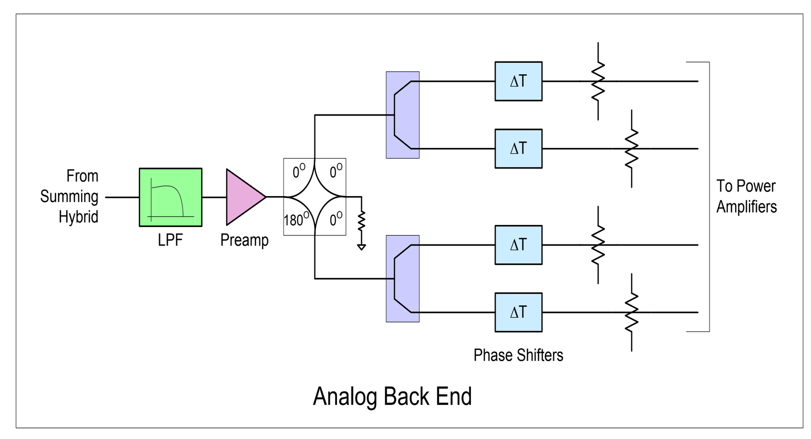
The Equalizer:
An analog equalizer was developed to compensate for amplitude and phase distortions introduced by the pickup and cabling. This compensation is necessary to allow us to properly apply a time-domain correction signal to the bunch. This work was done by K. Pollock, SLAC.



Equalizer Circuit (spice model)



Equalizer Frequency Response

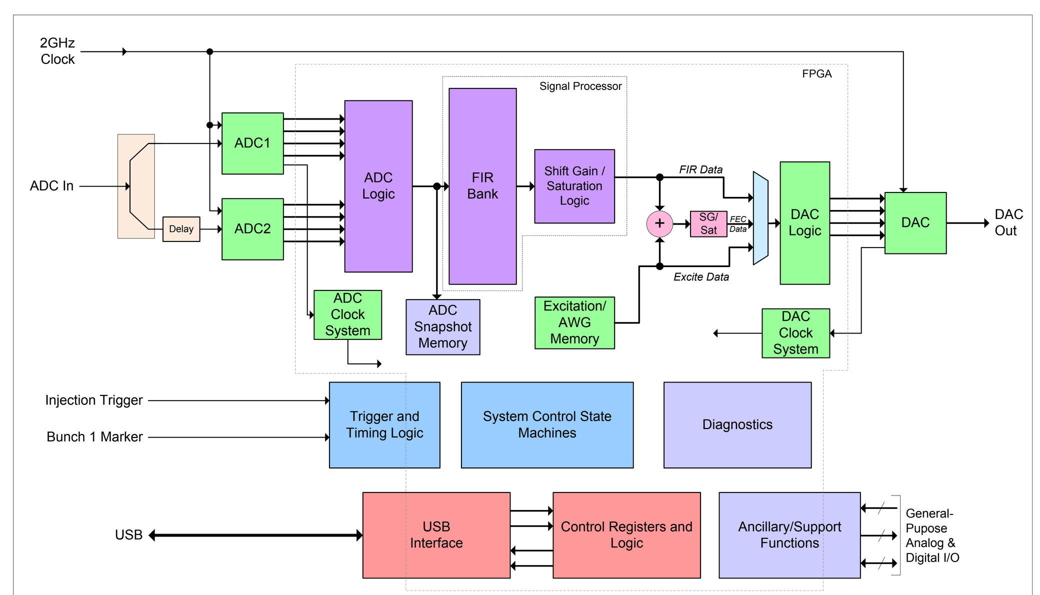


Analog Back End

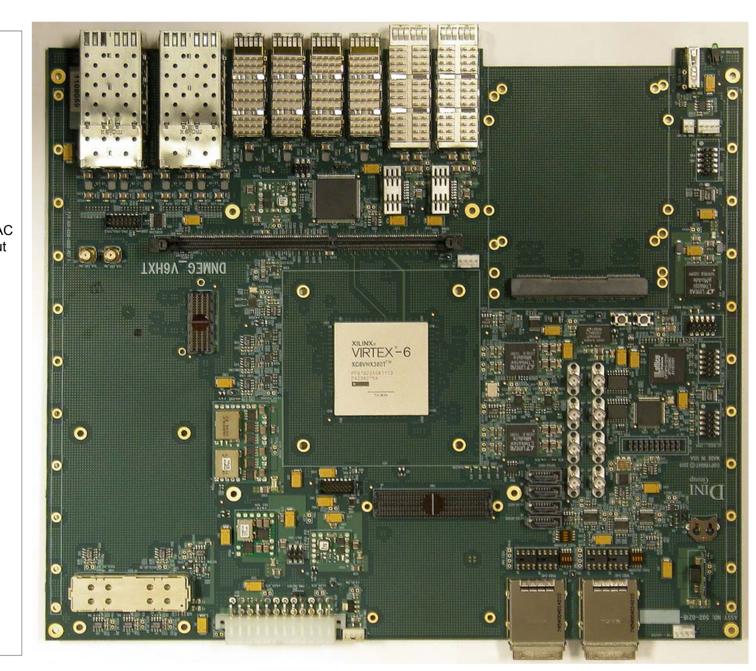
System Overview:

- We have built a single-bunch, ultrafast high bandwidth transverse feedback demonstrator system.
- This feedback system is essentially a high bandwidth re-configurable digital signal processing channel with an input ADC and output DAC capable of sampling at 4GSa/s. An FPGA implements the signal processor and the current design contains a 16-tap FIR bandpass filter.
- The feedback system acquires 16 samples or slices across one bunch, and outputs 16 correction samples, both at the 4GSa/s rate.
- For our measurements in the SPS, we the use Feedback and Excitation systems together, which allow us to drive the bunch into instability and then correct with feedback along the same signal path.
- Both sub-systems receive the RF Clock, Injection and Bunch 1 markers from SPS LLRF and Timing systems / used to synchronize and sequence operations;
- The 200MHz SPS RF Clock is multiplied to obtain the 2GHz sample clock, this clock is then doubled by the ADC and DACs to achieve 4GSa/s.
- Adjustable delay lines are included to align the input sampling, feedback output and excitation output to the beam bunch (10ps dly step resolution).
- RF Power Amplifier Specs: 0.02 to 1 GHz, 80 Watts (derated from 100W) / Manufacturer: Amplifier Research (Modular RF, Bothell, WA USA)

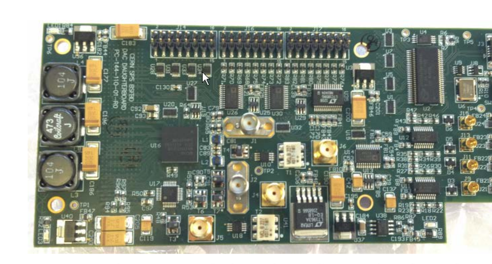
The Feedback Processor



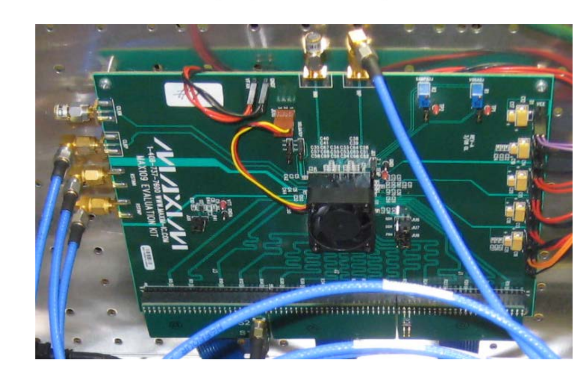
Feedback Processor Demonstrator Block Diagram



Commercial FPGA Motherboard



Custom High-Speed DAC Daughterboard



ADC Eval Board (1 of 2)

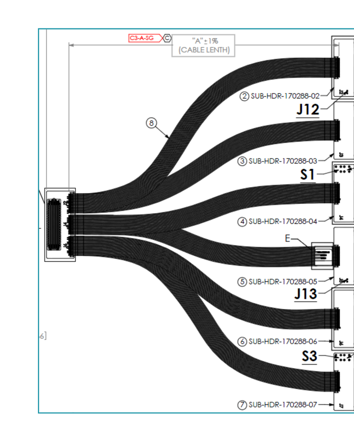
Feedback Processor:

- The Feedback Processor is a rapidly developed prototype, implemented using a mixture of commercial and custom-designed hardware. The entire system was designed, constructed and delivered to CERN in less than10 months.
- The design is modular, based around a commercial FPGA motherboard, with a custom-designed DAC daughterboard plus two commercial ADC evaluation boards. The ADC boards connect to the motherboard using a custom high-speed cable assembly, developed commercially (Samtec Corp). This design approach allowed us to quickly develop a solution within the confines of limited time and engineering resources.
- The custom DAC daughterboard contains the high-speed DAC, clocking circuits, trigger circuitry, general purpose analog and digital I/O and a USB 2.0 interface.
- The DAC is a Maxim Semi MAX19693 device (12-bit, 4GSa/s device used in 8-bit mode). The ADC is a MAX109 device (8-bits, 2GSa/s), two ADCs are used in interleaved mode to achieve the effective 4GSa/s rate. We used two MAX109 EVM evaluation boards to implement the ADC subsystem.
- All signal processing is implemented in the motherboard Xilinx Virtex-6, XC6VHX565T FPGA. The present design implements a bank of 16, 16-tap FIR filters. The filters are bandpass type, centered at the betatron frequency. The FIR Filters follow the relation:

$$y(n) = \sum_{k=0}^{15} h(k)x(n-k)$$

- Diagnostic features include a special ADC snapshot memory that allows us to selectively capture up to 65536 turns of pre-processed ADC data and save for later analysis.
- Feedback Processor can also operate as an excitation driver (arbitrary waveform generator) as well.
- All processing takes place on edges of the SPS RF clock. Acquisition, processing and output operations are sequenced from the SPS Injection and Bunch 1 marker signals.

System Chassis: all boards, cabling, cooling & power supply are packaged inside



Custom High-Speed ADC cable assembly: mates ADC eval boards to FPGA motherboard

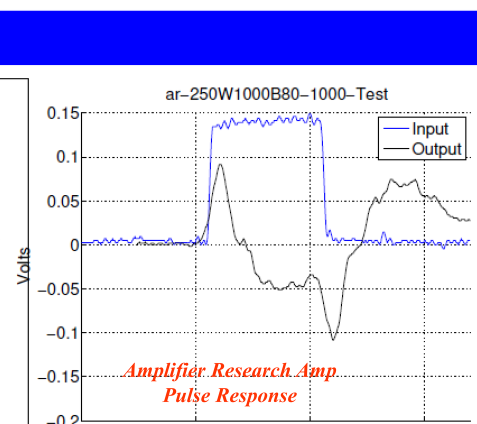
RF Power Amplifiers

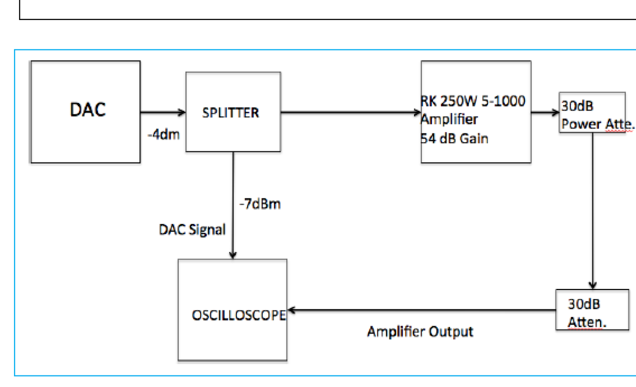
RF Power Amplifier:

Upgrades (require Pwr = 1KW, BW = 20MHz…1GHz)

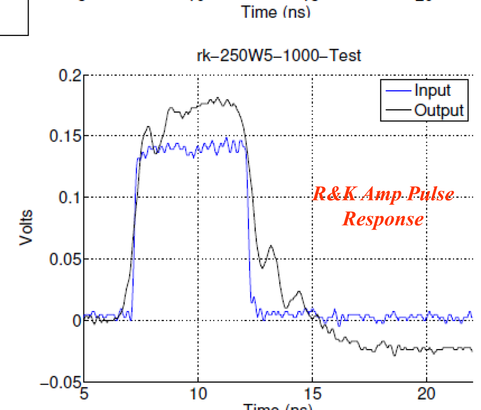
- Our Application requires that the RF Power Amplifier has good transient time-domain performance. This characteristic is typically not specified or tested for by manufacturers who are concerned with modulated CW operation. Therefore, we developed a test setup and methodology for evaluation of RF power amps in the time domain.

- Several different units were evaluated, with R&K Company Limited (Fuji-City, Japan) demonstrating the best performance.





Amplifier Test Setup



Measurements performed by O. Turgut / SLAC/Stanford Univ

Beam Kicker

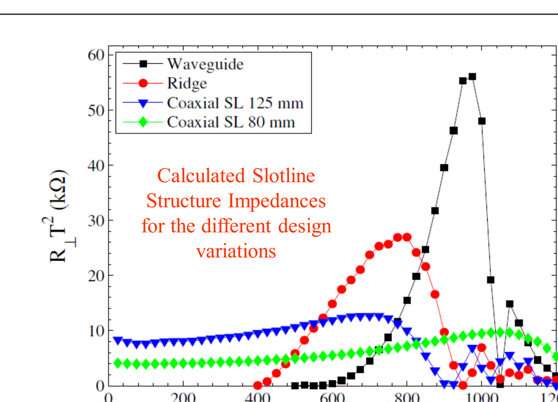
Kicker Structure:

Upgrades – The existing stripline structure at the SPS has limited BW (200MHz) and will not allow for correction of higher-order modes. Thus, a higher BW one needed to be developed

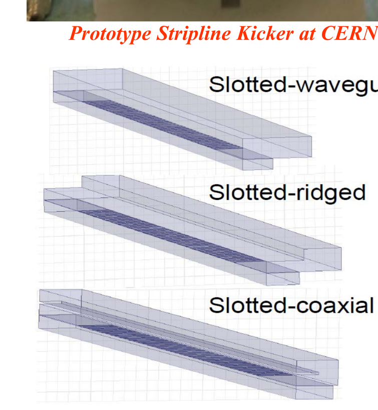
A design study was performed to evaluate three different types of kicker structures: Cavity, Slotline and Stripline. A design report was produced (SLAC-R-1037).

The Stripline and Slotline desings are being pursued.

- The Strlipline design has progressed to prototypes being developed, which will be installed into the SPS in Dec 2014
- The Slot Design is continuing to be developed.



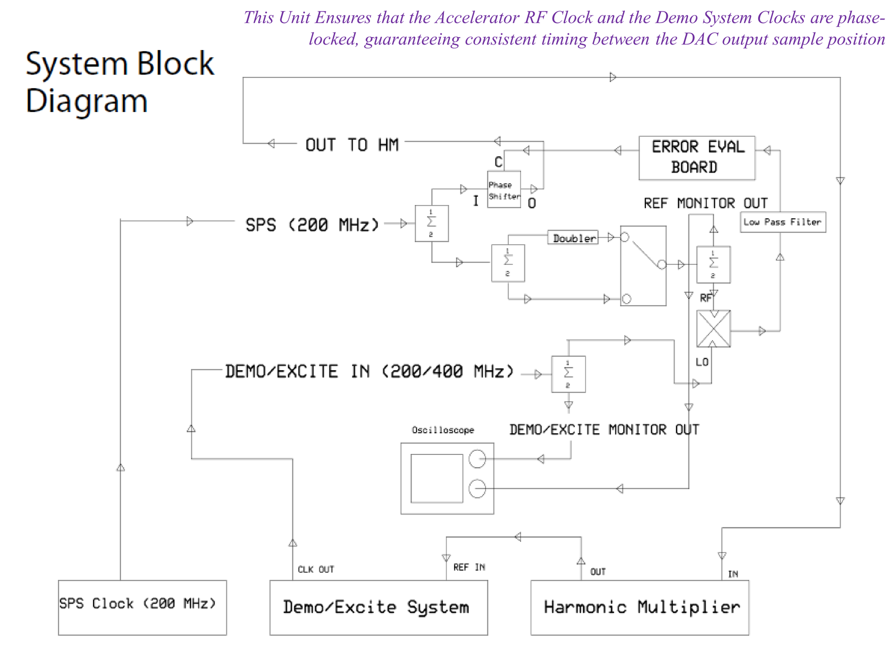
Prototype Stripline Kicker at CERN



Slotline Structure Designs

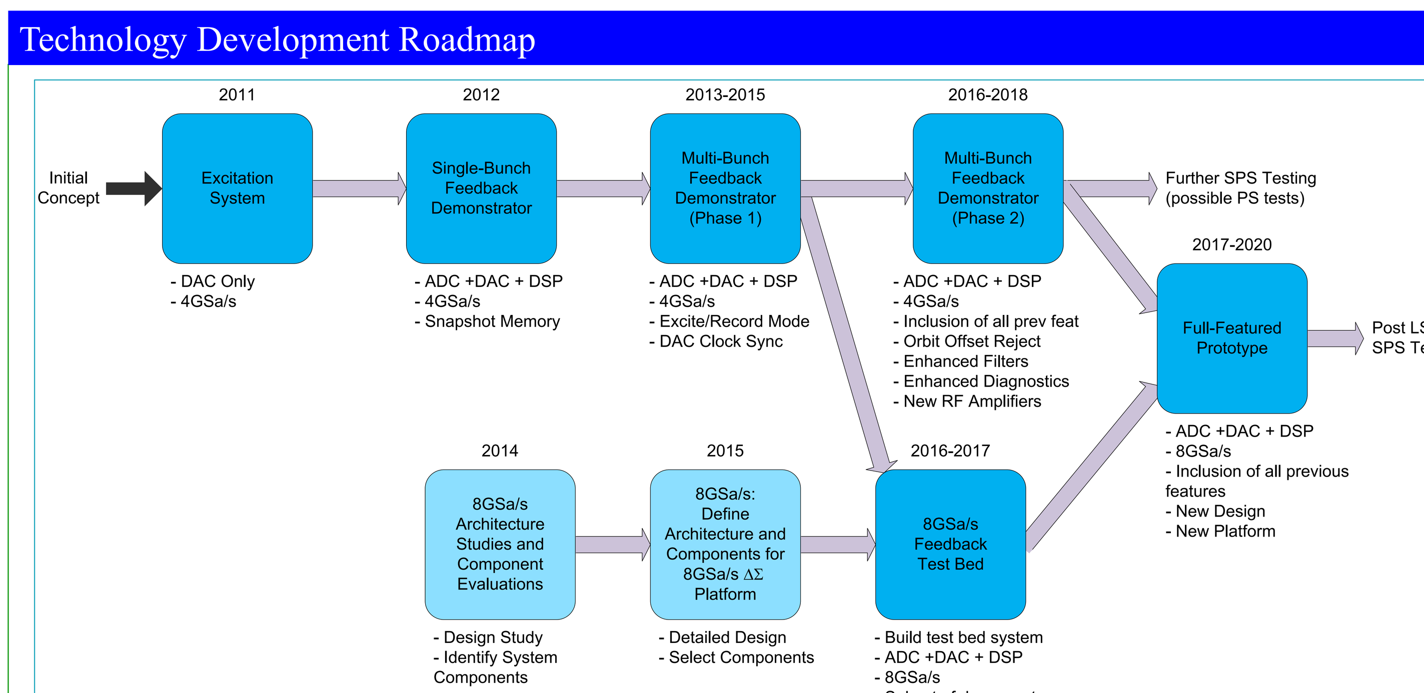
Demo Processor Support HW – PLL Chassis

This Unit Ensures that the Accelerator RF Clock and the Demo System Clocks are phase-locked, guaranteeing consistent timing between the DAC output sample position



Developed by J. Goldfield / Stanford University

Technology Development Roadmap



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