Development Status of SINAP Timing System

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Timing information with high precision is required to synchronize distributed devices and equipments in large accelerator facilities.

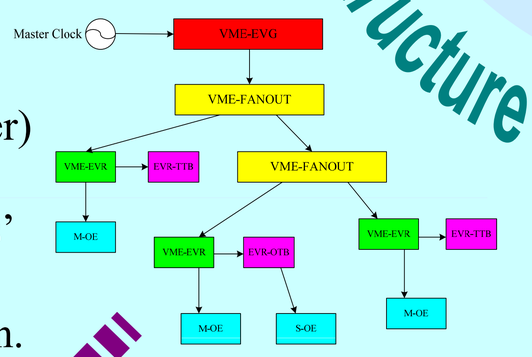
In the new version of SINAP timing system, bidirectional data transfer and EVG cascading function are supported. The hardware structure is also modified, where a versatile product, named VME-EVO, could be configured as EVG, FANOUT or EVR. Besides VME modules, PLC-EVR is developed as well, which complies with Yokogawa F3RP61 series. Based on upgraded hardware architecture, the jitter performance of SINAP v2 timing system is improved remarkably.

Introduction

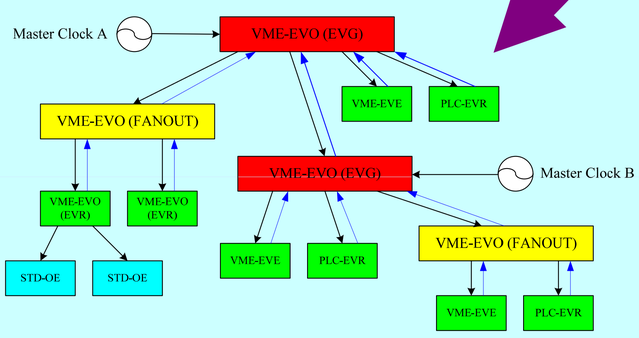
We started to develop SINAP timing system since 2007. SINAP v1 timing system was completed and implemented in Pohang Light Source II Project in 2010. Subsequently, we modified system design and improved performance in SINAP v2 timing system. The hardware development is completed so far.

History

SINAP v1 timing system adopts classic star broadcast topology. All of EVG (event generator), EVR (event receiver) and FANOUT are standard 6U VME modules. Output triggers' delay could be adjusted with coarse and fine delay resolution.



Structure



SINAP v2 timing system adopts similar topology based on fiber-optic network as well, but communication mode upgrades from simplex to duplex, which means that we could conduct deterministic data transfer and event distribution at the same time.

Features

1. Classic star network;
2. Bidirectional event frame transfer (not broadcast);
3. 2.5Gbit/s fiber-optic link;
4. Event clock from 60MHz to 135MHz;
5. EVG cascading function supported;
6. Hardware based on Virtex-6 FPGA;
7. All triggers delayed with multiple resolution;
8. A new versatile EVO could be configured as EVG, FANOUT or EVR;
9. PLC-EVR based on Yokogawa F3RP61 series.

1 byte	1 byte
trigger	data frame
K28.5	data frame
K28.5	data frame
K28.5	data frame
trigger	data frame
K28.5	data frame
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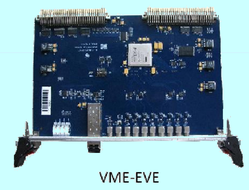
VME-EVO

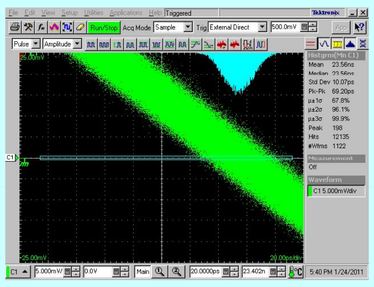

VME-EVE


PLC-EVR

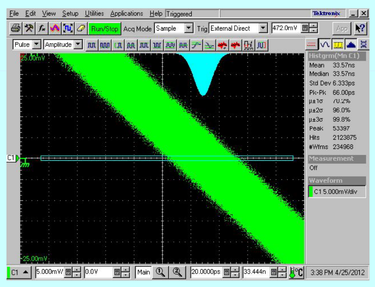

STD-OE

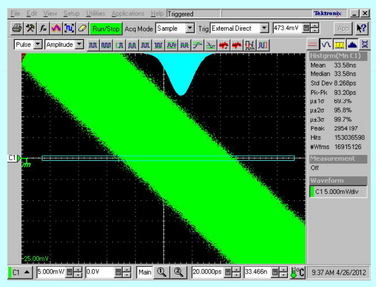
Performance

We made use of Tektronix TDS8000B oscilloscope and 80E03 Sampling Module to measure the short-term jitter between output trigger from EVR and RF reference clock of SINAP v1 timing system. The RMS jitter is about 10.1ps.



For SINAP v2 timing system, we made use of the same test bench to measure the short-term jitter between output trigger from VME-EVE and RF reference clock. The RMS jitter is about 6.3ps. The jitter performance of PLC-EVR is similar to VME-EVE. We measured the long-term jitter for 20 hours as well, which is about 8.3ps.





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