# ADVANCED LIGHT SOURCE TIMING SYSTEM UPGRADE*

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## Introduction

The primary function of the ALS timing system is to synchronize and sequence all systems required to deliver beam from the gun through the injection system to the storage ring. In addition, the timing system synchronizes diagnostics to the beam and provides controls for optimizing injection efficiency and selecting the operating mode.

A survey of similar, more modern accelerator timing systems revealed that the most common commercial solution for event-based timing systems was based on Micro Research Finland (MRF) hardware. In particular, NSLS-II had developed EPICS drivers for the MRF hardware in their timing system. MRF hardware was chosen as the platform for the new ALS timing system to accelerate development by leveraging demonstrated commercial hardware with EPICS drivers.

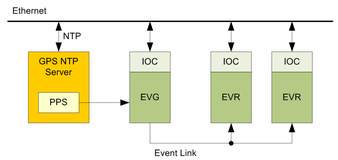



**Figure 1**. Timestamping block diagram. The timing IOCs get GPS time from the NTP server via Ethernet at boot time. The server also sends a GPS-locked Pulse Per Second (PPS) trigger to the EVG.

## Architecture

The ALS event system consists of a central Event Generator (EVG), event distribution using high speed serial transceivers, fiber optic cables, and electro-optical fanouts, and an array of Event Receivers (EVRs) placed as close to existing client signal inputs as feasible, or embedded in the system firmware of new clients. Each EVG and physical EVR resides in a VME crate with an IOC running EPICS connected to the ALS control system via Ethernet. The physical EVRs generate analog triggers and clock signals for the various existing client systems.

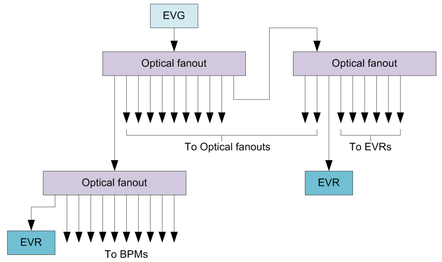



**Figure 2**. Optical event distribution block diagram. Events are transmitted from the EVG via 1:11 optical fanouts to EVRs and clients with embedded EVRs (i.e. BPMs).

## Embedded Event Receiver

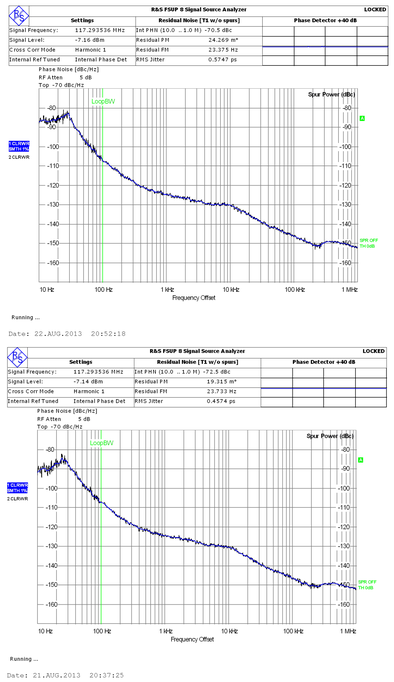
An MRF-compatible embedded event receiver was developed by NSLS-II and included in their accelerator instrumentation platform. This platform serves as the Digital Front End (DFE) board in the NSLS-II BPM chassis, which was adopted for use in the new ALS BPMs.

The NSLS-II embedded EVR was modified so that the phase relationship between the EVG event clock and the EVR recovered clock is fixed, permitting synchronous RF-based clock recovery. In the ALS BPM, the recovered clock is used to regenerate the orbit clock that is the reference for the BPM ADC sampling clock.

This modified embedded EVR has since been ported to the new ALS Bunch Current Monitor (BCM) system, where it is also used to derive an RF-synchronous reference for the sampling clock.

The embedded EVR was designed to use a Xilinx Virtex-6 series high speed transceiver. However, it is possible to port the design to another Xilinx device family or different FPGA vendor by replacing only the hardware-specific portion of the EVR code. This EVR only requires an FPGA with a high speed serial transceiver supporting transfer rates of 20x the event clock rate (2.5Gb/s for ALS) connected to an SFP port and a local reference clock close enough in frequency to the event clock rate that it can be used as a reference for the transceiver clock recovery PLL.

**Figure 3**. Phase noise measurements of the BPM ADC sampling clock. When the PLL reference is derived from the embedded EVR (top plot), the RMS jitter is ~570ps. When the reference is provided by the MRF EVR (bottom), the RMS jitter is ~460ps. There was no measured difference in the SINAD of the BPM.




## Event Sequence

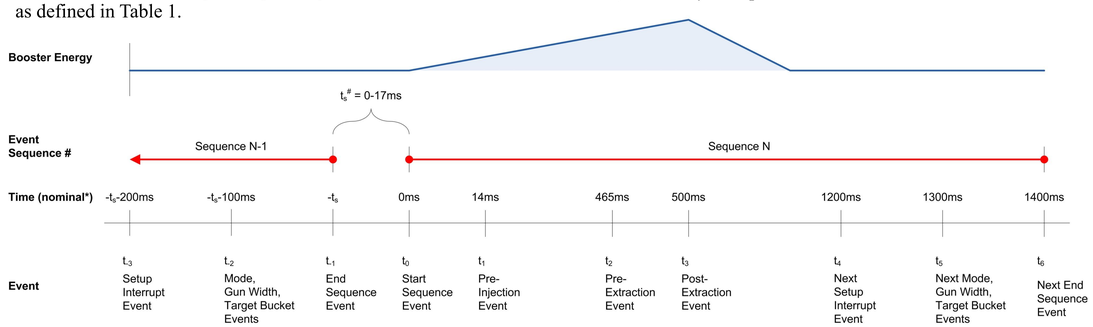
The Booster event sequence consists of a minimum of 7 event epochs, as shown in Figure 4. Before the Booster is ramped, some setup is required. Just over 200 ms before the start of the next sequence, the EVG sends the Setup Interrupt Event (event 62), which interrupts the master IOC (in the same crate). The interrupt triggers the IOC to read EPICS records containing parameters defining the next sequence, reset the mode to default (no beam), and increment the sequence number.

About 100 ms after the Setup Interrupt Event, the EVG sends 12 events (event 60 for binary 0, 61 for binary 1) that encode the Gun Width and Storage Ring Target Bucket values. Then the EVG sends one of the Mode Events (50-59). The modes cover the various anticipated operating modes of the accelerator, as defined in Table 1.

EVRs that use these parameters load the values into their interrupt FIFOs. When the EVR IOCs receive these interrupts, they shift the values into their local parameters, and then use this information to set up trigger enables and delays for the next sequence.

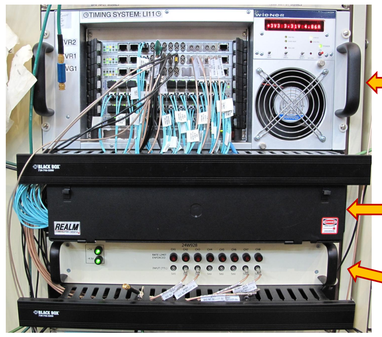
About 100 ms after the Mode Event is sent, the EVG sends the End Sequence Event (127). The EVG then waits for the next rising edge of the 60Hz line, followed by the rising edge of Coincidence Clock (COIC), which is generated by a free-running counter in the EVG. Once the EVG is synchronized to these signals, the next sequence can begin.

At the start of the sequence, the EVG sends out the Start Sequence Event 10 and enables the event sequence counter. Pre-Injection, Pre-Extraction, and Post-Extraction events are then sent according to the timestamps in the sequence table. After the Booster ramp is complete, the EVG sends the next Setup Interrupt Event, and the cycle repeats.




*Time values are approximate since events occur in multiples of $4/f_{RF}$ (~8ns).
$^{\#}t_s$= the variable time to synchronize to the AC Line (16.666ms) and then Coincidence Clock (~82us).

**Figure 4**. Timing Event Sequence. The event epochs are shown with respect to relative time, event sequence number, and Booster Energy.




Main timing VME chassis, including EVG, 2 EVRs, 4 optical fanouts, and IOC CPU.

Main fiber optic distribution chassis connects central optical fanouts to trunk cables feeding entire accelerator.

TTL Translation/Rate Limit chassis provides signal translation to existing timing clients.


Each sector has a satellite fiber optic distribution chassis to connect the trunk cable to local optical fanout.

1U VME chassis containing local optical fanout.

BPMs in each sector receive timing directly from optical event link (aqua cables).

## Conclusion

The ALS timing system upgrade combines mature and widely used commercial hardware with custom hardware for ALS-specific functions and interfaces. This allowed a reduction in the scope of the project while providing a flexible, expandable and event-based timing master. Leveraging the NSLS-II embedded EVR firmware and MRFIOC2 EPICS support greatly accelerated development.

Building the RF-clock recovery into the embedded EVR reduced the number of MRF EVRs and physical connections needed, significantly reducing equipment installation, cost, and maintenance in the long-term. The embedded EVR can be included in any new instrumentation firmware requiring machine timing.

A flexible and configurable event sequence scheme provides support for existing and future modes of ALS operation. Timestamps are accurate and precisely synchronized across all timing system clients, providing a level of multi-system diagnostic data correlation previously unachievable at ALS.

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