DEVELOPMENT OF A HIGH SPEED BEAM POSITION AND PHASE MONITORING SYSTEM FOR THE LANSCE LINAC*

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Abstract

The Los Alamos Neutron Science Center (LANSCE) is currently developing beam position and phase measurements (BPPMs) as part of the LANSCE risk mitigation project. BPPM sensors have been installed in the 805-MHz linac and development of the monitoring electronics is near completion. The system utilizes a high speed digitizer coupled with a field programmable gate array (FPGA) mounted in a VPX chassis to measure position, phase and bunched-beam current of a variety of beam structures. These systems will be deployed throughout the LANSCE facility. Details of the hardware selection and performance of the system for different timing structures are presented.

INTRODUCTION

Development efforts at LANSCE over the last year have been focused on creating a new electronics system to measure the beam position, bunched-beam current and phase of particles for the variety of time structures and species accelerated in the LANSCE 805-MHz side coupled linac. This system will replace the legacy ΔT system used during accelerator tune-up and also provide valuable transverse beam information during beam production which is not currently monitored.

ARCHITECTURE

The design of the system requires capturing signals from 4-electrodes of a beam position and phase monitor (BPPM) along with the accelerator reference signal. The signals are then conditioned to 201.25MHz RF waves. The five signals are then digitized and analyzed by a digital signal processor (DSP) to convert waveforms to position, phase and bunched-beam current. Processed data is provided to the end user through channel access managed by EPICS. [1] The system architecture is shown in Figure 1.

A high speed digitizer was selected to capture data at a 4-nanosecond time increments in order analyze beam position and phase variations that occur throughout the 1 millisecond pulse cycle. A field programmable gate array (FPGA) is being used for the DSP to analyze these signals in different timing modes such as long pulse (50 µsec), short pulse (150 nsec), and single shot (1 nsec).

A soft core processor, which resides in FPGA fabric, is used to store the results to the EPICS database for use by beam operators and other users.

Timing for synchronous measurements between BPPMs and beam specific information is provided by an event receiver connected to the master timer via optical links. The BPPM results are then stamped with the timing and beam species information prior to submission to the EPICS database. A real time operating system is used to collect data and match it with the correct timing information for each cycle of the beam.

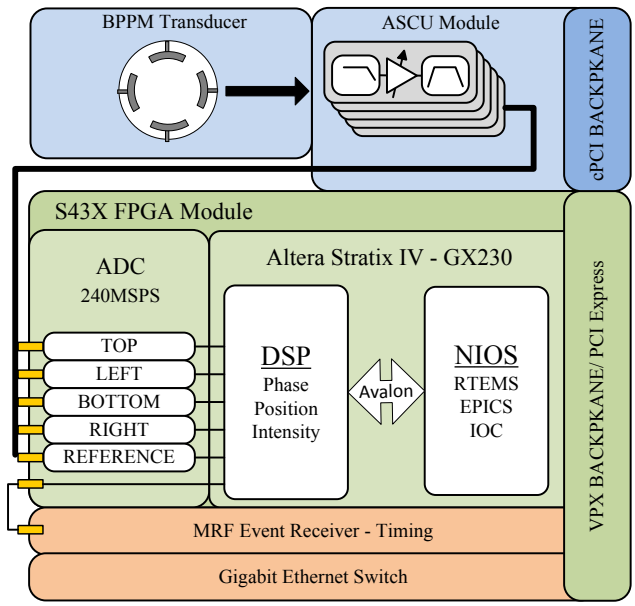

Figure 1: BPPM architecture.

REQUIREMENTS

The requirements for the BPPM system were broken up into two main regimes. The first regime is phase requirements that translate to time of flight (ToF) and energy measurements. These measurements are used to determine the phase set points for the acceleration modules. The second regime is position measurements that determine the transverse location of the beam centroid [2, 3].

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Phase Requirements

Phase requirements were driven by the existing system which provides good measurements but many of its components have reached end of life. The original specification for this system required a ToF accuracy of 13.8psec which is approximately 1 degree at 200-MHz [3].

In addition the system must be capable of taking simultaneous measurements between two sensors to support tuning and provide results at 120-Hz operation.

Position Requirements

Position requirements did not have a legacy specification but were driven by experience with other BPM's at LANSCE such as the proton storage ring. Requirements were set based on what would be useful to users tracking problems with other systems, beam optimization and analyzing variation in positions over small time increments. Table 1 below details the requirements for signal levels, precision, accuracy, averaging and range.

Table 1: BPPM Requirements [4]

	Long Pulse	Short Pulse	Single Pulse
Minimum Charge	5 pC (1 mA peak)	5 pC	30 pC
Maximum Charge	100 pC (20 mA peak)	100 pC	150 pC
Phase Precision	0.25 deg	1.0 deg	n/a
Phase Accuracy	1.0 deg	2.0 deg	n/a
Averaging Window	50 us	150 ns @ 2.8 MHz	n/a
De-bunch Range	18 dB	n/a	n/a
Position Precision	0.1 mm	0.1 mm	
Position Accuracy	1.0 mm	1.0 mm	2.0 mm
Transducer Radius	50% (13 mm)	50%	
Phase Resolution	1 µdeg	1 µdeg	n/a
Position Resolution	1 µm	1 µm	1 µm

These requirements set the overall dynamic range listed in Table 2.

Table 2: Dynamic Range Budget

Charge range	26 dB
De-bunch range	18 dB
Max Current, position range	4 dB
Noise Floor Margin	10 dB
Total Dynamic Range	**58 dB**

In addition to these requirements some additional features were requested and will be supported by the new system.

- In-situ calibration of path losses
- Single pulse measurement capability
- EPICS timed and flavoured data
- Provide data to multiple clients

DEVELOPMENT

Analog-to-Digital Converter

The dynamic range requirement set the ADC performance specification for a minimum effective number of bits (ENOB) at 10-bits. This led to the choice of using the TI ADS62P49 analog-to-digital converter since it met both the ENOB requirements and the high speed sampling requirement. This 8-channel digitizer was available as an off the shelf part from 4DSP in a FPGA mezzanine carrier (FMC) form factor [5], allowing it to be interfaced to an Altera Stratix IV FPGA carrier [6].

Figure 2 shows how these two boards become a single module that is placed in a VPX chassis. This module is the main payload card for the design. It does all the digitizing, DSP analysis, system configuration, software execution and EPICS control.

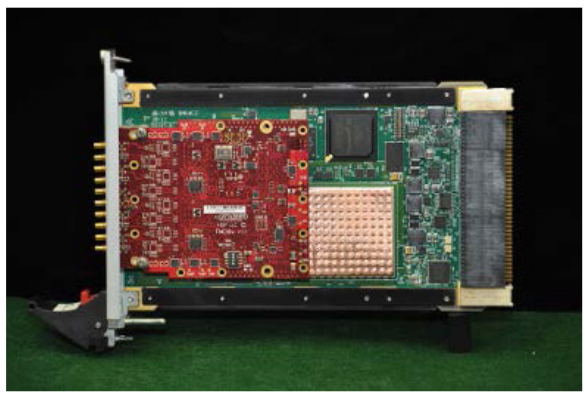

Figure 2: FPGA carrier with ADC mezzanine card.

Analog Conditioning

An analog-signal conditioning unit (ASCU) was developed in house to condition the BPPM's beam doublet signals to fall within the amplitude and frequency range of the ADC inputs. The ADC's full scale range is 2 Vp-p or +10 dBm. Typical BPPM signals for 1mA peak beam are -40 dBm with maximum signal at 20mA peak reaching -10 dBm. To optimize the headroom of the ADC the ASCU not only filters the beam doublets to pass 201.25-MHz but increases gain by 20-dB to take full advantage of the ADC's range.

Digital Signal Processing

The main effort has been in developing and testing the DSP algorithm. This is an under-sampling architecture where the sampling bandwidth is high enough to show

modulation effects of the 201.25-MHz signals but analysis is performed in the FPGA on the aliased signal at 38.75-MHz. The reference signal is sampled and then split into its in-phase and quadrature-phase (IQ) components. This is then used to convert the electrode signals to separate IQ signals. These IQ components can then be used to calculate phase and amplitude for each electrode. Phases are then averaged for all four electrodes and amplitudes are used in a look up table that interpolates the position based on amplitude maps of the sensor.

Timing

The timing network triggers synchronous measurements of BPPM systems. Distributing this timing to all BPPM's allows for a single beam pulse to be measured as its travels down the linac. These timing cards are manufactured by Micro-Research Finland. This system is able to pass triggering information every 10 nanoseconds and provide timestamp and beam species information over the optical link.

Network

The network link is passed from the network switch in the chassis over PCI express to the other payload slots in the VPX chassis. This allows an EPICS IOC running on the FPGA's soft-core processor to communicate over the LANSCE network.

Figure 3 shows the four cards that make up the full system architecture.

Figure 3: ASCU, FPGA, timing and network cards.

TESTING

Testing was done to measure both the position and phase performance of the system. Phase performance testing used a 5-channel phase locked synthesizer to provide simulated beam signals from each electrode and a reference signal. All five channels were phase aligned and calibrated prior to testing.

Position was measured on a wire map system, used previously to characterize BPPM probes. This wire map system has laser micrometers for alignment and the positional error is less than 5 microns. This system simulates beam by exciting a wire with RF energy at 201.25-MHz. A 3-axis table then moves the wire through a mapped sequence inside the clear aperture of the probe.

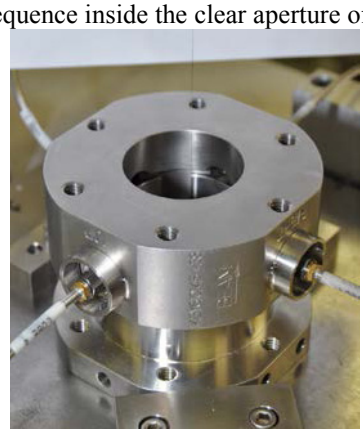

Figure 4: BPPM mounted to wire map table.

Initial testing of the DSP algorithm showed an oscillation in position and phase accuracy across a 360 degree phase sweep. Two problems were causing this oscillation. It was shown in Matlab simulations that an oscillation of the position could occur given a DC offset on the reference signal [7]. This first problem was fixed by turning on the DC cancellation mode of the ADC and using an extra sample in the quadrature calculation.

The second problem found was isolation in the ADC card between channels. The reference signal comes in at a high level and the ADC channels adjacent to the reference were picking up interference. The reference signal was moved to a separate ADC chip with a spare channel spaced in between. This solution provided enough isolation to remove any oscillations in position and phase.

PERFORMANCE

Phase

Results of accuracy, precision and linearity are given below for a 50-dB signal level sweep in power and 360-degree phase sweep.

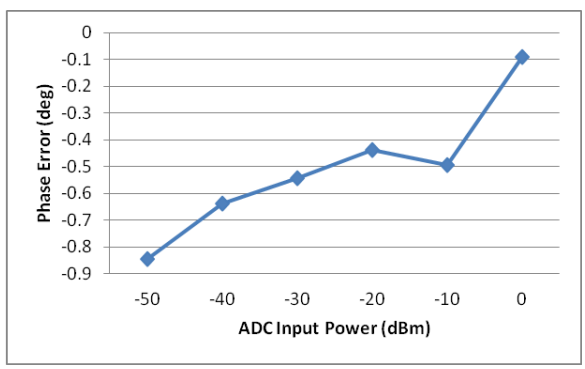

Figure 5: Phase accuracy (< 1.0 deg).

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Results in Figure 5 show the phase accuracy requirement of 1 degree is able to be met down to -50 dBm referenced to the ADC input for long pulse mode.

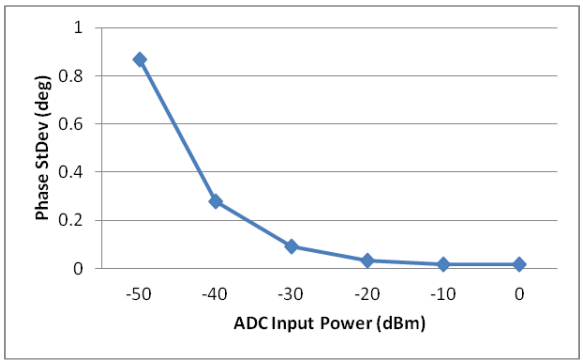

Figure 6: Phase precision (< 0.25 deg).

Phase precision graph in Figure 6 shows that the requirement of 0.25 degrees can be met down to -40 dBm. Typical electrode power for tuning is -35 dBm at the input of the ASCU. If the ASCU is set to 15dB of gain the system can meet the precision specification.

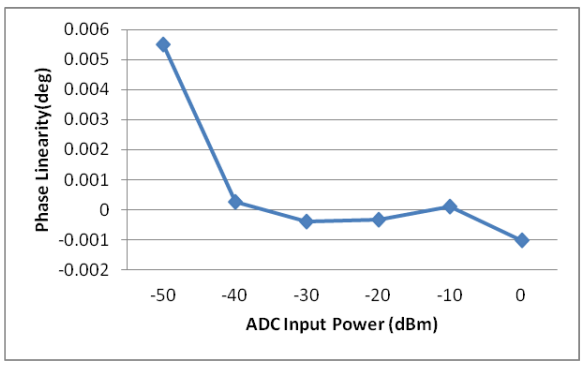

Figure 7: Phase linearity vs ADC input power.

Phase linearity did not have a specific requirement but is shown in Figure 7 to demonstrate how well the algorithm responds to increments in phase. The delta T procedure ultimately uses the relative difference in phase when the tank acceleration is on and off to determine the correct phase set point.

Position

Results for position accuracy and precision are displayed below. Position results were taken in a 13mm radius map in 1mm steps. Power levels for this test were taken at -25 dBm at probe center from each electrode. This level is about 10-dB lower than what would be expected for long pulse tuning beam in the accelerator.

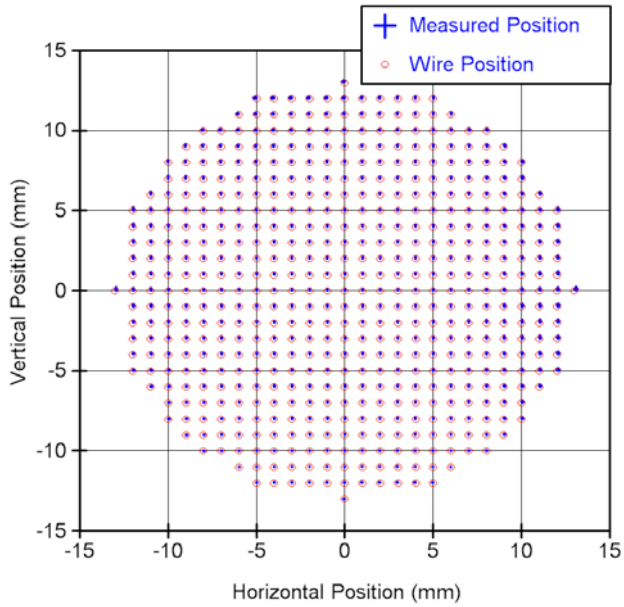

Figure 8: Wire position vs. measured position.

Figure 8 shows measurements on an actual BPPM sensor where the red circles are the commanded position of a thin tungsten wire. The blue + sign's center is the measured position by the BPPM electronics, with error bars showing the standard deviation. The precision is difficult to recognize in the plot since it is so small in comparison to the incremental step of 1-mm. Results are well within specifications for up to a 50% radius of the BPPM.

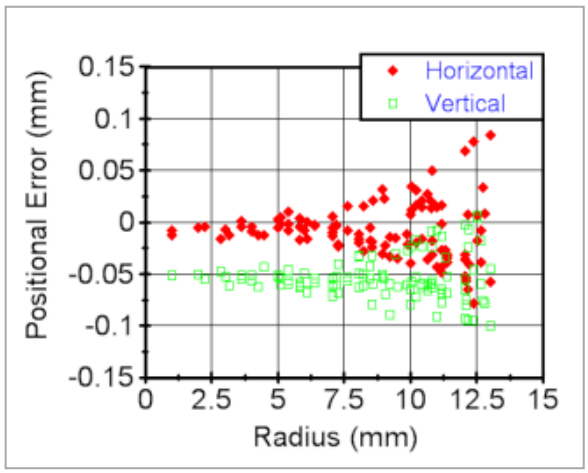

Figure 9: Position accuracy (< 1mm).

The positional error graph in Figure 9 shows that accuracy and precision of the system degrades as beam centroid approaches the outer radius of the aperture. This is expected given that the electrode power opposite the position change is being reduced in power level and is more susceptible to noise.

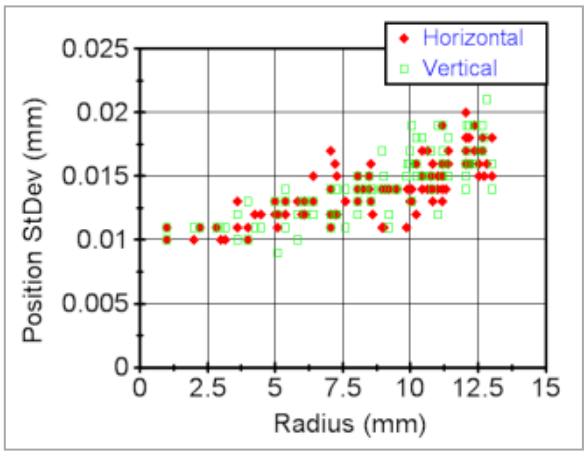

Figure 10: Position precision (< 0.1mm).

The position precision graph in Figure 10 shows that 0.1-mm of precision is achievable. Precision decreases slightly as beam approaches the outer limit of the aperture. Precision also degrades as the input level to the ADC is reduced. Figure 11 shows that the 0.1-mm precision requirement can be met as long as signal levels stay above -40 dBm. To achieve lower levels of sensitivity the gain of the ASCU will be increased.

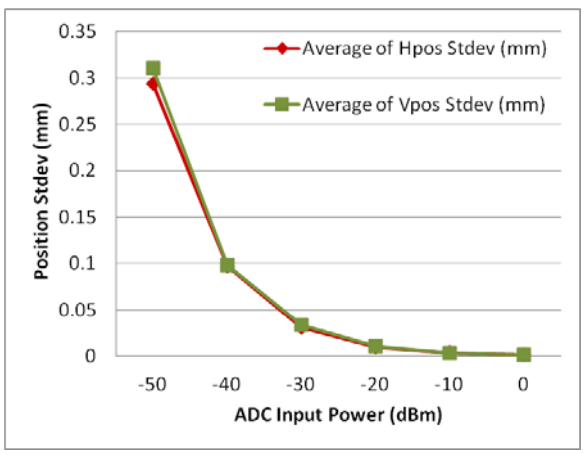

Figure 11: Position precision vs. ADC input.

These results were all taken with 30-µsecond averaging where the DSP is analyzing results every 1 µs. Accuracy and precision may show a slight improvement once the averaging is increased to 50 µs and the ASCU unit is placed in front of the ADC. These results are based on the long pulse mode of the DSP. The short pulse and single pulse modes need to be fully characterized along with actual beam measurements.

SOFTWARE INTEGRATION

The remaining steps to get this system deployed and data provided to the accelerator operators is the software components. There are two main areas that need to be integrated. The NIOS II soft-core processor must be instantiated in the FPGA design with the DSP code. Once the NIOS is able to collect data from the DSP and stamp it with timing information it is ready for upload to the EPICS database. This will allow multiple clients to subscribe to BPPM data for the variety of beam species and timing flavours that exist at LANSCE.

CONCLUSION

A high-speed beam position and phase monitoring system has been developed at LANSCE that meets all the intended requirements. There is still some work left to complete final deployment to the beam line that should be completed in early FY15. In all, approximately 40 systems will be deployed along the LANSCE SCL with proposals of extending this system to LANSCE's isotope production facility and proton storage ring.

REFERENCES

[1] R. McCrady, H. Watkins. "BPPM Design Review" Presentation, September 2013.
[2] J.D. Gilpatrick "Proposed beam position and phase measurements for the LANSCE LINAC" DIPAC, Venice, 2007, TUPB10, p. 78 (2004).
[3] I. H. Campbell, "LAMPF DELTA-T Hardware Review".
[4] R. McCrady. "Requirements for measurements of beam position and phase in the LANSCE risk mitigation project" Personal Email, September 2013.
[5] 4DSP, "FMC108 high pin count FMC ADC, 8-channel 14-bit ADC – 250MSPS" FMC108 datasheet, www.4dsp.com.
[6] Bittware, "S4-3U-VPX Commercial & Rugged Altera Stratix IV GX 3U VPX Board with Optional VITA 57 FMC for I/O" S43X datasheet, May 2014.
[7] Matlab R2012b. Mathworks Inc, Massachusetts, USA, 2012.

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