

# DESIGN, DEVELOPMENT AND COMMISSIONING OF A MTCA-BASED BUTTON AND STRIP-LINE BPM SYSTEM FOR FLASH2

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## Abstract

The FLASH (Free Electron Laser in Hamburg) facility at DESY (Deutsches Elektronen-Synchrotron) in Germany has been extended by a new undulator beam line called FLASH2 to provide twice as many experimental stations in the future [1]. After the acceleration of the electron bunch train up to 1.2 GeV, a part can be kicked into FLASH2, while the other is going to the old undulator beam line. In order to tune the wavelength of the SASE (Self Amplified Spontaneous Emission), the new line is equipped with variable gap undulators. The commissioning phase of FLASH2 started in early 2014 and continues mostly parasitically during user operation in FLASH1. One key point during first beam commissioning is the availability of standard diagnostic devices such as BPM (Beam Position Monitor) [2]. In this paper we present the design and first operational experience of a new BPM system for button and strip-line monitors based on MTCA.4 [3]. This is referred to as LCBPM (low charge BPM) in contrast to the old systems at FLASH initially designed for bunch charges of 1 nC and higher. We summarize the recent analog and digital hardware development progress [4, 5] and first commissioning experience of this new BPM system at FLASH2 and present a first estimation of its resolution in a large charge range from 1 nC down to 100pC and smaller.

## INTRODUCTION

The demand for beam time at the user facility FLASH increased substantially in the past. In order to fulfill this need the FLASH facility has been extended by a new undulator beam line for SASE generation called FLASH2. The charge delivered to FLASH2 can be adjusted independently from the old FLASH facility with an independent laser. FLASH2 has been ready for electron beam commissioning in March 2014, has seen the first beam on 4th March and was able to deliver SASE for the first time on 20 August 2014 [6, 7]. This was done simultaneously during SASE delivery in the FLASH1 undulator beam line. The electron beam delivered to FLASH2 is accelerated within the same RF (Radio Frequency) pulse in the FLASH facility up to 1.2 GeV after approximately 150 m and is then kicked into the FLASH2 tunnel. One part of the diagnostics in FLASH2 are button and strip-line monitors at 16 locations in the machine utilizing new MTCA.4 electronics designed by us [4, 5]. Challenges in the development of this system are the resolution requirement of 50  $\mu\text{m}$ , operation at charges well below 100 pC and a high bunch repetition rate of up to 4.5 MHz. This is compatible with the requirements for the European

XFEL [8]. The hardware development status and operation experience with these new systems are summarized in this paper.

## OVERVIEW

The new FLASH2 undulator beam line runs in parallel to the old FLASH1 undulator beam line which can be seen in Figure 1. It is divided into several sections namely EXTRACTION, SEED, SASE, BURN, and DUMP section with button and strip-line monitors in different locations. Most

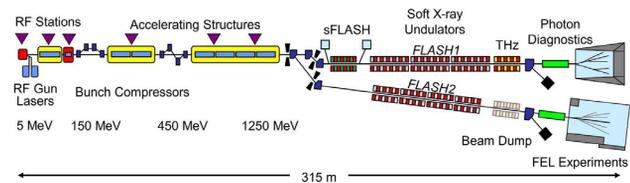


Figure 1: Section overview FLASH.

of the LCBPMs are distributed along the EXTRACTION section at the beginning of FLASH2 with nine BPMs and the rest of 4 BPMs are in the BURN/DUMP section. Due to space limitations in the SASE section three button BPMs have been installed here as well instead of using the more preferable cavity BPMs which offer the required resolution for orbit tuning in the SASE section [9, 10]. A variety of different beam pipe diameters for the button BPMs and a few refurbished strip-line BPMs with different RF cable lengths ranging from 35 to 58m installed in the machine required the development of a very robust but also flexible BPM electronics. The button type design is the same as for the European-XFEL that has been reported in [11]. Table 1 summarizes all types of BPMs for which the electronics are currently in operation. Electromagnetic field simulations [12] delivered the monitor constants. An overview of

Table 1: Types of Beam Position Monitors Installed in FLASH2 and Corresponding Monitor Constants

Type	amount	Diameter	Monitor constant
button	2	40 mm	10.6 mm
button	4	34 mm	9.06 mm
button	3	100 mm	23.84 mm
strip-line	4	44 mm	8.678 mm
in-air	1	100 mm	31.25 mm
button	3	10 mm	2.55 mm

the connections between the BPMs and readout electronics can be seen in Figure 2.

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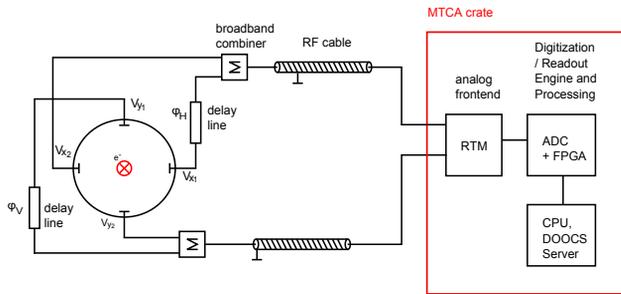


Figure 2: Overview Beam Position Monitor System.

The beam excited RF signals in the horizontal and vertical plane are combined after a delay of 100 ns to suppress interference with the next bunch in the train. This so-called Delay Multiplex Single Path Technology (DMSPT) [13, 14] method has been successfully in operation for many years in HERA<sup>1</sup> at DESY. It successfully proved to suppress the common mode EMI disturbances on the RF cable from the tunnel to the electronic racks. It also reduces the number of necessary ADC (Analog Digital Converter) channels for each BPM. The electronics for signal conditioning and processing are separated into an analog and digital card. The two cards are housed in a MTCA.4 crate. The position calculation takes place in the Firmware on the digital card and is given by the normalized difference of the signal on opposite electrodes [15]. This position information can then be read from a device server which can display the position in a panel.

## ELECTRONICS

### Analog Electronics

The BPM signals delivered to the electronics rack have a rise-time, fall-time, and duration in the order of a few 100 ps. Since it is very difficult to sample such a signal even at a high sample rate, these signals are pre-conditioned for digitization and processing on a custom made RF module. This makes it also easier to sample the signal and achieve the necessary resolution of the entire BPM system. Such a RF module has been designed and developed following the specifications of the MTCA.4 standard for RTM (Rear Transition Module). Each RTM has two RF channels that can measure beam position from one BPM using the delay-line multiplex method. A picture of the analog RF front-end is shown in Figure 3.

The filtering and amplification in the RF receiver signal path has been designed in a way to guarantee a dispersion free signal transport. This has been done to avoid interference between the two signals of each plane and to increase the integrity of the original signals along the signal path. The signal paths consists of a cascade of amplifiers and step attenuators and a peak-hold detector circuitry with a discharge switch. The peak amplitude from the amplified RF signal is detected with a Schottky diode and its value is tracked by a

<sup>1</sup> Hadron Elektron Ring Anlage



Figure 3: Rear Transition Module RF front-end.

capacitor. The discharging of the hold capacitor takes place after a time of approximately 40 ns and is adjusted by the timing settings in the custom made firmware. A picture of a single RF channel is shown in Figure 4.

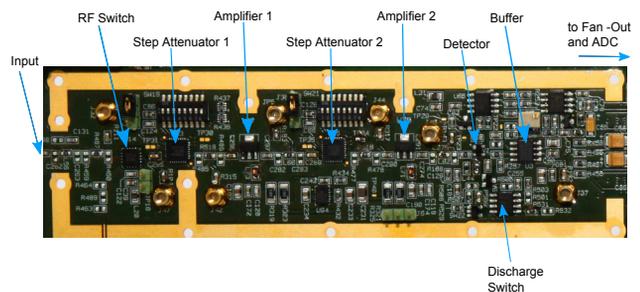


Figure 4: Single channel RF front-end.

The functionality of the electronics at low charge requires high gain in the receiver channel. The maximum gain of a single RF channel is on the order of 38 dB with a 3 dB bandwidth of approximately 600 MHz. Primarily the two step attenuators are used to adjust the signal strength for different charges with a dynamic range higher than 60 dB, while the step attenuator 2 can also be used to optimize the position measurement resolution for large beam offsets. Currently the information for signal level attenuation is loaded manually into the step attenuators. Before the analog signal is digitized it is distributed in a fanout stage for sampling by four ADCs in parallel for optional averaging. The analog bandwidth at the output of the fanout stages is approximately 230 MHz.

### Digital Electronics

The digitization and signal processing takes place on a digitizer board containing ten ADC channels and a FPGA (Field Programmable Gate Array) [16]. The analog RF front-end and the digitizer board are connected to each other via a high speed connector keeping the signal integrity with the required analog bandwidth up to the ADCs. The pre-conditioned analog signals are buffered and filtered in front of the ADC channels and are then digitized by 16Bit at a rate of 125MSPS. The custom made firmware (FW) on the FPGA is operating in real time and delivers bunch by bunch information at its output registers. The FW contains registers to adjust the step attenuators on the analog RF

front-end and a state machine to control the discharge of the hold capacitors on the analog board. The FW can operate in four different modes of which two are capable to work independently from the timing system as described in [5]. The timing coupled FW operating mode uses the bunch train trigger, ADC clock, and charge information as delivered by the timing system. This mode is the most stable from all modes. An AGC (Automatic gain control) based on the charge information will adjust the step attenuators on the RF front-end for optimized position reading resolution. This mode is currently under development and intended to be the most stable mode. The mode currently in operation at FLASH2 is the so called quasi-autarcic mode. In this mode the FW receives an external pre-trigger from the timing system. All other bunch related timings such as the hold capacitor discharging signal on the RTM, and the calculation of the bunch position are derived from this initial trigger inside the FW. The ADC clock is also generated locally independent of the FLASH2 timing system.

## SYSTEM INTEGRATION

### *Crate System and Timing*

The analog and digital cards for all 16 BPMs have been installed in 19" MTCA.4 crates with twelve AMC slots on the front and ten RTM slots on the back side. A maximum of five BPMs are installed in each crate to minimize interference between the neighbouring cards. Two of the crates in operation carry five, one carries three, and one carries four BPM electronics. The power module, the MCH (management carrier hub), the CPU and timing system receiver board and the digitizers are installed on the front side of the crate. The trigger from the timing system to the digitizer is delivered on a dedicated line on the backplane. The crates are located in a technical site next to the FLASH2 tunnel in climatized racks. An example installation for five BPMs from the EXTRACTION section in FLASH2 is shown in Figures 5 and 6.

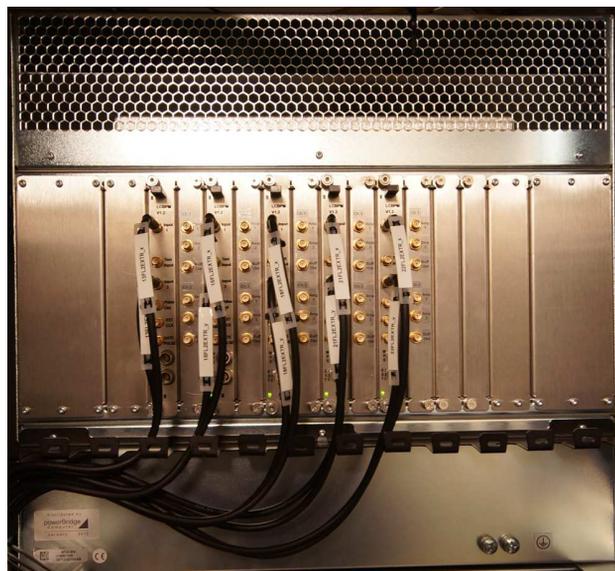


Figure 6: Rear View of a MTCA crate carrying five LCBPMs at FLASH2.

### *Driver and Software*

The position information calculated in the Firmware is read out by a customized driver from a PCIe bus system to which all modules are connected in the crate. The links on this PCIe bus can be configured in the MCH. A device server application running on the system CPU is polling FW registers on the digitizers, which are connected via the PCIe bus. This server can be accessed remotely over ethernet and its content can be visualized by use of control system panels.

## MEASUREMENTS

A typical distribution of position readings over 200 pulses from a strip-line BPM is shown in Figure 7 and 8. This measurement has been taken at a charge of 36 pC measured at a beam charge monitor located closest to the BPM. Similar results have been taken at higher charges up to 300pC which indicates that the electronics is not at its resolution limit. It is possible to steer the beam through an aperture of  $\pm 10$  mm for most BPMs without the need to adjust the second step attenuator. For both planes a standard deviation around  $20 \mu\text{m}$  has been obtained.

The standard deviation for all BPMs in the extraction section is below  $50 \mu\text{m}$  at charges lower than 50 pC for a centered beam but increases in the dump section to values in the order of  $100 \mu\text{m}$ . In the current setup the three BPMs in the SASE section do not deliver sufficient signal amplitude for measurements. This will be overcome with additional pre-amplification of the BPM signal in the future. The fulfillment of the specifications for  $50 \mu\text{m}$  position resolution at charges well below 100 pC has been shown for single-bunch operation at bunch repetition rates up to 1 MHz in the current state of commissioning. Increased BPM performance can be expected from bunch synchronous measurements from all FLASH2 BPMs in order to remove the correlated electron beam jitter from the position readings.

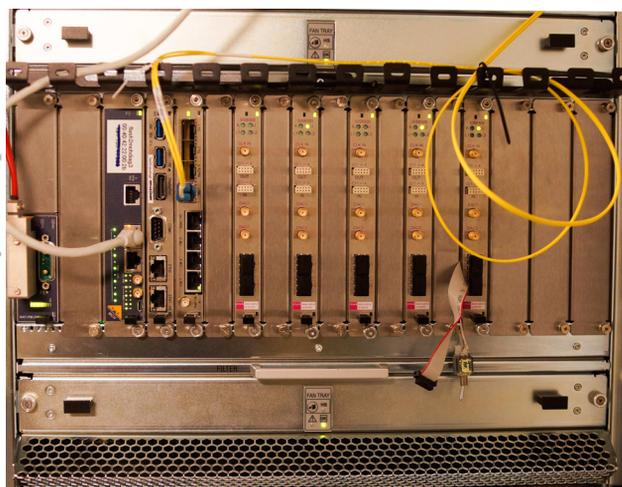


Figure 5: Front View of a MTCA crate carrying five LCBPMs at FLASH2.

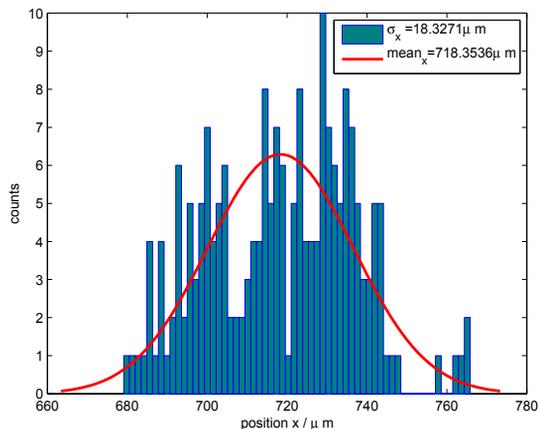


Figure 7: Position fluctuations in x direction for a strip-line BPM located in the FLASH2 EXTRACTION section.

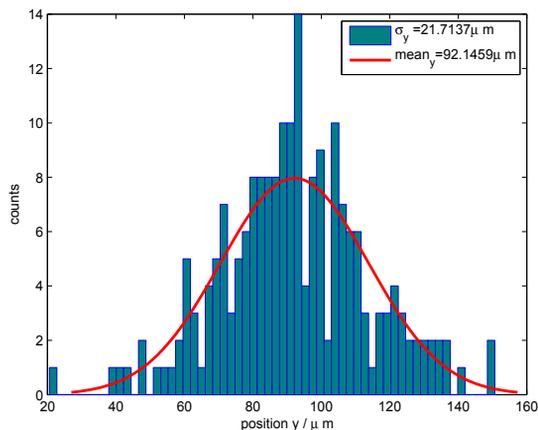


Figure 8: Position fluctuations in y direction for a strip-line BPM located in the FLASH2 EXTRACTION section.

### SUMMARY

A new type of MTCA.4 based Beam Position Monitor System for button and strip-line monitors has been designed, developed and successfully installed in FLASH2. The system has been a useful tool during first commissioning and SASE production of the machine [17] and ongoing machine commissioning [18]. It operates at charges down to 35 pC and lower and has a large headroom for operation at higher charges due to the high dynamic range given by the two step attenuators.

### OUTLOOK

The LCBPM system will be developed further to become more operator friendly for standard machine operation. This includes additional Firmware, device server and middle layer server upgrades. The performance will be analyzed as soon as data can be taken synchronously from all BPMs. In the future the system will replace the existing BPM system for the rest of FLASH which has been designed for a charge of

1 nC. Further increased BPM performance is expected by the implementation of the fully timing coupled mode. Additional pre-amplifiers will also enable LCBPM measurements in button BPM systems in the SASE section of FLASH2.

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