NSLS-II RF BEAM POSITION MONITOR-SYSTEM TEST AND INTEGRATION

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Abstract

The NSLS-II Synchrotron Light Source is a state of the art 3GeV electron storage ring currently in the process of commissioning at Brookhaven National Laboratory. The RF Beam Position Monitors (RF BPM) are one of the key diagnostics systems required for a successful and efficient commissioning. There are more than 250 RF BPM installed in the injector and storage ring. Each RF BPM was fully tested, first under laboratory environment, and then after installation utilizing a built in pilot tone signal source. These successful tests provided a solid base for the integrity of the RF BPM system, prior to the start of beam commissioning. This paper will describe tests performed and results of system integration.

INTRODUCTION

Beam stability is a key factor in meeting the specifications for intensity and brightness designed to be delivered by NSLS-II. The multi-bunch stored beam condition for vertical and horizontal resolution, as well as long term stability must be less than 200nm. The NSLS-II BPMs are installed in thermally stabilized racks which are regulated to +/- 0.1 degree C of operating rack temperature, which is essential to meet the stability requirement [1,2]. This paper will detail the implementation of various test procedures designed and performed on each BPM receiver (Fig. 1) pre and post installation.

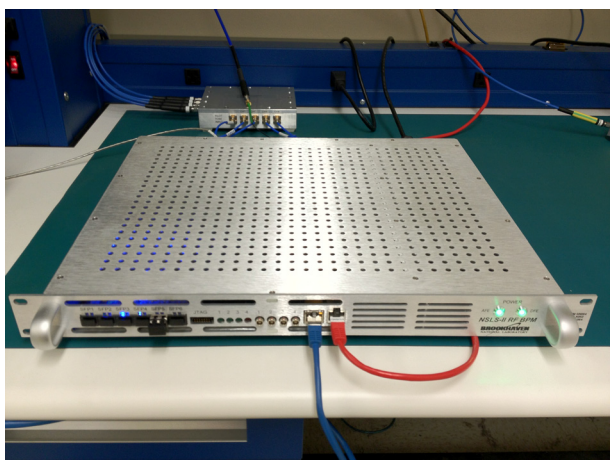

Figure 1: NSLS-II RF BPM production unit.

PILOT TONE COMBINER

An integral part of testing depends on implementation of the on board Pilot Tone Synthesizer, which generates a CW signal that is phase locked to the machine clock and is connected to the Pilot Tone Combiner module (PTCM) – shown in Fig. 2. This module is a custom design consisting of a passive RF board mounted in an aluminum enclosure and resides in the tunnel, near the BPM PUE and is connected via custom SIO2 Semi-Rigid Cables. The PTCM is characterized by comprehensive S-Parameter measurements, where S21 channel to channel variations are removed via automatic calibration routine, which maps the pilot tone to the received beam signal via measured S21[1,2].

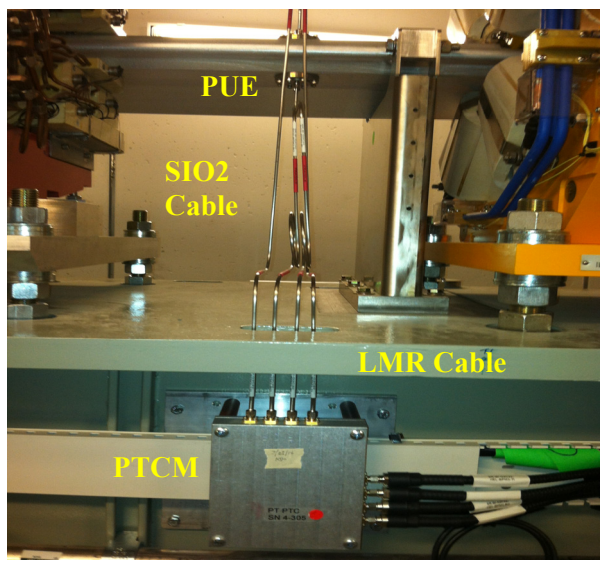

Figure 2: Pilot Tone Combiner Module (PTCM).

PRE/POST-INSTALLATION TESTING

Testing is conducted in a controlled laboratory environment using a custom test setup including VME based event/timing system, data acquisition, and post processing. MATLAB and Python based scripts have been developed to execute routines to test key functions and features of the BPM receiver. Performance tests procedures are first completed on each Analog Front End Board (AFE) using a dedicated receiver chassis populated with a Digital Front End Board (DFE). System testing is accomplished using custom routines developed to capture data for all three

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phases of functional tests, and utilizes the on board Pilot Tone Synthesizer as a CW source. The data is then organized, plotted and archived on per unit bases. Test results are stored in PDF, HTML, or screen shot images using MATLAB publishing feature. System integration tests are performed when BPM receivers are installed, and are run using EPICS to test network communications as well as IOC functionality and is presented using Control System Studio (CSS) as the user interface. High level applications are developed to run via Control System Studio (CSS) via a dedicated BPM IOC Server, with the added benefit of remote access to all of the BPM receivers installed in the accelerator [3]. These tools are used pre and post installation for lab based tests as well as integration tests and commissioning. Engineering panels for CSS have been developed to easily control parameters of each BPM in real-time. Figure 3 shows one of the CSS Engineering panel.

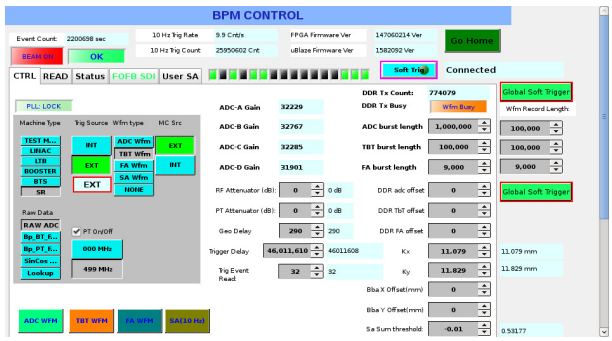

Figure 3: CSS Engineering panel for BPM control.

There are 3 phases of testing performed on each BPM receiver prior to installation. Each phase tests have several scripts performing various tests, as shown in Table 1.

PHASE 1 TEST

Communication interface and Firmware verification - This test is Python based and reports the IP address, MOXA port assignment, Mode, Firmware version, and PLL status – as shown in Fig. 4. Each RF BPM is parametrically configured for Single-Pass, Booster, and Storage Ring application. They are assigned a unique IP address and is mapped to a geographical location at NSLS-II. Upon power up, the BPM is examined to determine proper configuration mode. The ip address and MOXA port are manually configured. The firmware version , PLL status, ip, and port assignment is obtained by executing Phase 1 test script. Each BPM is automatically configured to one of three operational modes, as all three operational modes are derived from the storage ring revolution frequency.

Table 1: Stages of Testing and Routines

Description	Script	Output
Phase 1 Test	PYTHON	
Serial Communication	bpm_status.py	MOXA ip/port #
Network Communication	bpm_status.py	BPM Receiver ip
Firmware Version	bpm_status.py	FPGA/ublazer ver #
PLL/Machine Clk Present(378KHz)	bpm_status.py	PLL status T/F
Phase 2 Test	MATLAB	
117MHz Phase Noise(Jitter)	R&S FSUP	VCXO/PLL output
ADC Raw Data(117MHz Sample Rate)	test2.m	A-D, Sum Plot
Frequency Domain	test2.m	dbFs vs. Freq plot
Time Domain	test2.m	Samples vs. Counts plot
TBT Data(378KHz(SR), 1.89MHz(BR)	test2.m	A-D,X,Y Plot
FA Data (10KHz)	test2.m	A-D,X,Y Plot
SA Data (10Hz)	CSS	A-D,X,Y Plot
Phase 3 Test	MATLAB	
Cable Orientation Verification	test2.m	A-D FFT Plot
Static Gain Calibration	Static_gain_cal.m	
Intensity Dependence	Intensity_sweep_test.m	

Figure 4: Phase 1 test data (Communication/Firmware Verification).

PHASE 2 TEST

ADC_Raw Histogram Data, ADC_Raw Data in Time & Frequency Domain, TBT_Position, FA Position, and 117MHzPhase Noise (Jitter) plot – These tests are MATLAB based and are performed on each receiver both as a lab test, as well as a site test after installation, and compiles raw data to plot Time and frequency domain response of each ADC channel output, as well as 10KHz FA position data, and TBT position data. The test setup is fairly elaborate (shown in Fig. 5) and essentially a representation of operations configuration. The site test is performed when all BPMs are installed in the rack and cabled with production hardware.

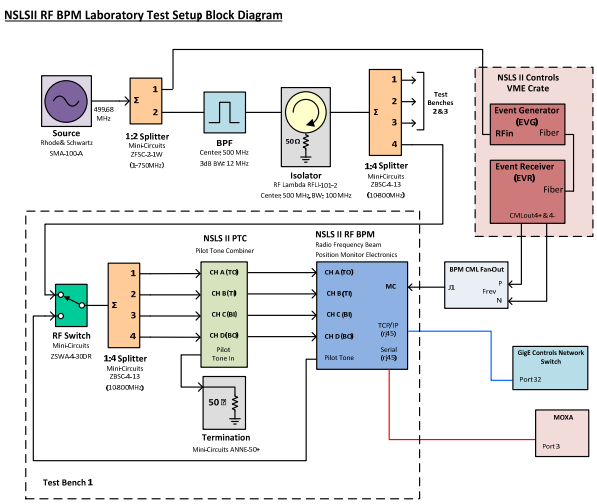

Figure 5: Phase 2 Test set up.

All test scripts are run local to racks via portable laptop computer. EPICS based applications via CSS engineering panels can also be used as a cross check during this phase of site testing, and is part of the integration testing requirement. A Noise jitter plot for the VCXO/PLL output is also produced using a Rhode & Schwarz FSUP Signal Source Analyzer. Figures 6-10 show the plots of data for phase 2 test.

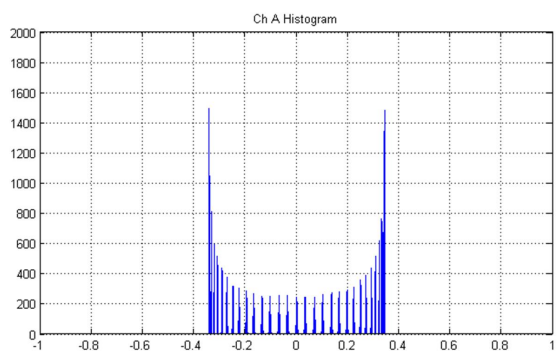

Figure 6: Phase2 data - channel A ADC raw histogram.

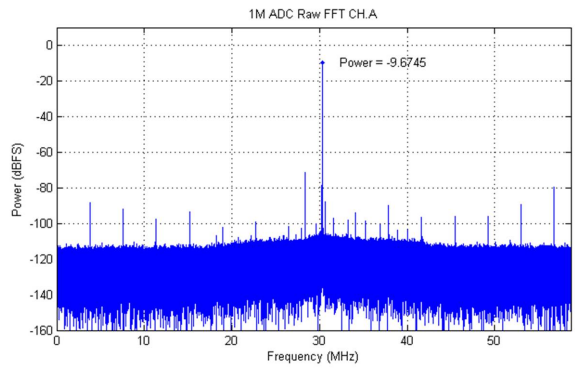

Figure 7: Phase data - channel A- ADC raw.

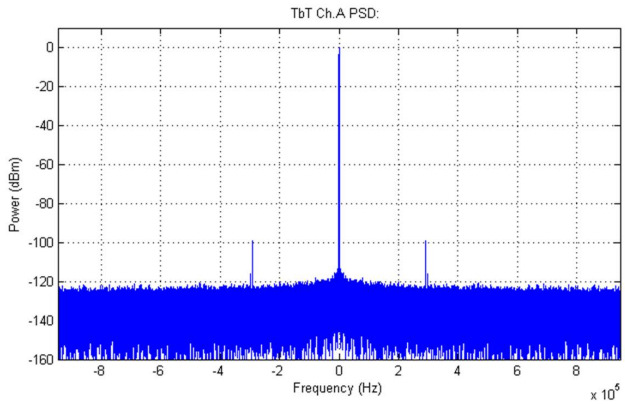

Figure 8: Phase 2 data - channel A - TBT Pwr dBm.

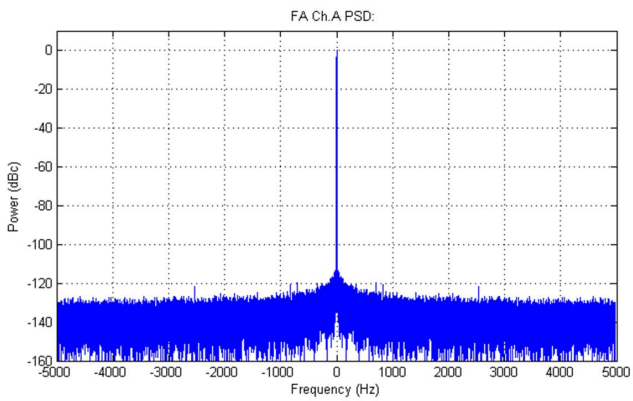

Figure 9: Phase 2 data - channel A FA Pwr.

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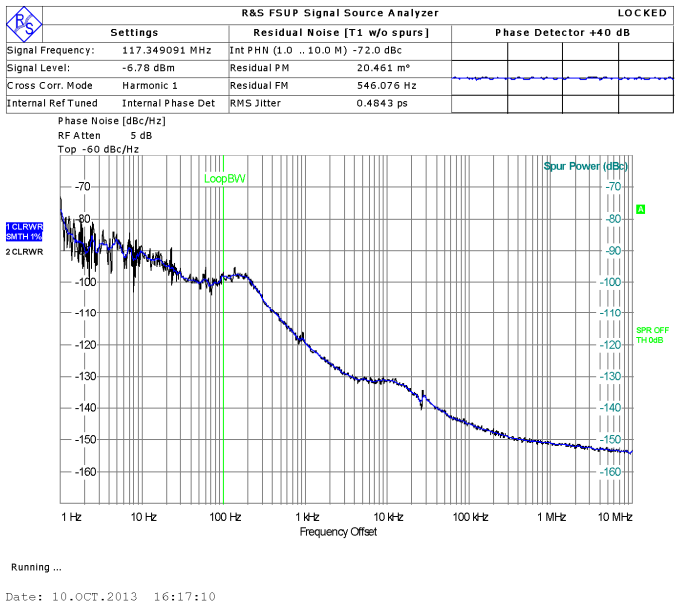

Figure 10: Phase 2 data -117MHz phase noise.

PHASE 3 TEST

Cable Orientation Verification (COV), Static Gain Calibration (SGC), and Intensity Dependence Test (IDT) - There are 3 separate MATLAB routines developed to perform these tests, and is part of site wide system integration. In addition the on-board Digital Step Attenuators are used for the SGC and IDT test respectively. The COV test is performed to certify all cable connections between the PUE and receiver, and is pilot tone based. The SGC test is performed to calculate the offsets due to channel-channel AFE amplifier gain differences. The IDT routine quantifies the performance of each channel as a function of position vs. signal power over the range of the Digital Step Attenuator in the Pilot Tone Synthesizer (0-31db), in 1db increments, and uses the PT as CW source. The hardware setup is identical for both SGC and IDT; and is shown in Fig. 11.

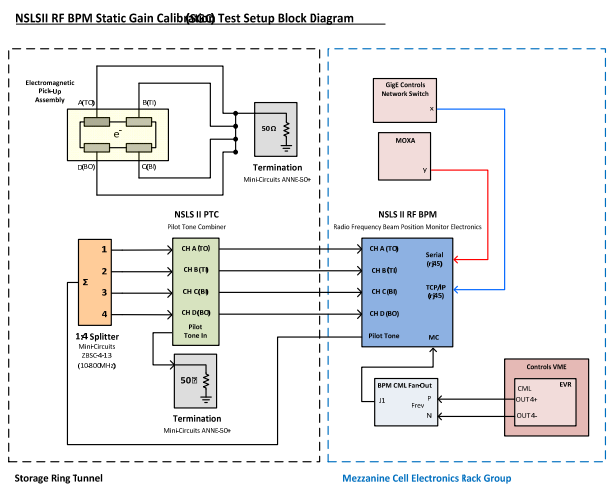

Figure 11: Phase 3 SGC/IDT test setup.

Cable Orientation Verification (COV)- A Process was implemented to address cable orientation verification. This helps insure that cables were connected correctly between PUE and receiver inputs. The NSLS-II BPM system consists of three distinct transmission line sets including phase matched, low loss SIO2 and LMR Coaxial cable, as well as phased matched custom patch cables in the rack. In addition, various adaptors are incorporated in these connections, and comprise over 6 thousand connections system wide. An elegant simple solution was developed using either an external CW source or the on board Pilot Tone Synthesizer and external attenuators installed as follows; Channel A(TO) = 0db, Channel B(TI) = -10db, C(BI) = -20db, D(BO) = -30db. The power level plots in Fig. 12, provided by MATLAB script illustrates 1:1 mapping of all channels in Frequency domain.

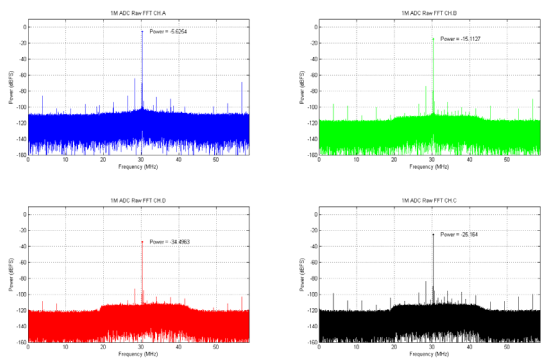

Figure 12: Phase 3 data - Pwr dBFs vs. freq.

Static Gain Calibration (SGC)- To address differences in the channel-channel AFE amplifier gain, which could result in significant offsets to the calculated position values, a MATLAB based test and calibration process was developed. The pilot tone drive through a calibrated 1:4 splitter is supplied at the tunnel PTC. The power is then measured at the receiver. The MATLAB routine selects one of the four channels as

unity. The difference between the remaining three and unity channel is calculated. This process is repeated in 1dB increments from 0db to 20dB using the available digitally controlled attenuators. A 21:5 element matrix is generated with weighting coefficients for each channel, across the gain set range and shown in Table 2 below.

Table 2: Static Gain Coefficient Matrix

	A	B	C	D
0	32597	31789	**32767**	31993
1	32553	31772	**32767**	31972
2	32569	31807	**32767**	31992
3	32531	31794	**32767**	31971
4	32551	31786	**32767**	31979
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.				
15	32304	31552	**32767**	31722
16	32117	31366	**32767**	31624
17	32094	31352	**32767**	31597
18	32120	31395	**32767**	31598
19	32097	31382	**32767**	31598
20	32124	31379	**32767**	31605

Figure 13 shows that position variation has been reduced to less than 1 micron after applying the SGC.

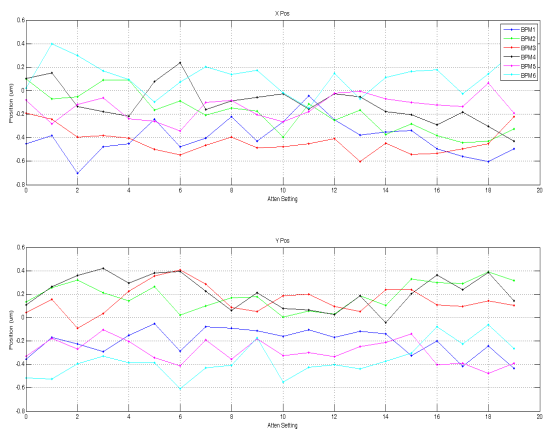

Figure 13: Position Vs attenu ator after applying static gain calibration.

Intensity Dependence Test (IDT)- Intensity dependence test is pilot tone based and is performed on each BPM site wide as a measure to test performance specification of 200 um stability in its linear range. It is the same hardware setup as the SGC test, and implements a custom MATLAB script. The on board Pilot Tone Synthesizer is used as a CW source and the Digital Step Attenuator is varied from (0-31db), in 1db increments. Figure 14 shows a typical intensity dependence and rms noise with power range of 40 dB.

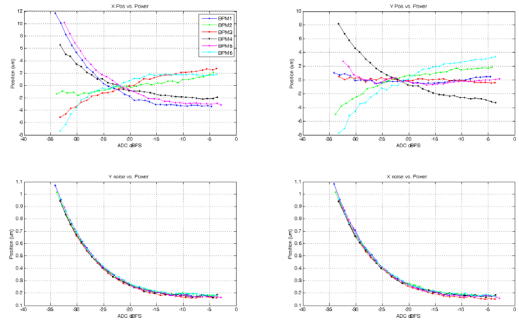

Figure 14: Phase 3 Intensity Dependence Data.

SUMMARY

Beam position Monitor system test and integration procedures including custom software routines and data capture, contributed to a methodology that provided effective and successful diagnostics for system level testing both pre and post installation in preparation for Storage ring commissioning. This streamlined efforts to meet system requirements as well as schedule for operations readiness. An exhaustive set of test procedures proved to produce a very high yield of working production units, as well as insuring system integrity site wide. This also provided a means to characterize and catalog performance of each BPM unit prior to installation. This data was also depended on as baseline measure for integration testing, as to ensure that design specifications were met.

REFERENCES

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