

DEVELOPMENT STATUS OF SINAP TIMING SYSTEM

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Abstract

After successful implementation of SINAP timing solution at Pohang Light Source in 2011, we started to upgrade SINAP timing system to version 2. The hardware of SINAP v2 timing system is based on Virtex-6 FPGA chip, and bidirectional event frame transfer is realized in a 2.5Gbps fiber-optic network. In event frame, data transfer functionality substitutes for distributed bus. The structure of timing system is also modified, where a new versatile EVO could be configured as EVG, FANOUT or EVR with optical outputs. Besides standard VME modules, we designed PLC-EVR as well, which is compatible with Yokogawa F3RP61 series. Based on brand new hardware architecture, the jitter performance of SINAP v2 timing system is improved remarkably.

INTRODUCTION

Timing information with high precision is required to synchronize distributed devices and equipments in large accelerator facilities. Based on event timing mechanism, SINAP timing solution provides trigger pulses with programmable polarity, width and delay. Edge aligned clocks with variable fractional factors are integrated in output function as well. [1]

We started to develop SINAP timing system since 2007. The prototype of SINAP timing system was completed and tested at LINAC of SSRF in January 2010. Pohang Light Source adopts the system in its upgrade project, and first beam accumulation was realized in August 2011. [2][3] Subsequently, we modified system design and improved performance in SINAP v2 timing system. The hardware development is completed so far. And we will implement the system for different project this year.

SYSTEM DESIGN

Thanks to rapid development of high-speed serial communication and FPGA technology, event timing system became the sophisticated solution for timing system in the large-scale accelerator facilities, especially for the 3rd generation light source. The main advantage of event timing system is that the required triggers and clocks could be transmitted in the uniform fiber-optic network. This means wherever the timing system fiber-optic network reaches, triggers and clocks could be provided. [4]

SINAP v1 Timing System

SINAP v1 timing system adopts classic star broadcast topology based on fiber-optic link of 2.5Gbps. Single event clock from 120MHz to 135MHz is supported. All of EVG (event generator), EVR (event receiver) and

FANOUT are standard 6U VME modules. All output triggers delay could be adjusted with coarse resolution of event clock period. Optical triggers from front panel of EVR could be additionally adjusted with fine delay resolution of 1/20 event clock period and 5ps. Interrupt function is integrated in EVG and EVR. The event logic and VME local bus is realized in Virtex-4 FPGA chip and CPLD respectively. [5] The system structure is illustrated in Fig. 1.

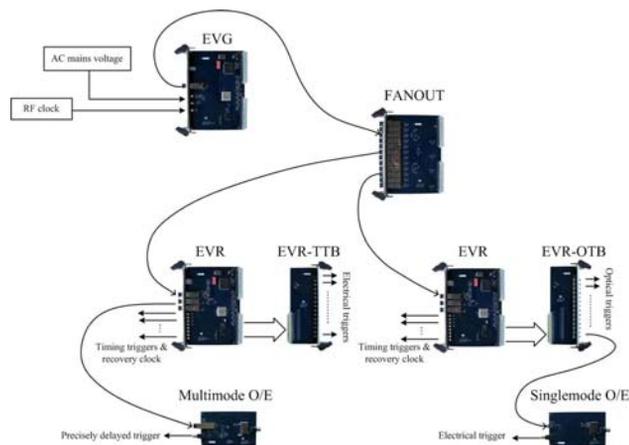


Figure 1: Structure of SINAP v1 timing system.

Software of the system is based on EPICS base 3.14.8.2 and vxWorks 5.5.1. During injection, the positions of all injection event codes stored in Sequence RAM of EVG are changed, but delay values of EVR output keep fixed. When transmission of all event codes is completed, an interrupt is generated in EVG, which makes a new list of event codes added to Sequence RAM. The whole mechanism is easy and efficiency. [6]

SINAP v2 Timing System

SINAP v2 timing system adopts similar topology based on fiber-optic network as well, but communication mode upgrades from simplex to duplex, which means that we could conduct deterministic data transfer and event distribution at the same time.

The frame format in the new version is illustrated in Fig. 2. One byte is for event code and the other byte is for data frame. Conventional distributed bus is abandoned, and all clocks are generated in EVR. Event clock from 60MHz to 135MHz is supported. EVG cascading function is supported. Two or more RF clocks are allowed to exist and synchronize output triggers in one single system consequently. Besides, all output triggers, no matter

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electrical or optical, could be delayed with multiple resolution, including event clock, 1/20 event clock and 5ps.

1 byte	1 byte
trigger	data frame
K28.5	data frame
K28.5	data frame
K28.5	data frame
trigger	data frame
K28.5	data frame
:	:

Figure2: Frame format in SINAP v2 timing system.

The system structure is illustrated in Fig. 3. Types of hardware modules are simplified. Only two types of core modules, VME-EVO (event optical board) and VME-EVE (event electrical board), could form one complete system. They are standard 6U VME boards, and both of event logic and VME local bus are realized in one Virtex-6 FPGA chip. VME-EVO board could be flexibly configured as EVG, FANOUT or EVR with optical outputs by software. VME-EVE could only be used as EVR with electrical outputs. Both of VME-EVO (configured as EVR) and VME-EVE support feature of multi-channel backplane transition board.

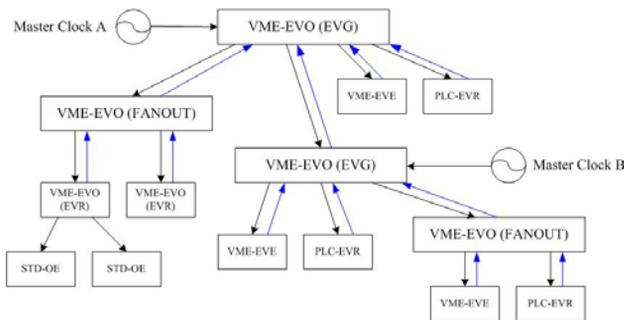


Figure 3: Structure of SINAP v2 timing system.

Additionally, the former one-channel Multimode Fiber OE module upgrades to four-channel STD-OE (stand-alone optical-to-electrical convertor), so as to achieve electrical isolation for critical equipments of high power. The module converts modulated optical triggers from VME-EVO (configured as EVR) to electrical triggers.

A new PLC-EVR was designed, which is compatible with Yokogawa F3RP61 series and suitable for low-cost applications. The module is one-slot width, and requires external 5V/3A DC power supply. Heat dissipation was specially considered to maintain the performance for long-term operation. We use an E²PROM chip to restore

essential information for configuration before normal operation. I/O register addressing mode is utilized in PLC software. Interrupt function is supported.

The four modules mentioned above are illustrated in Fig. 4.



Figure 4: Modules of SINAP v2 timing system.

Software in SINAP v2 timing system is similar to v1. Graphic interface is provided for basic operation and debugging with EDM.

TEST RESULTS

We made use of Tektronix TDS8000B oscilloscope and 80E03 Sampling Module to measure the short-term jitter between output trigger from EVR and RF reference clock. As shown in Fig. 5, the RMS jitter is about 10.1ps. By the way, the background short-term RMS jitter of the oscilloscope and sampling module is about 1.5ps.

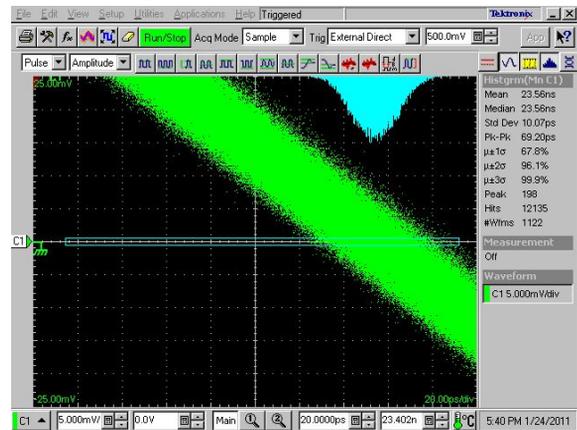


Figure 5: Jitter of SINAP v1 timing system.

For SINAP v2 timing system, we made use of the same test bench to measure the short-term jitter of output trigger from VME-EVE and RF reference clock. As

shown in Fig. 6, the RMS jitter is about 6.3ps. The jitter performance of PLC-EVR is similar to VME-EVE. We measured the long-term jitter for 20 hours as well, which is about 8.3ps and illustrated in Fig. 7.

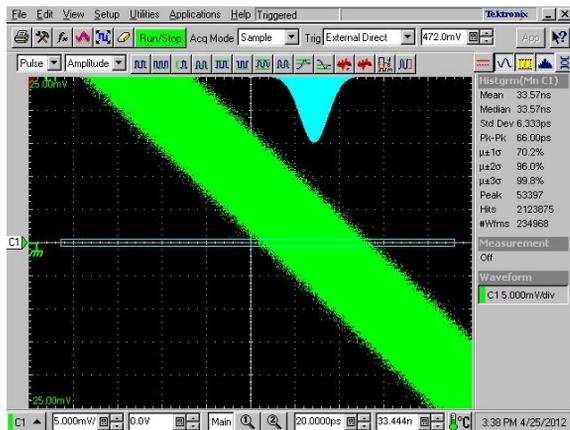


Figure 6: Jitter of SINAP v2 timing system.

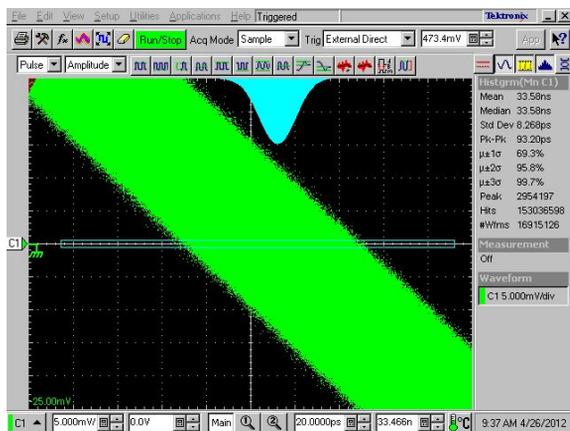


Figure 7: Jitter of SINAP v2 timing system with long-term drift.

CONCLUSION

As shown above, performance of SINAP v2 timing system is improved remarkably compared with v1 system. We designed a brand new firmware with Virtex-6 FPGA chip in the development of SINAP v2 timing system. Moreover, a lot of effort was done in dealing with ground bounce, which is often caused by high throughput of data in reading and writing VME bus.

After successful implementation at Pohang Light Source, SINAP timing system attracts the attention of many projects under construction or newly approved. SuperKEKB from Japan, ADS (Accelerator-Driven System) from China and CSNS (China Spallation Neutron Source) adopt the system as their timing solution. Shanghai Advanced Proton Therapy Project also considers the system as a competitive option.

With experience in research and design of SINAP timing system, we realized that it is barely possible to reach beyond magnitude of picoseconds for jitter performance in an electronics timing system. Therefore, we will focus on fiber-optic laser system to achieve lower jitter for accelerator facilities with higher requirement.

ACKNOWLEDGMENT

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