

Development of Gated Turn-by-Turn Position Monitor System for the Optics Measurement During Collision of SuperKEKB

Makoto Tobiya, Hitoshi Fukuma, Kenji Mori and Hitoshi Ishii,
KEK Accelerator Laboratory, 1-1 Oho, Tsukuba 305-0801, Japan

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Abstract

Gated turn-by-turn monitor system to measure optics functions using non-colliding bunch has been developed for SuperKEKB accelerators. With the fast, glitch canceling beam switch, beam position of the target bunch will be measured without affecting the fine COD measurement using narrow-band detectors. The gate timing and the bunch position detection are controlled by the Spartan-6 FPGA. The performance of the system, such as the gate timing jitter, data transfer speed from the system to EPICS IOC and the noise effect to the downstream narrow-band detector are reported.

Introduction

SuperKEKB Collider

40 times larger luminosity ($8 \times 10^{35}/\text{cm}^2/\text{s}$) by

- Reducing vertical beam size at IP
- Double beam currents
- [Nano-beam scheme]
- Low emittance (few nm mrad)
- Low X-Y coupling (less than 0.3%)
- Low vertical dispersion

Measure optics functions and correct
Betatron functions
X-Y couplings
Dispersion functions

Optics measurements

KEKB

- Excite one of steering magnets and measure COD response (Single kick method). Several steering magnets with different phase advance are used.

Betatron functions, X-Y couplings

- Shift RF frequency
- Dispersion functions

Low current (~30mA), single beam (without collision) multi bunched beam.

Not safe for large beam current nor colliding beam

Beam-beam tune shift
Strong bunch-by-bunch feedback

SuperKEKB

- Initial optics correction with similar methods used in KEKB (single kick, dispersion)
- New optics measurement using gated turn-by-turn beam position monitors (TbT).

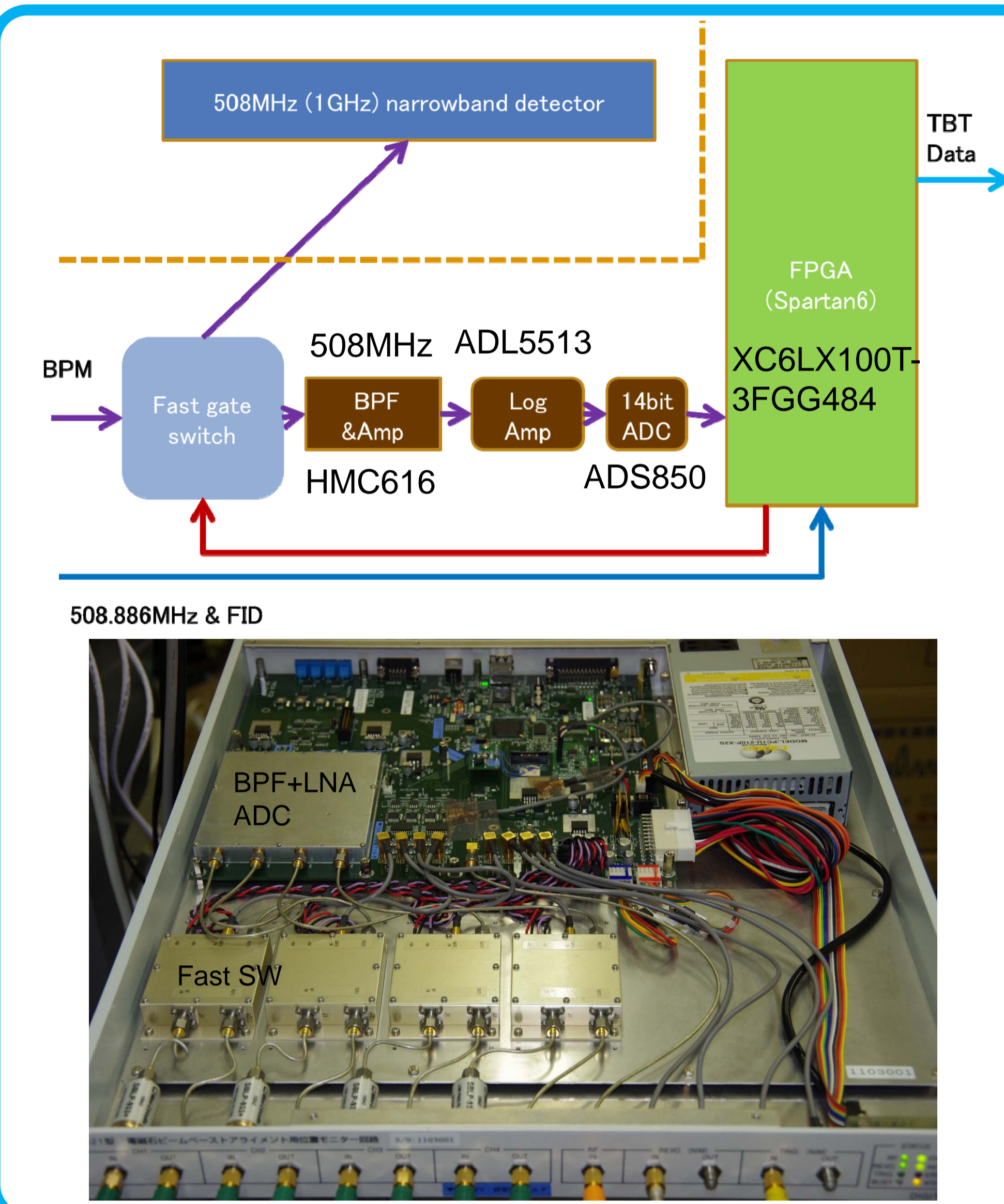
Optics measurement (and correction) with colliding huge beam current.

Main parameters of SuperKEKB rings

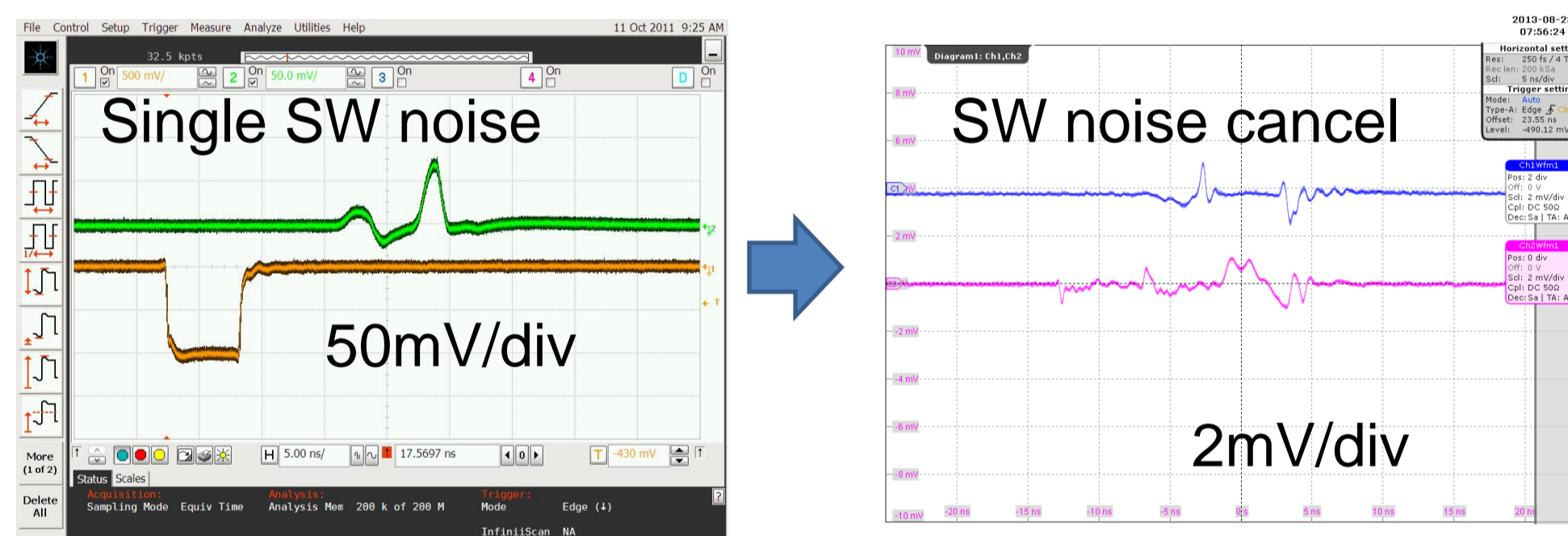
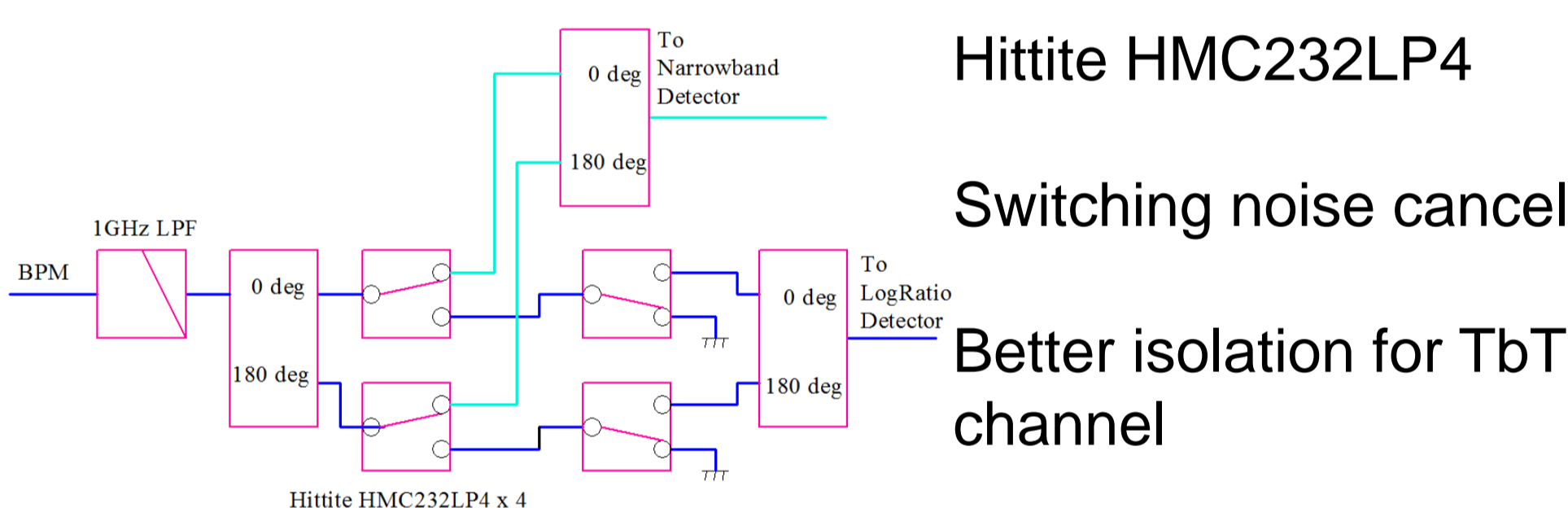
	HER	LER
Energy (GeV)	7	4
Circumference (m)	3016	
Max. beam current (A)	2.6	3.6
Number of bunches	2500	
Single bunch current (mA)	1.04	1.44
Bunch separation (ns)	4	
Bunch length (mm)	5	6
RF frequency (MHz)	508.887	
Harmonic number	5120	
Revolution frequency (kHz)	99.39	
β^* at IP H/V (mm)	25/0.30	32/0.27
Horizontal emittance (nm)	4.6	3.2
X-Y coupling (%)	0.28	0.27
Vertical beam size at IP (nm)	59	48
Rad. damping time T/L (ms)	58/29	43/22
Number of BPMs	446	444
Number of TbT monitors	135	135

Gated turn-by-turn BPM

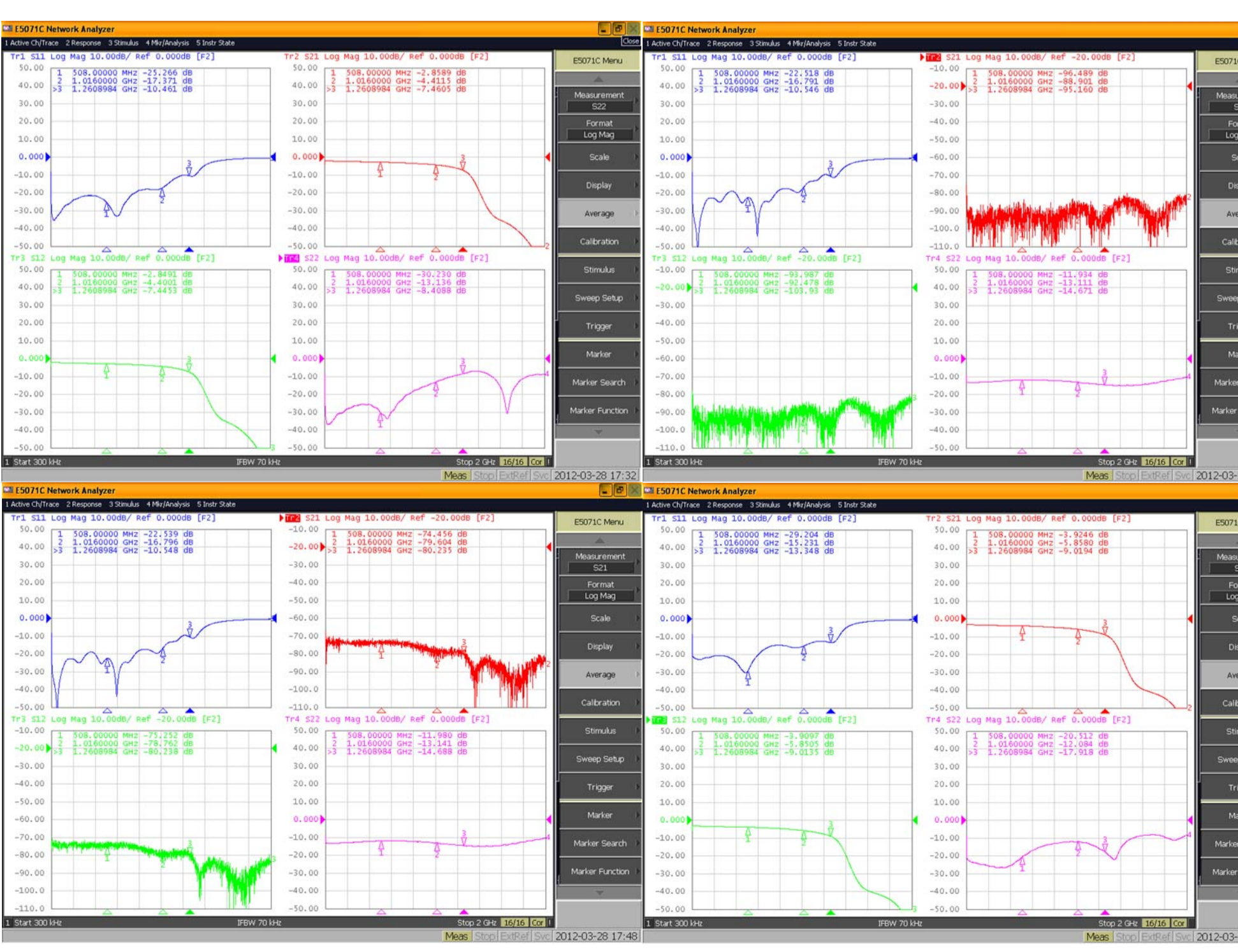
- Should not disturb the measurements of normal narrowband BPM. Switching noise should be suppressed.
- Rise and fall time of the gate should be short enough with the nominal bunch separation of 4ns.
- Enough isolation for turn-by-turn channel, much better than 70dB.
- Compact, all-in-one, (relatively) cheap system.



Fast Gate Switch



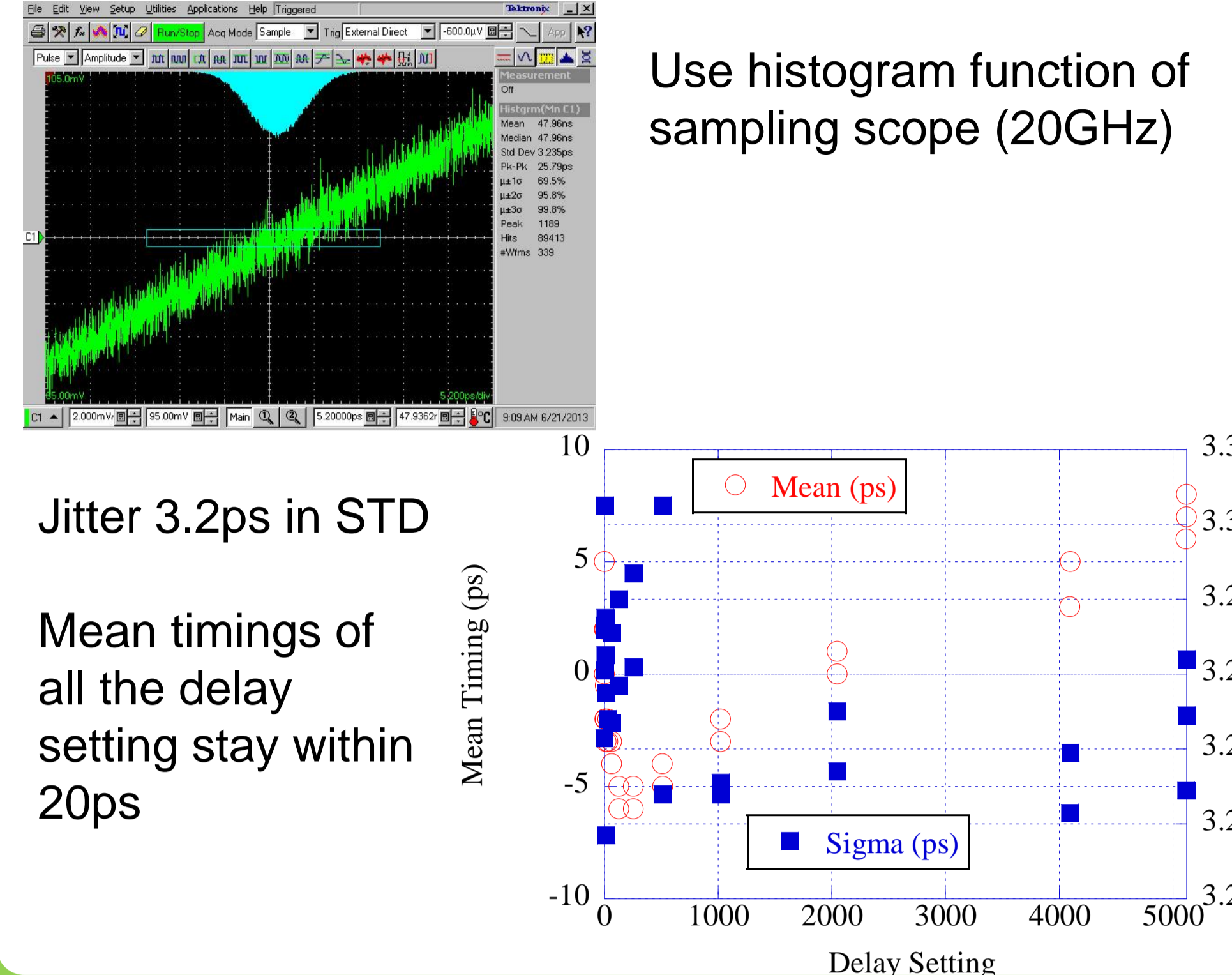
Excellent performance
Ultra-low SW noise
Fast rise/fall time (~0.6ns)
Good isolation (>80dB)



Gate timing

- Created in the Spartan6 FPGA
- External D-FFs are used to resynchronize timing
- EP195s for fine timing adjustment
- Gate width (a) 2ns-10ns, (b) inv of mode a (c) ON (d) OFF

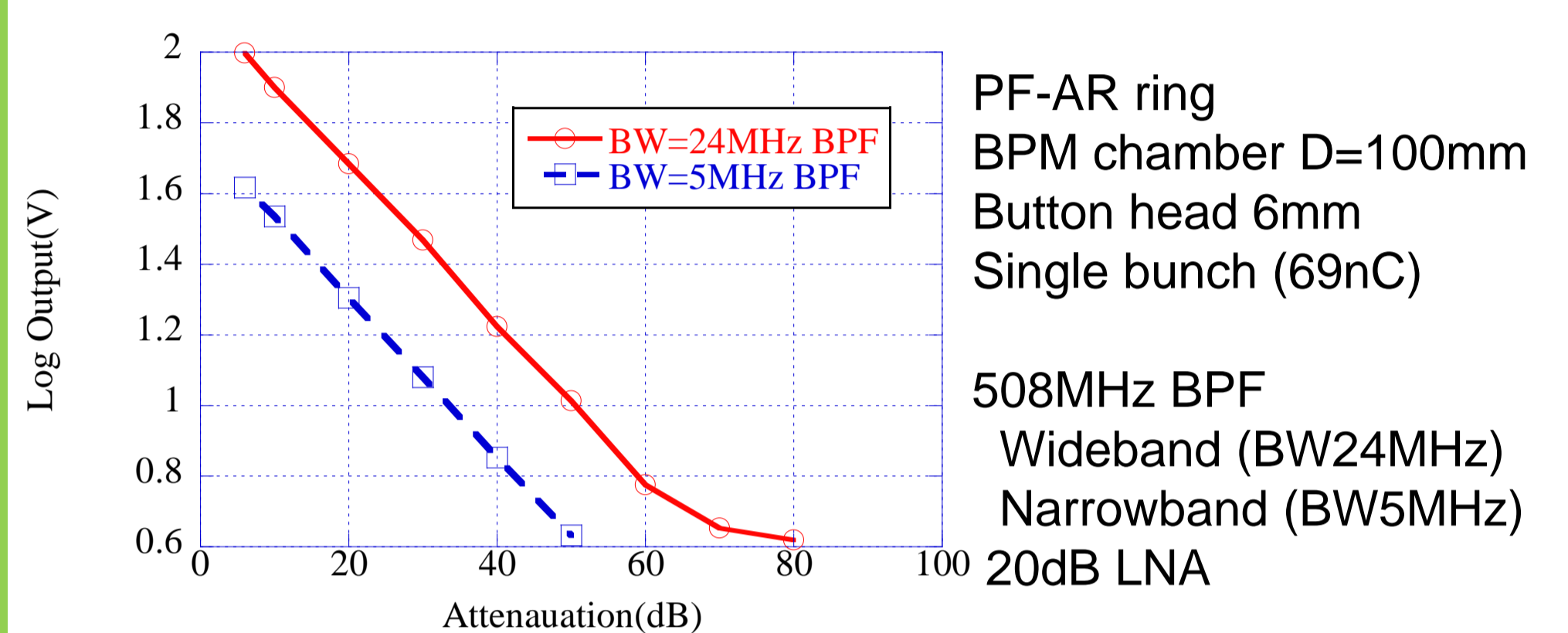
Gate timing jitter



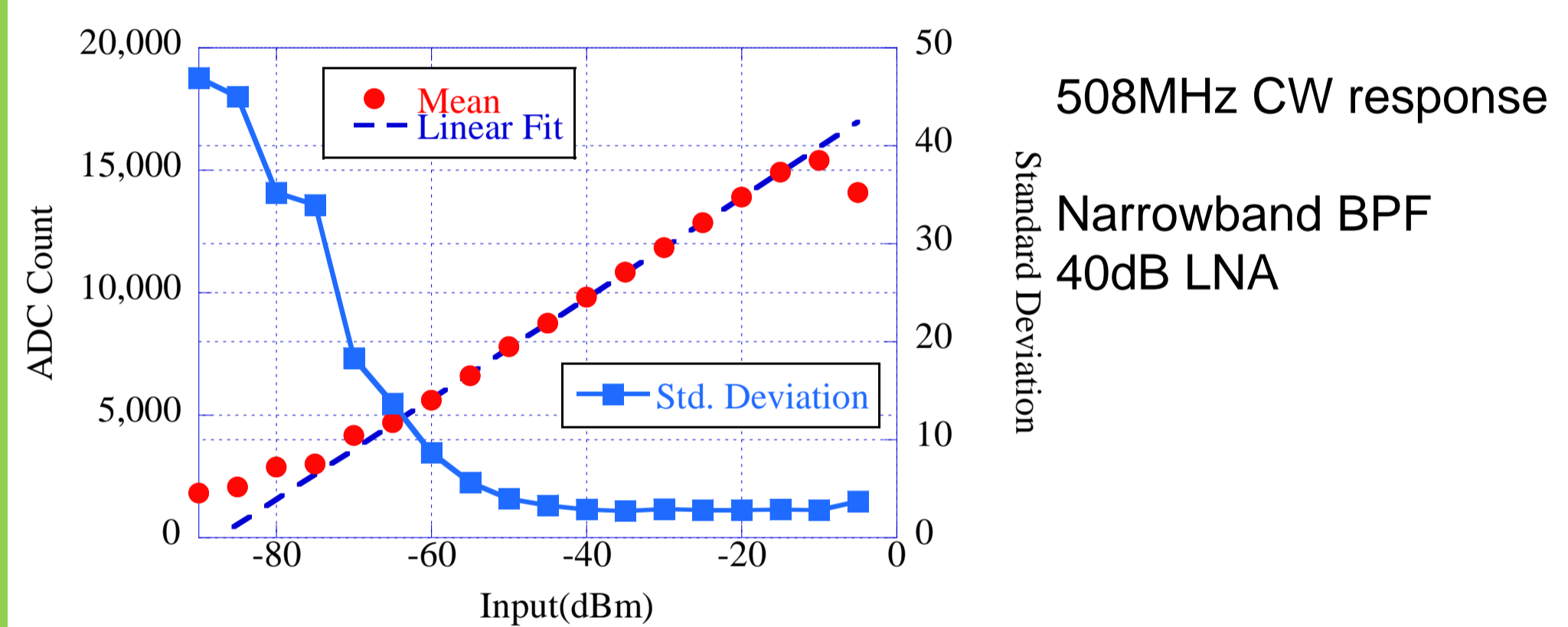
Jitter 3.2ps in STD

Mean timings of all the delay setting stay within 20ps

Linearity, Dynamic Range, position error



0.5nC injection bunch, $\phi 150$ chamber \rightarrow -43dB
Max charge $\phi 90$ chamber \rightarrow -8dB
Use narrowband BPF with limited VBW (<1MHz)



Standard deviation of ADC from -50dBm to -10dBm ~ corresponds roughly 30um of position jitter

Board control and data transfer

GbE (Gigabit Ethernet connection) by MicroBlaze
Status monitors (RF, Fid, temperatures, voltage)
RAW and calculated data on DDR3 SDRAM

EPICS R314.12.1 + ASYN4-21 + Seq
CentOS 6.4-x64 on Xeon E3-1220v2 (1U server)
(will handle 12-16 TbT systems for each local control substations)

Data transfer speed

Unexpectedly slow!
4-ch 0.5M turns of data (5s) - 44s!
<2M/s: Unacceptable!

Noise to narrowband detector

SW noise : negligibly small
Radiation (amplifiers, RF distributors etc.): much lower than most of the NIM modules.
However...
More RF shield, separate rack etc..

Future development (in progress)

SiTCP for much faster data transfer (~900M/s)
Automatic record parameters on EEPROM
Firmware update through Ethernet

Summary

- Designed and tested turn-by-turn BPM detector with fast gate switch
- SW noise has been successfully suppressed
- Timing control using FPGA
- Data transfer checked. Trying to speed up by SiTCP

The technology of fast gate switch with noise cancelling has been developed by Prof. T. Naito and Prof. T. Ieiri. We would like to express our sincere application to Prof. T. Obina for the support on the EPICS system and SiTCP system. We thank our colleague of SuperKEKB beam instrumentation for numerous support on the development.