DEVELOPMENT OF COMPACT ELECTRONICS DEDICATED TO BEAM POSITION MONITORS IN INJECTORS AND BOOSTERS

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Abstract

The need for state-of-the-art electronics for data-acquisition and the processing of BPM signals in Injector and/or Booster Synchrotrons is being addressed in a development that aims to make such systems available with less complexity while fulfilling precisely the needs of such specific BPMs.

The ESRF Booster Synchrotron uses 75 BPMs in its 300 m circumference to measure the orbit along its acceleration cycle of 50 milliseconds for the electron beam from 0.2 to 6 GeV. The 25-year-old electronics of these BPMs are in need of replacement.

While BPM electronics developments in recent years have focused on devices for Storage Rings that face extreme requirements such as sub-micron drift with time, beam intensity, etc. that result in complicated implementation schemes, this new development combines both simplification in the measurement concept and the implementation of new features such as compact design that integrates RF electronics with power-over-Ethernet supply and passive cooling, a powerful System-on-Chip engine and easy communication via SCPI commands. This paper will present the full design concept and its intended functionalities as a BPM device that should offer an excellent price/performance ratio.

MOTIVATION FOR DEVELOPMENT

The electronics for BPMs have in the past focused on storage rings and their requirements. The stability in the storage rings should be as good as it can be. The key component is therefore precise measurement of the beam position at fast rates. This is addressed by high resolution and high data-throughput instrumentation – typical sub-micron resolution @ 10 kHz data output.

For boosters, such performances are not needed; the complexity of design can therefore be reduced. The beam position measurement for boosters is in the tens of microns or even millimetre ranges.

Active feed-back control of the beam position in the booster is not required as the stabilization of the beam in terms of lateral coordinates is not crucial. On-demand information about the beam position is sufficient for the operator.

Based on this, development was initiated to optimize the functionality of the instrument to the booster application needs in terms of performance and including features such as digital-down-conversion (DDC) having the mean average filtering (MAF) functionality to optimize measurements at different fill patterns of the booster.

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The goal of the project is to provide an instrument that supports:

- micro-meter beam position resolution to cover the acceleration cycle
- beam position data available on demand
- no maintenance instrument
- rapid adaptation to a different machine

A detailed description of the ESRF's booster BPM pick-ups and setup is available in [1].

DESIGN CONCEPT

The idea of the design concept was to cover more than one booster application. This required a customizable platform that could be reconfigured to suit more needs – for instance, filters and amplifiers to customize gain and bandwidth. The balance between the more general and the optimized platform was taken into account, such as the possibility of implementing phased-locked-loop (PLL), if needed, the variable attenuation. An example of ESRF booster implementation is presented. Details of the ESRF's booster are available in [3].

The design is such that the position will be available to the user on demand. It will be calculated in the software from I and Q data processed in the field programmable gate array (FPGA) logic to make the FPGA design as simple as possible and thus enable the developers/users to further optimize or add complexity to booster implementation. The refreshing of data will be at trigger frequency, which can be max. 10 Hz. The position will be available per request of the user through a Standard Commands for Programmable Instrument (SCPI)-based interface.

The plan was for the BPM instrument to comprise the following functional blocks:

- hardware (HW)
- FPGA
- software (SW)

All three blocks are devoted to delivering position measurement information to the operator in the control system when he requests it. In the case of ESRF, it would have to be integrated into the TANGO control system.

Hardware

For the HW, several goals were set:

- ability to deliver RF signals @ 352 MHz to the analogue-to-digital converters (ADC) from the BPM button pick-ups
- No maintenance needed
- Low power consumption

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Processing capability on a single chip – System on Chip (SoC) supports achievement of the expected performances and has low power consumption. This FPGA technology will be addressed in the FPGA section.

No maintenance was achieved by removing the fans. This led to the decision to utilize passive cooling and, at the same time, to reduce power consumption to a minimum.

The ability to deliver RF signals to the ADCs is not so straightforward with the constraints mentioned. Careful attention should be paid to signal quality and power consumption when selecting the components. This limits the use of amplifiers and filters and necessitates the smart design of the RF input stages.

The RF analogue part has a wide bandwidth (from DC to ~500 MHz), but is expected to be limited by the use of Surface Acoustic Wave (SAW) filters to enhance the signal quality at selected bandwidth.

Sampling frequency is generated by a crystal oscillator (XO) and can be set from 80 MHz to 125 MHz. Selected

ADCs support such sampling frequency and output 14-bit data.

With low power consumption, Power-over-Ethernet (PoE standard IEEE802.3af) power supply utilization is feasible.

The basic block diagram is presented in Fig. 1. The white structures are external interfaces and the gray present the functional blocks.

The first development prototype boards are being tested. Signal quality is proved to be sufficient for providing micro-meter measurement resolution.

FPGA

SoC hosts both field programmable gate arrays (FPGA) and the Central Processing Unit (CPU) – the hard-core processor concept presented in [2]. With previous technologies, the CPU was usually outside the FPGA chip and communication between FPGA and CPU chips had to be handled. With SoC, data transfer is no longer a bottle-neck since the data is shared between the FPGA and CPU.

The SoC selected for this instrument is the Xilinx Zynq 7020.

The processing of the signals is designed as presented in Fig. 2.

There are three types of data stored in the buffers:

- ADC data
- I and Q data, which is the ADC data processed using the digital down-conversion (DDC) block [2] and stored to the TbT buffer
- further decimated I and Q data, which is TbT data decimated by 64 – see Fig. 2

Fig. 2 shows the FPGA part, which consists of:

- DDC
- ADC, TbT and TbT/64 buffers

The most direct data path is into the ADC buffer. From the 14-bit ADCs, the data is converted to 16-bit words and streamed to the ADC buffer – see Fig. 2. Sampling frequency defines the timespan covered by data when the buffer is full – see Table 1 for details. For the ESRF case, the sampling frequency is approx. 108 MHz.

The data comes from the DDC into the TbT and TbT-decimated (shown in Fig. 2 as TbT/64) buffers. Its function is digital-down-conversion by utilising the Cascaded Integrated Comb (CIC) and Finite Impulse Response (FIR) filters [2]. The filters' parameters are optimized on the basis of the booster's physical dimensions and the RF at which they operate. I and Q data is outputted from the DDC block.

I and Q data is then stored in the TbT buffer with a decimation factor compared to the ADC buffer. In the TbT/64 buffer, an additional 64 decimation factor to the TbT data is applied before storage.

The partitioning of the buffer sizes is presented in Table 1.

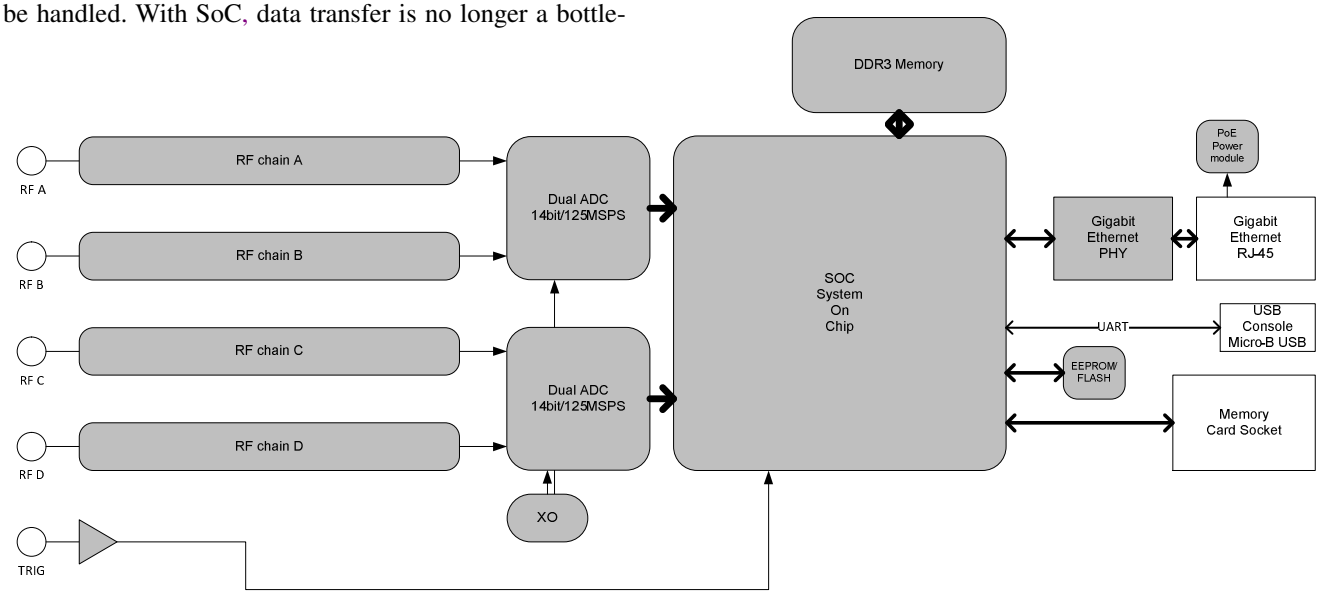

Figure 1: Basic HW design.

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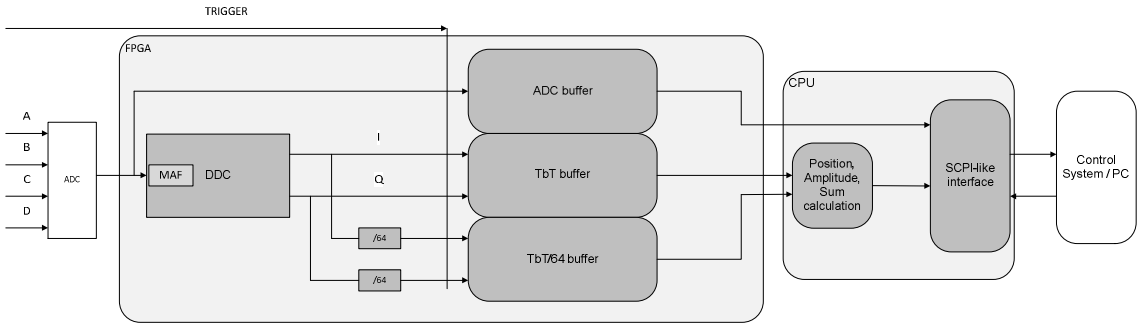

Figure 2: Functionality in the SoC.

Table 1: Memory Partitioning

Buffer	Capacity [kAtoms]	Capacity [MB]	Timespan† [ms]
ADC	1024	8	10
TbT	256	4	262
TbT/64	256	4	16777

Software

The software provides:

- further elaboration of the signals by the calculation of the position, sum and amplitudes from data in both TbT and TbT/64 buffers
- SCPI-like interface

SCPI-like commands enable the user to access the signals and to set parameter values or check parameter setting. For each signal, the instrument will provide data in two formats:

- ASCII as human-readable format
- binary for reducing the data transfer load over the network when the instruments are integrated into the control system

The booting of SW is supported in two ways, from:

- a configurable server with TFTP, or
- a memory card, if inserted

As a consequence of this booting implementation, upgrading of the SW is possible from a single location.

The CPU uses the standard delta over sum equations to calculate position.

CONCLUSION

The development of the instrument is under way, with the first prototypes being produced – see Fig. 3. The first results of the measurements of the HW part are under way using the already-implemented SCPI daemon and FPGA. They are still in development, but have enabled measurements on ADC data.

The **initial** results of the measurements on **development prototypes** in the lab are within expectations:

- crosstalk between channels: typically better than -60 dB
- unit boot options and ADC data buffer functionalities were evaluated and confirmed
- PoE functionality within the specifications of the IEEE802.3af standard.

Confirmation of the design and its implementation is expected to be done on the development prototype at the end of October 2013 at ESRF.

The idea is to put the instrument close to the BPM pick-ups (as the power is delivered over the Ethernet cable), thus avoiding long RF cabling, using proper radiation shielding.

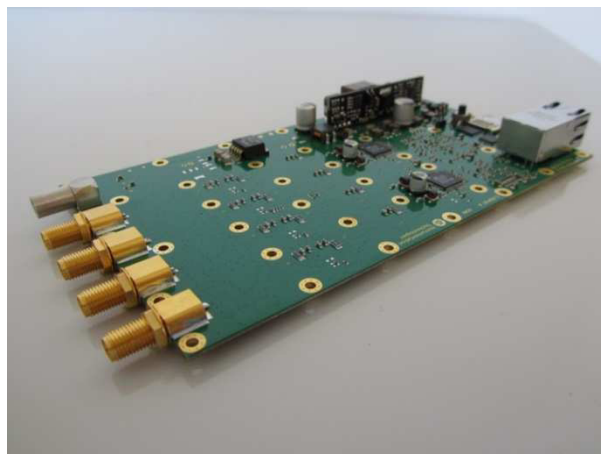

Figure 3: Prototype board.

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[3] http://www.esrf.eu/Accelerators/Accelerators/Booster, Online: August 2013.

†For the ESRF: RF @ 352 MHz, sampling frequency 108 MHz, decimation factor 108, 16-bit data

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