THE DESIGN OF BPM ELECTRONICS FOR CSNS RCS

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Abstract

This article introduces the design and implementation of the BPM electronics for CSNS RCS. The challenge of designing the BPM electronics is to acquire and process the signal with large dynamic range (5.8mv~32V) and changing width (80ns to 500ns). The analog circuit described in this paper, which is constructed of single-stage amplifier and analog switch, can cover the input signal with large dynamic range. Because of the minimum bunch length (80ns) and the requirement of position resolution, a 14 bit 250MHz ADC is adopted to digitalize the signal. Besides, the algorithm developed in FPGA is able to make Bunch-by-Bunch position calculation and Closed Orbit position calculation in real time. In addition, some preliminary test results will be presented and discussed, which show that the resolution of Bunch-by-Bunch position is 0.8mm when the input signal is 10mV and the resolution of Closed Orbit position is 50 μ m.

INTRODUCTION

Beam Position Monitor (BPM) is indispensable for accelerator of stable running. In the future China Spallation Neutron Source (CSNS), 32 BPMs will be installed on the Rapid Cycling Synchrotron (RCS). A complete BPM consist of Pick-Up and electronics. The Pick-Up is mounted on the beam pipe. When the proton bunch passes by, the Pick-Up generates current signal which is relevant to the bunch density. Using the Pick-Up signal, BPM electronics calculate the position deviation of the bunch.

CSNS RCS BPM PICK-UP SIGNAL

Equivalent Circuit of Pick-Up

CSNS RCS BPM adopts the linear-cut pick-up electrode. The capacitor C between the electrode and the beam pipe is 366pF, and the pick-up signal is transmitted to the electronics through a 50m cable. The input impedance of electrodes is 50Ω, and the equivalent circuit is shown in Figure 1 [1].

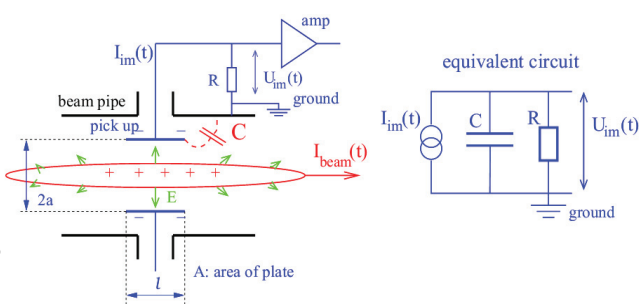

Figure 1: Scheme of a pick-up electrode and its equivalent circuit.

Dynamic Range of Pick-up Signal

In a beam cycle, the beam bunch in the RCS run about 20,000 circles, which can be divided into three stages: injection, acceleration, extraction [2]. After the first bunch is injected, it is painted in the next 250 circles. In the duration, the beam bunch has a rectangular shape. After that, the bunch is accelerated and compressed, with the length of bunch varying from 500ns to 80ns. In the end, the beam bunch is extracted after about 20,000 circles. In this time, the beam bunch has a shape of cosine-square, and the beam current is in maximum. Different beam bunch shapes generate different pick-up signals, and the pick-up signals in injection and in extraction stage are showed in Fig. 2.

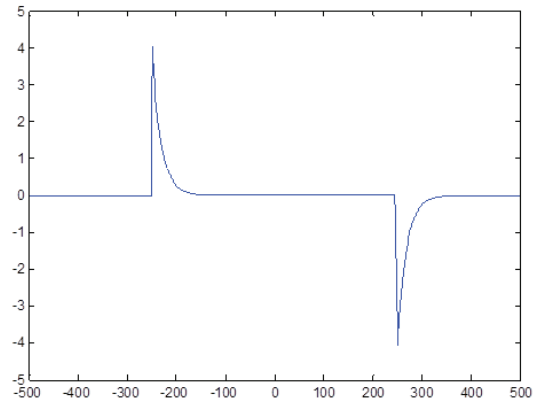

Figure 2-1: Pick-up signal in injection.

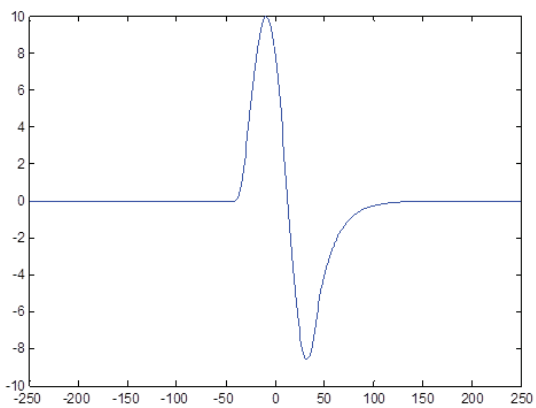

Figure 2-2: Pick-up signal in extraction.

In calculation and simulation, the electrode signal has a dynamic range of 9.4mV to 14.2V. This is the theoretical result on the condition that the load of the electrode is 50 Ω. For reliability considerations, this BPM system

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requires the electronics has ability to receive and process the signal with dynamic range of 5.8mV~32V.

Features of Pick-Up Signal

In addition to the dynamic range of the pick-up signal, there are some other features of the signal that affect the design of electronics. We make a summation of the parameters of the signal as follow:

Dynamic range:	5.8mV~32V(75dB)
Length of signal:	80ns~500ns
Analog bandwidth:	30MHz
Revolution frequency:	1MHz~2.4MHz

DESIGN OF ELECTRONICS

A BPM system include 4 pick-ups (A,B,C,D), placed symmetrically around the beam pipe, as the Figure 3 shows. For a pair of electrodes placed symmetrically, it has the relationship as below [3]:

$$X = \frac{1}{k} \cdot R \frac{V_l - V_r}{V_l + V_r} \qquad (1)$$

Vl Left electrode signal
Vr Right electrode signal
K Parameters, here is 0.84
X Displacement of the beam bunch from center
R The radius of the beam pipe

The aim of the BPM electronics is to receive and process the BPM electrode signal, and to calculate the displacement of the beam bunch from centre in real-time.

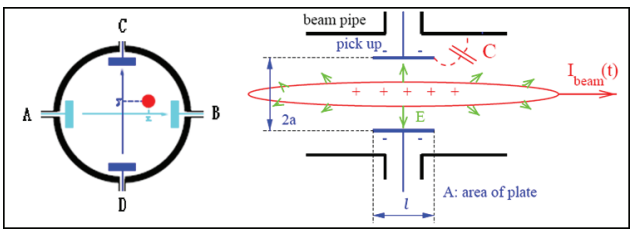

Figure 3: Scheme of a set of electrode.

Architecture of Electronics

Considering the advantages and disadvantages of all BPM signal processing methods, the CSNS RCS BPM system adopt the digital Δ/Σ method to process the pick-up signal [1]. The architecture of the electronics is showed in Figure 4. The four pick-up plate signal is processed and digitalized individually, and the digital signal is transmitted to FPGA. In FPGA, bunch-by-bunch position and closed orbit position information is calculated based on formula (1). The bunch-by-bunch position information is sent to DDR2 for storage and the closed orbit position information is sent out through the VME bus. Besides, the electronics use a CPLD and a Flash to implement online configuration. In addition, there is one connector for receiving external trigger, one connector for external clock, and two connectors for output of beam bunch information.

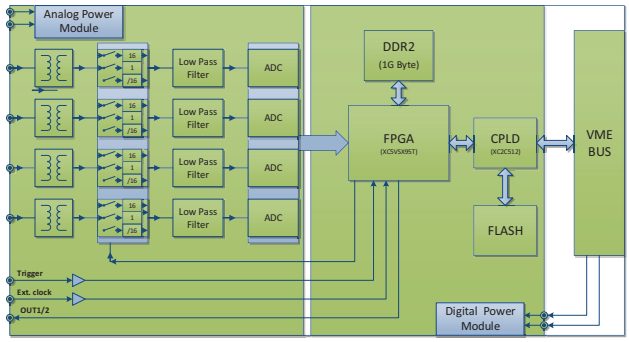

Figure 4: Architecture of BPM electronics of CSNS RCS.

The Design of Analog Circuit

The BPM electronics use the variable gain amplifier (VGA) implemented by amplifier and analog switch to receive and process the pick-up signal. The gain setting is showed in Table 1. This design set 3 gains: *16, *1, 1/16; and the three gains cover the electrode signal with large dynamic range.

Table 1: Gain Setting of VGA Circuit

Gain	Cover range	Process range	LSB
*16	0—125mV	0—125mV	0.0076mV
*1	0—2.0V	125mV—2.0V	0.122mV
1/16	0—32V	2.0V—32V	1.953mV

According to the gain setting, we propose a structure of analog circuit as Figure 5. The circuit consists of three stage amplifier. Because the maximum output voltage swing of the selected amplifier is +/-18V, the first stage amplifier has a gain of 0.5 to receive the pick-up signal with all amplitude. The second stage amplifier, combined with analog switch, configure gain 16, 1 and 1/16. The third stage amplifier converts the single-ended signal to differential signal to provide to ADC. In addition, a low pass filter (LPF) is placed between the second stage and the third stage amplifier, with a 3dB bandwidth of 30MHz. The LPF is used to enhance the signal noise Ratio.

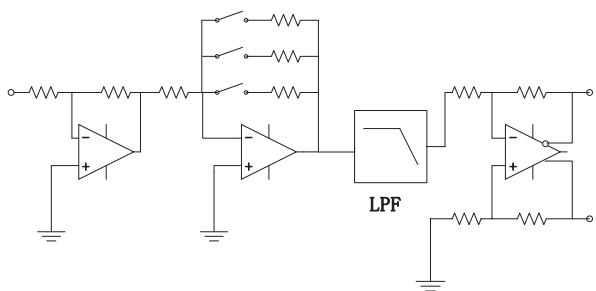

Figure 5: Scheme of analog circuit.

For the second stage amplifier, it is challengeable using single stage amplifier to implement VGA with gain

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changing from 16 to 1/16. We propose a structure of the second stage amplifier, as is showed in Figure 6. In this structure, the resistors have a relationship: R1=R4，R2=R3，R2=7.5*R1. When switch S1 is ON, and S2, S3 are OFF, the gain of the circuit is 16. When only switch S2 is ON, the gain of the circuit is 1. When only switch S3 is ON, the gain is 1/16. Because one side of the switches is connected to inverting input of the amplifier, the "Off Isolation" parameter is not important in this structure. So, this circuit can transport signal with bandwidth as high as 30MHz.

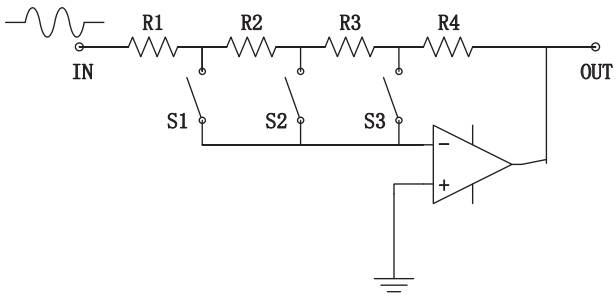

Figure 6: Structure of the second stage amplifier.

SIGNAL PROCESSING

The minimum length of the beam bunch is 80ns, hence half of the bipolar signal is 40ns. Besides, on the behalf of resolution of the electronic system, a 250MHz 14bit ADC is determined. The signal from the 4 pick-ups of a BPM system is digitalized individually, and the digital signal is transported to FPGA. According to equation (1), we develop the firmware that can calculate the position information in real time.

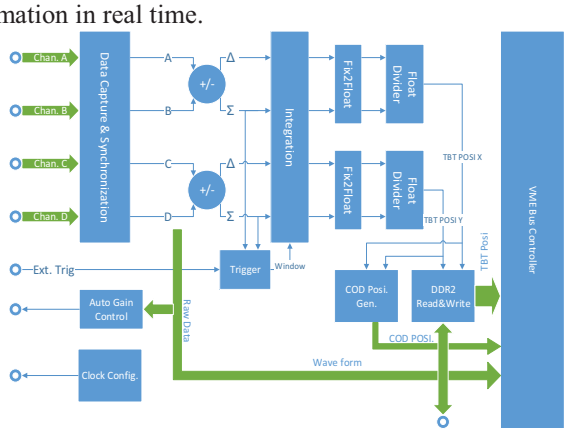

Figure 7: The architecture of the firmware.

The architecture of the firmware is showed in Figure 7. Firstly, the digital signal from the four ADCs is aligned to each other. Then, the Δ, Σ value is computed. When the beam signal come, the firmware triggers by the coincidence of self-trigger and external trigger. After that, the firmware generates a trigger window. In the window, Δ, Σ value is integrated. In the end, the integrated Δ, Σ value is substituted into the equation (1) to calculate the bunch-by-bunch position. Closed orbit position is calculated by averaging the bunch-by-bunch position [1]. The bunch-by-bunch position is transmitted to DDR2 for storage, and the closed orbit position is sent out through VME bus.

In addition to this, the firmware has the function of waveform recording. Under this function, the waveform of the 4 channel can be recorded and partially sent out through VME bus. Moreover, the firmware has a module of Auto Gain Control, which can change the gain setting of the analog circuit according to the amplitude of the pick-up signal.

TEST

Bunch-by-Bunch Resolution

Test method: channel A and channel B are provided with pick-up signals with the same amplitude and the same phase, and the amplitude varies from 10mV to 4.5V. We tested the bunch-by-bunch resolution in each amplitude point, and depicted the result in Figure 8. The result shows that the resolution is 0.9mm in the minimum amplitude of 10mV.

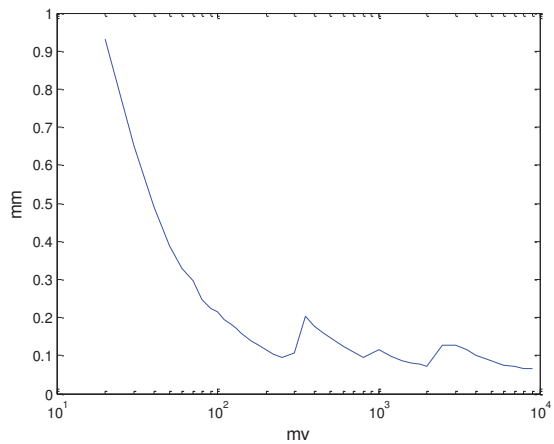

Figure 8: Bunch-by-bunch resolution when beam in the centre of beam pipe.

Closed Orbit Position Resolution

Test method: channel A and channel B are provided with pick-up signals with the same amplitude and the same phase, and the amplitude varies from 10mV to 4.5V. We tested the closed orbit resolution in each amplitude point, and depicted the result in Figure 9. The result shows that the closed orbit resolution is 45 μm in the minimum amplitude of 10mV.

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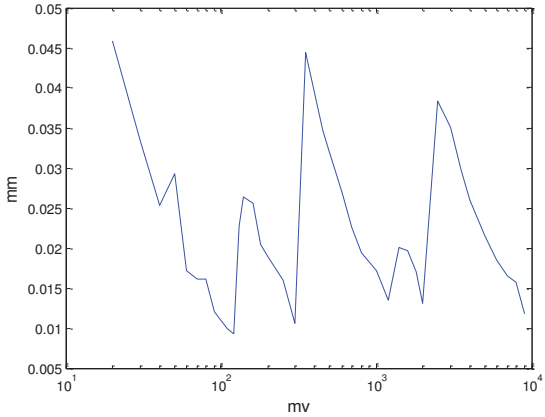

Figure 9: Closed orbit position resolution.

CONCLUSION

This article introduces the design of CSNS RCS BPM electronics which is implemented by digital Δ/Σ method. To achieve low noise and high resolution of BPM electronics, the article propose a VGA circuit, which consists of single stage amplifier and analog switch, to process the pick-up signal with dynamic range of 75dB. The primary test show that bunch-by-bunch resolution is 0.9mm for minimum signal of 10mV and the Closed Orbit resolution is 50 μm.

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