REFERENCE SIGNAL GENERATION WITH DIRECT DIGITAL SYNTHESIS FOR FAIR

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Abstract

In this paper, a method for the generation of RF reference signals for synchrotrons and storage rings will be presented. With these reference signals, the RF cavities in the Facility for Antiproton and Ion Research (FAIR) shall be synchronised. Digital frequency generators that work according to the DDS (direct digital synthesis) principle will be used as reference generators.

Via an optical network with star topology, these reference generators will be fed with two clock signals that show a certain correlation of frequency and phase. Due to delay measurements, their phases at different end points of the optical network are known. From these clock signals, reference signals with specific frequencies can be derived. The phases of these reference signals can be fine-tuned against the phases of the clock signals, allowing the phases of different reference signals to be synchronised.

With the commercially available DDS generators used in the prototype, phase steps of 0.022° are possible. At a reference signal frequency of 50 MHz, this corresponds to 1.22 ps.

The presentation describes the functionality of this method for reference signal generation and shows under which conditions the step size of the phase adjustment can be improved further.

INTRODUCTION

The method presented here for generating reference signals may be used in the future timing system for FAIR [1] (BuTiS – Bunch Phase Timing System [2]) as an alternative to other local reference synthesizers. Some aspects of this system, like the structure of the optical network and its noise characteristics, were already described in [3-4]. This article provides a more detailed description of the novel method for reference signal generation. To convey an appreciation for the system function of the reference generators used for this purpose, the basic principle of cavity synchronisation in FAIR is once again explained by way of introduction [3-5].

Cavity Synchronisation in FAIR

The objective is to synchronise the electrical fields of the cavities in the future FAIR (Fig. 1) [6] whose target frequencies (0.4 to 5.4 MHz) and target phase are defined by nearby signal generators (Fig. 2). The signal generators are frequency generators also that work according to the DDS (direct digital synthesis) principle.

To enable synchronous operation of the signal generators, these must be fed phase-synchronous reference clock signals. Reference Signal 1 (50 MHz) is used by the signal generator for digital signal synthesis, and Reference Signal 2 (97.7 kHz) is used to enable frequency and phase shift commands to be carried out synchronously. In combination with data telegrams that are sent in the time window of Reference Signal 2, commands may be executed at an arbitrary slope of Reference Signal 1. Therefore, both reference signals together represent the reference time. The reference signals must have the same phase independent of the location where they are needed. In the concept presented here, the reference signals are generated by a DDS unit. This DDS unit requires a clock frequency at least two times higher than the output frequency. Therefore, the global clock signal of 200 MHz is defined by BuTiS [2]. As a conclusion, two system clocks (200 MHz and 97.7 kHz) are transmitted from a central point to the reference generators in order to generate the reference signals[†]. Due to the star distribution of these system clocks to different locations, they will be frequency-synchronous with one another but exhibit a phase displacement $\Delta\varphi$ that depends on the respective delay of the system clocks τ_n. To determine phase displacement, the delays are measured. With the help of this information, phase corrections are effected in the reference generators and in this way the phases of the reference signals φ_{Ref} are synchronised. Since the delays are time-variable due to environmental influences, they must be measured on a permanent basis.

The purpose of the system is to produce phase-synchronous and phase-stable reference signals at 13 spatially separate points of the facility.

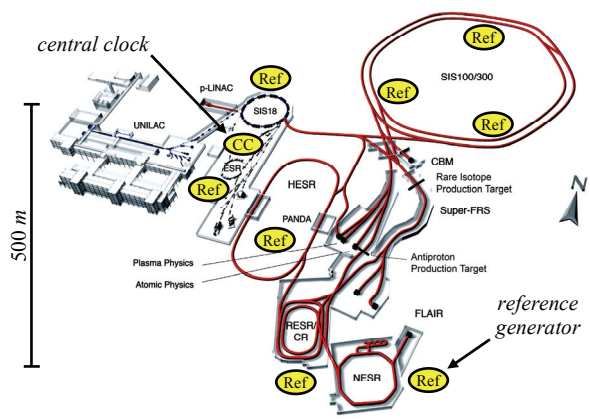

Figure 1: Facility for Antiproton and Ion Research.

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[†] The system will be modified in future in such a way that the frequency 97.7 kHz for Reference Signal 1 and clock signal 1 is replaced by a frequency of 100 kHz.

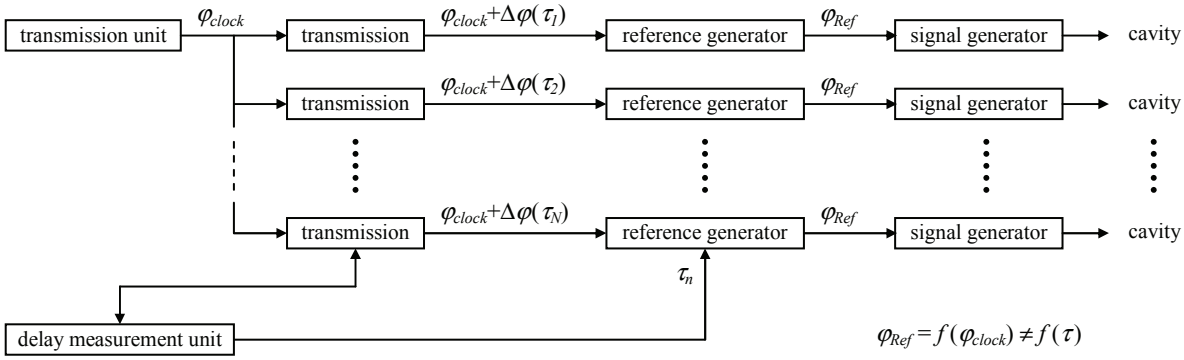

Figure 2: Basic principle of the cavity synchronisation.

State of Technology

In other systems, various techniques are used to shift the phase of the signal to be transmitted in such a way that the phase stabilises at the end of the transmission line. For phase shifting, the following are used: optical delays [7], optical phase shifters [8], fibre stretchers [9], compensation fibres in temperature cabinets [10-11], electrical delays and phase shifters [12-14]. For phase stabilisation this suffices to compensate the arising delay fluctuations. However, for synchronising the reference signals having a frequency of 97.7 kHz this is not sufficient because the phases have to be shifted by several microseconds. For this reason, a new method of phase correction was developed.

Not the phase of the system clocks are shifted, but new reference signals are created from these using digital frequency generators. The phase of the reference signals can be shifted in relation to the phases of the system clocks at the entry of the generator. In the following, the principle of direct digital synthesis (DDS) according to which the frequency generators operate and the resulting properties for the system are first described. After that the system parameters achieved in the prototype are presented, and lastly a way of enhancing performance even further is shown.

DIRECT DIGITAL SYNTHESIS

The structure of a DDS unit is shown in Fig. 3 [15, p. 25], [16, p. 21], [17, p. 1]. For the purpose of explaining the functioning principle, it is assumed that the phase register at the beginning contains the value 0. With the first clock pulse, the value of the *FTW* (frequency tuning word) is added to the content of the phase register. The adder at the same time performs the arithmetic operation modulo 2^M and the result is written into the phase register[‡], with M standing for the binary word length of the phase accumulator. The phase register can receive values between 0 and 2^M-1 which represent phases from 0 to nearly 2π. With the next clock the value of the *FTW*, which is constant in the application considered here, is added to the phase register. This process is repeated with each further clock, with the phase values accumulating in the phase register. In the bottom left of Fig. 3, this accumulation is represented for the first 8 clocks with an $FTW = 2^{M-3}$.

A phase shifter represents the next step of the DDS unit. Here, a phase displacement can be added to the current value of the phase register. The size of the phase displacement is predefined by the *POW* (phase offset word). Since its word length N as a rule is smaller than that of the phase accumulator, it has to be multiplied[§] by the factor 2^{M-N} to enable phase shifts of any size. However, this reduces the resolution of the phase displacement. The result of a displacement by 90° at the exit of the phase shifter can be seen in Fig. 3 below once again for the first 8 clocks. After that the phase values are normalised to 2π and in this way the phase signal is

$$\varphi_{DDS}(n) = \frac{2\pi}{2^M}\left[\left(nFTW + 2^{M-N}POW\right) \bmod 2^M\right] \quad (1)$$

obtained. The phase signal is fed to a phase-to-amplitude converter which via a look-up table assigns to each phase value $\varphi_{DDS}(n)$ an amplitude value $x(n)$[**] and outputs the same. This gives rise to a time- and value-discrete signal

$$x(n) = a \cdot \sin\left[\frac{2\pi}{2^M}\left(nFTW + 2^{M-N}POW\right)\right], \quad (2)$$

with the amplitude a, which is then converted in the digital-to-analogue converter into an analogue signal

$$x(t = nT_{clock}) = a \cdot \sin\left[\underbrace{\frac{2\pi}{2^M T_{clock}}FTW}_{\omega_{DDS}} \cdot t + \underbrace{\frac{2\pi}{2^N}POW}_{\varphi_{DDS,Off}}\right]. \quad (3)$$

The output signal of the DDS unit with $f_{clock} = 1/T_{clock}$ exhibits the frequency

$$f_{DDS} = \frac{FTW}{2^M} f_{clock} \quad (4)$$

[‡] Actually, the phase register overflows at the value 2^M and starts again at 0.

[§] The multiplication is achieved by bit shifting of the binary *POW*.

[**] In real systems, the phase normalising is also performed in this functional block.

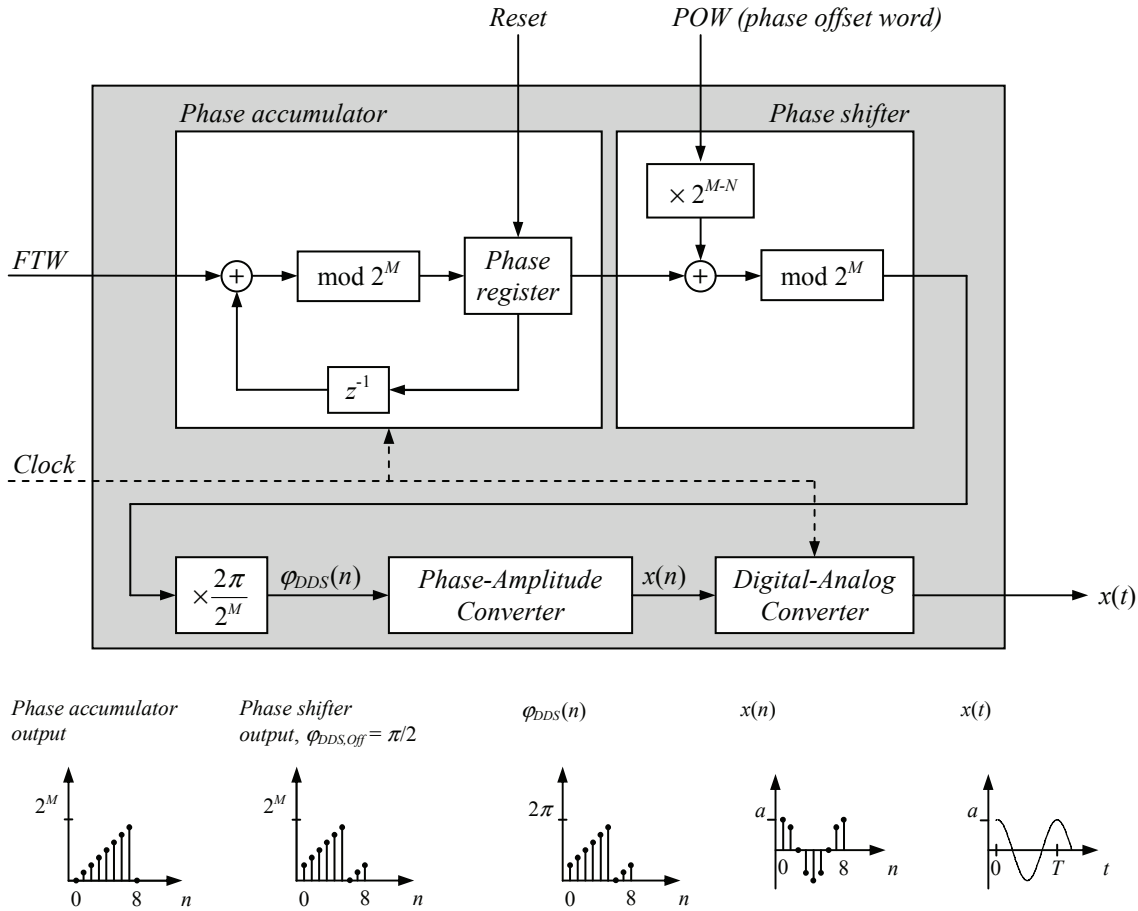

Figure 3: Direct digital synthesis principle.

and the phase displacement

$$\varphi_{DDS,Off} = \frac{POW}{2^N} 2\pi. \qquad (5)$$

REFERENCE SIGNAL GENERATION

Fig. 4 shows how two DDS units are used to generate the reference signals. Both were clocked by the system clock 1 at the frequency $f_{clock,1}$ = 200 MHz. DDS_1 works at the $FTW_1 = 2^{M-2}$ and DDS_2 at the $FTW_2 = 2^{M-11}$, which is why according to Eq. (4) they generate the frequencies $f_{Ref,1}$ = 50 MHz and $f_{Ref,2}$ = 97.65625 kHz[††]. The following integer relationships arise between the frequencies of the system clocks and reference signals which all have a uniform time reference:

$$\frac{f_{Ref,2}}{f_{clock,2}} = 1 \qquad \frac{f_{Ref,1}}{f_{Ref,2}} = 2^9 \qquad \frac{f_{clock,1}}{f_{clock,2}} = 2^{11}. \qquad (6)$$

As a matter of principle, then, there is a constant phase relationship between the system clocks and the reference signals. However, this phase relationship is still undefined, which is resolved by the possibility of setting the phase registers of both DDS units to zero. This is done by means of system clock 2. To initialise the reference generator, the phase registers of both DDS units are set to zero after the positive edge of system clock 2 to the next positive clock edge of system clock 1 and this value is output by the phase accumulator at initialisation time n = 0. The following phase accumulation is then once again similar to that of the example in Fig. 3. Now the phase displacement between the system clocks delivered to the reference generators at interface 2 and the reference signals is known (Fig. 4)[‡‡]. The last step for generating the reference signals consists in adjusting the phases at the exit of the reference generators by means of the phase shifters of the DDS units in such a way that they are synchronous at all reference points. For this purpose, a correction is made by calculating the phase values from the delays that were determined by the measurement unit which, after being converted into the binary form of the *POW*, are delivered to the DDS units which perform a corresponding phase shift.

[††] As a matter of principle, the exact generation of 100 kHz for Reference Signal 2 is not possible according to Eq. (4).

[‡‡] In practice, the delays in the DDS unit still have to be taken into account.

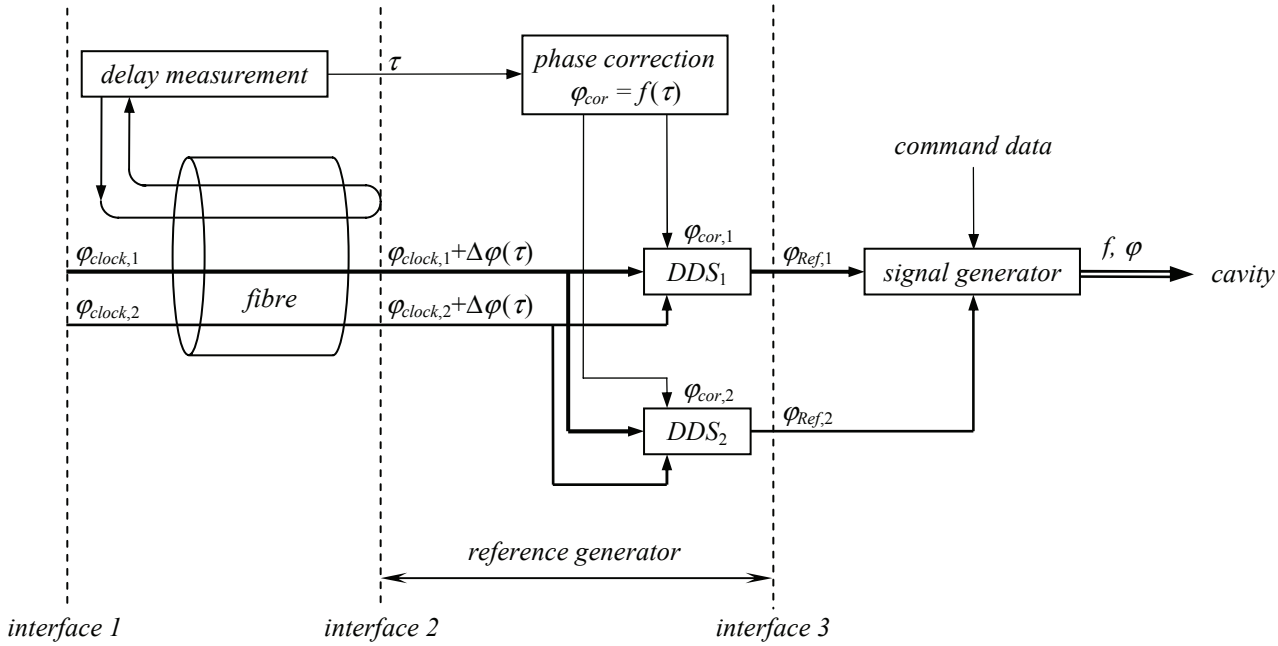

Figure 4: Generation of the reference signals.

PERFORMANCE

Now that the functioning principle of the reference generators has been explained, a description of the practical properties of the DDS units used (Fig. 5) will be provided. In Tab. 1 the values for the examined key values of the standard deviation of jitter, increment and precision of time adjustment are listed for each of the two reference signals. For the overall precision of the reference time, the quality of Reference Signal 1 is decisive.

Table 1: Quality of the Reference Signals

	Jitter	Increment	Precision
Reference Signal 1	7.56 ps	1.22 ps	< 7.5 ps
Reference Signal 2	140 ps	625 ps	527 ps

The jitter of Reference Signal 1 was measured directly at the generated sinusoidal oscillation, whereas Reference Signal 2 was converted prior to the measurement into a rectangular signal by means of a comparator[‡‡]. The latter facilitates further signal processing beyond interface 3 in the signal generators of the cavities. Moreover, phase relationships of Reference Signal 2 to the other signals can be measured significantly better given the higher edge steepness. The increment by which the time information of the reference signals can be shifted results from Eq. (5) in

$$t_{inc} = \frac{\left(\Delta\varphi_{DDS,Off}\right)_{\min}}{2\pi} T_{DDS} = \frac{1}{2^N f_{DDS}} . \qquad (7)$$

[‡‡] The comparator is integrated into the DDS unit.

The *POW* of the DDS units used has a binary word length of 14 bits, resulting in an increment of 1.22 ps. To measure the precision of the time adjustment, two reference generators were connected via phase-stable, electrical components directly, i.e. without an optical network, to the system clock source. After that a phase synchronisation was performed and the extent to which the phases of both signals drifted apart was measured. Here, the phase displacement was always meaned over a time period of one second to suppress the influence of the jitter. Fluctuations occurred whose maximum amplitudes are recorded in Tab. 1. When the precision of Reference Signal 1 was measured, the difference between the minimum and maximum phase deviation over a time period of 7 hours was below the measurement precision of the oscilloscope of 15 ps. From this it is concluded that the precision is better than 7.5 ps.

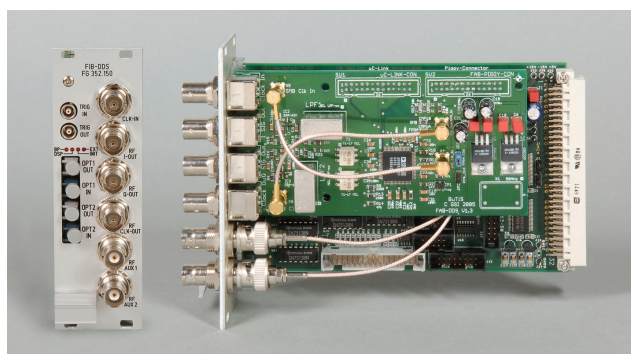

Figure 5: DDS unit.

All values for Reference Signal 2 in Tab. 1 are poorer due to the lower frequency, but perfectly adequate to satisfy the task of this signal of clearly identifying an edge of Reference Signal 1. The probability of an incorrect assignment approaches nil [5, p. 160]. This

ensures that commands to change the frequency and phase can be carried out synchronously in the different signal generators of the cavities (Fig. 2 and 4).

SUMMARY

A new method allowing for the generation of reference signals for synchronising cavities has been presented. This is done by means of digital frequency generators that work according to the direct digital synthesis principle (DDS). The phase of Reference Signal 1 (50 MHz) can be adjusted at increments of 1.22 ps and a precision of better than 7.5 ps. The jitter of the signal has a standard deviation of 7.56 ps.

All of the described values were subjected to practical examination.

A significant advantage compared with methods used to date to compensate for delay fluctuations in systems for distributing phase-stable signals is that the phase deviation is unlimited. The phases of the reference signals can be adjusted as desired and at small intervals.

OUTLOOK

The performance of the method presented can be enhanced even further by two measures. Firstly, the frequency of system clock 1 and of Reference Signal 1 must be increased (e.g. to 1 GHz, and 250 MHz, respectively) and, secondly, DDS units of a different type other than those of the prototype which can be clocked at such a high frequency must be used. Such DDS units are now available commercially and also bring further advantages in terms of precision [18]. The big advantage lies in the reduction of the jitter produced by the reference generator to a value of < 1 ps. Moreover, the increment is reduced by a *POW* having a large binary word length of 16 bit and the higher frequency of 250 MHz according to Eq. (7) to a value of 61 fs.

With these considerations it has to be kept in mind that developments in the area of frequency generators operating according to the DDS principle are advancing continually, and that in future even higher clock rates as well as larger word lengths of the *POW* and thus also even better properties for generating reference signals can be expected.

If combined with more effective temperature and delay stabilisation of the reference generators, this improvement will also enhance the precision with which the reference time can be adjusted.

The presented method can also be used in other systems to generate a stable reference signal if the DDS unit is capable of generating a frequency high enough for this.

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