BEAM POSITION MONITOR SYSTEM OF THE ESS LINAC

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Abstract

The pulsed ESS Linac will include about 100 BPMs, mostly with a European XFEL style button design, 6 BPMs with a special design for the Medium Energy Beam Transport, as well as 8 compact-size BPMs foreseen for the Drift Tubes. The required accuracy and resolution of the position measurement are 100 µm (rms) and 20 µm (rms) respectively with the 50 mA 2.86 ms nominal pulse. In addition to the position measurement, the BPM system needs to measure the beam phase in the nominal pulse as well as several diagnostics pulse modes with a minimum duration and intensity of 5 µs and 5 mA respectively. After a study of the possible electronics platforms, MTCA.4 is now considered as the main prototyping platform for the high performance sub-systems at ESS. It is foreseen to prototype a Rear Transition Module for IQ-based RF signal measurements intended for both the BPM and LLRF systems. The requirements and specifications of the BPM system are presented and the plan for the continuation of the project is described in this paper.

INTRODUCTION

The 352.21 MHz and 704.42 MHz pulsed ESS Linac will include in total about 140 BPMs of various types. In addition to the transversal beam position, the BPMs shall be able to measure the beam phase for energy calculations based on time-of-flight measurements. Furthermore, the BPM system needs to measure the beam position and phase in several diagnostics pulse modes with a minimum duration and intensity of 5 µs and 5 mA respectively. Table 1 summarizes the main specifications of the BPM system.

Table 1: Main BPM System Specifications

Parameter	Value	Unit
Position measurement accuracy	100	µm (rms)
Position measurement resolution	20	µm (rms)
Phase measurement accuracy	1	° (rms)
Phase measurement resolution	0.2	° (rms)
Phase measurement range	±180	°
Measurement range (w.r.t. beam pipe)	50	%
Electronics response time	< 1	µs
ADC sample rate	10-100	MSPS
Refresh rate (end user)	14	Hz

It is planned to use a single type of electronics for all the BPMs. Therefore, the design of the front-end electronics should be flexible so that it can be adapted to all types of the BPM detectors through minor modifications. The electronics should have a large dynamic range and a high bandwidth, so that the BPM system gives useful results, even when the pulse amplitude and duration are decreased to minimum values.

The BPM front-end will include a fast analogue front-end, where the BPM signals are picked up by some sensitive electronics, level-adjusted, down-converted (to be confirmed), filtered and conditioned. The signals are then digitized and fed into an FPGA for position, phase and intensity calculations, linearization, memory read/write etc. The BPM electronics will be integrated into the future EPICS control system.

CONCEPT

Following a study of the available electronics platforms and as part of an electronics standardization strategy, MTCA.4 is considered as the main candidate for the high performance electronics at ESS, including the BPM and LLRF systems. The main reasons for choosing MTCA.4 against other platforms include: timing and synchronization resources, possibility of using a Rear Transition Module (RTM), high redundancy/availability and future support. Figure 1 shows a simplified schematic view of the BPM system, which is currently being prototyped at ESS. The induced voltages on the buttons are transferred by four coaxial cables to the MTCA.4 crate, to be located in the future ESS Klystron gallery. The crate houses several electronic modules such as a RTM performing the required analogue signal processing, a digital board for ADC sampling and digital signal processing, a CPU running under Linux where EPICS drivers for the electronic cards will be installed, a MicroTCA Carrier Hub (MCH) managing the crate and handling the interconnection among the modules, a timing module providing the required timing and synchronization signals and finally, the infrastructure modules such as power and cooling.

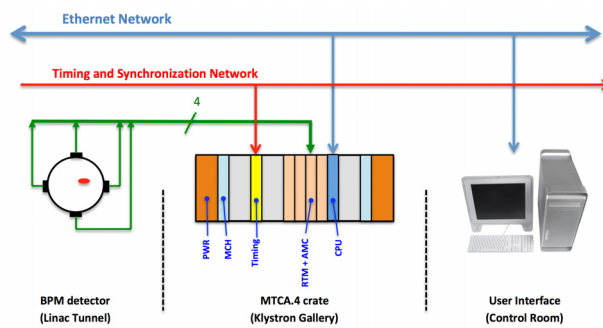

Figure 1: Simplified schematic of the BPM system including the detector, MTCA.4 crate and the terminal.

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BPM DETECTOR

Figure 2 shows a draft design of the quadrupole doublet located between each two consecutive cryomodules in the cold Linac. The two quadrupoles will transversally focus the beam along the horizontal and vertical axis with a BPM mounted in each quadrupule. The beam pipe diameter for the quadrupole BPMs will be either 60 mm or 100 mm. These BPMs will be of button type with a European XFEL button style design [1].

It is foreseen to use 8 BPMs for the 4 DTL tanks (2 BPMs per tank). These BPMs should have a compact size, similar to the SNS type, to be mounted in the Drift Tubes. Also, several wide-aperture BPM detectors might be used in the Medium Energy Beam Transport (MEBT) and the Accelerator-to-Target line, where the beam pipe has a larger diameter.

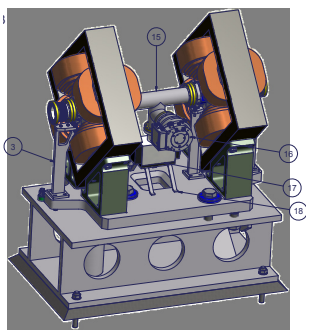

Figure 2: Draft design of the quadrupole doublet.

Detector Signals

Using the equations presented in [2], the button voltage is simulated in MATLAB for the ESS beam with the result shown in Fig. 3. Figure 4 shows the Fourier spectrum of the button voltage due to a 352 MHz repetitive bunch. For a longitudinally well-focused beam (i.e. σ_{bunch} in the order of 2-3 mm), the amplitudes of some higher harmonics are larger than the fundamental one. As the beam gets defocused, though, these harmonics quickly decrease, and with a σ_{bunch} above 50-60 mm, they become negligible. This suggests using the lower harmonics for the BPM signal processing. On the other hand, processing in same frequency as the RF power is not desirable due to the potential interference with the high power RF sources. Therefore, it is planned to process the second harmonic (i.e. 704 MHz) in the first part of the Linac operating at 352 MHz, while processing the fundamental harmonic in the second part of the Linac where the RF frequency is doubled. The ability to measure the beam position/phase with a de-bunched beam is important, for example during the machine tuning when the aim would be to perform a cavity phase scan while looking at the beam position several hundred meters down stream, before the target, with no additional longitudinal focusing in between.

Considering the extreme cases for the beam and assuming a measurement bandwidth of 10 MHz and a noise factor of 10 dB for the electronics, the thermal noise will translate into the positions errors shown in Table 2 after the spoke section. The cases marked by "-" indicate that the BPM signal cannot be distinguished from noise. In order to make sure that the BPM system will give useful results with a debunched beam, the XFEL button size may be increased for ESS.

Table 2: Position Error due to Thermal Noise

Parameter	352 MHz	704 MHz
I_{beam} = 50 mA, σ_{bunch} = 2.5 mm	4.4 μm	3.4 μm
I_{beam} = 5 mA, σ_{bunch} = 2.5 mm	43 μm	34 μm
I_{beam} = 50 mA, σ_{bunch} = 170 mm	49 μm	-
I_{beam} = 5 mA, σ_{bunch} = 170 mm	-	-

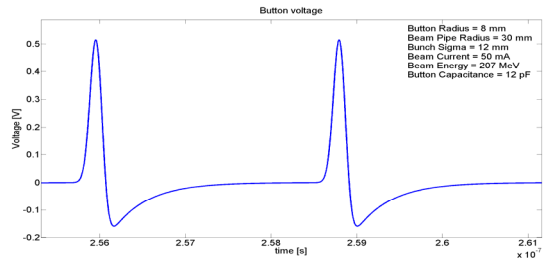

Figure 3: Simulated button voltage due to each bunch.

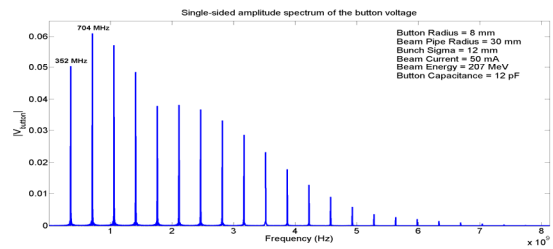

Figure 4: Fourier spectrum of the button voltage.

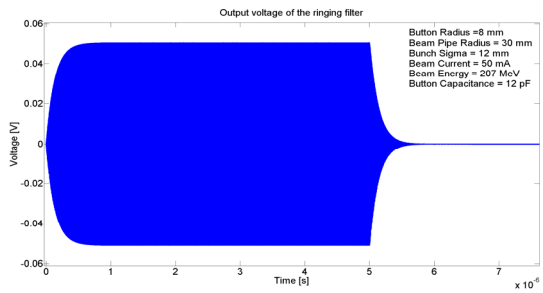

Figure 5: Simulated response of the band-pass filter.

BPM ELECTRONICS

Analogue Front-end

The BPM signals will be transferred to the analogue front-end using four well-shielded coaxial cables with low attenuation and equal lengths. The BPM cables will be about 60 m long with their lengths equalized to less than 1 mm. In the analogue front-end, depending on the RF frequency, either the first or the second harmonic will pass through the electronics and all the other harmonics will be filtered out. These filters should be carefully designed so that they sufficiently suppress the unwanted

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harmonics and noise while giving a fast enough response with a narrow beam pulse. Figure 5 shows the simulated response of the band-pass filter to a 5 μs pulsed beam with a settling time of less than 1 μs. Besides filtering, the analogue front-end conditions the detector signals and amplifies (and/or attenuates) them so that their level becomes compatible with the ADC inputs.

Digital Back-end

Two solutions are currently being considered for measuring the button signals, being IQ sampling (or IQ under-sampling) in 1) RF 2) IF.

With the first solution, a fast ADC will be used to sample the RF signal (i.e. 352 MHz or 704 MHz) directly. One possibility would be to set the sample time to $(n + 0.25)T$ where T is the period of the RF signal and n is an integer number to be chosen based on the ADC speed. This, will result in a digital steam of I, Q, -I, -Q… where I and Q are the in-phase and quadrature-phase components of the RF signal. A higher sample rate (i.e. lower n) is in general preferred as it enables baseband noise reduction through averaging. The second solution is based on down-mixing the RF signal to IF before IQ sampling.

Sampling in RF has the advantage of increasing the measurement bandwidth and simplifying the design of the analogue front-end. The main drawback, is that, when implemented on an RTM, some signal degradations may occur due to the bandwidth limitation and cross talk at the connection point of the RTM to the digital module. Also, with this method, jitter requirements for the ADC clock becomes more stringent due to the higher ADC speed. Sampling in IF, on the other hand, eases the ADC sampling, because of the lower IF signal frequency and less bandwidth requirements. The compromise, however, lies in the additional complexity of the analogue front-end due to the RF-IF conversion stage.

Both of these solutions are kept open for the BPM front-end, with a potential use for the LLRF system as well. The final decision should to be taken after advantages and drawbacks of both methods have been checked in practice.

The sampled BPM signals are, in the next stage, fed into an FPGA for the low-level digital signal processing including beam position/phase calculations and interfacing to the control system. Also, some additional features such as auto-calibration and post-mortem data capture might be added if needed. The FPGA code should be generic and flexible so that with little modifications, it could be used for all the BPM types. Also, system automation up to a certain level would be needed

TIMING AND SYNCHRONIZATION

Several timing and synchronization signals will be required for the BPM system. That includes the RF phase reference (in case an IF signal has to be locally generated), the 14 Hz machine trigger as well as the ADC clock. These signals should be all locked in phase/frequency to the ESS master clock, providing the RF reference for the whole Linac. Figure 6 shows the use of each timing signal. Two 14 Hz triggers will be used to mark the beginning and the end of the pulse flat-top. During this time, the beam parameters will be calculated and temporarily stored on a memory. Similarly, the beginning and the end of the gap will be marked by another two 14 Hz triggers, where the beam data will be published on the Ethernet network and made accessible to the end-user. The gap will be used also for auto-calibration and error compensation if needed. The 14 Hz triggers could be all external or partly generated by the FPGA. Details on how to implement these signals are currently being discussed with the ESS Controls Group. The BPM data will be time-stamped so that each data package could be associated with its pulse number. Time stamping may be alternatively performed at a lower level, such as the raw ADC output.

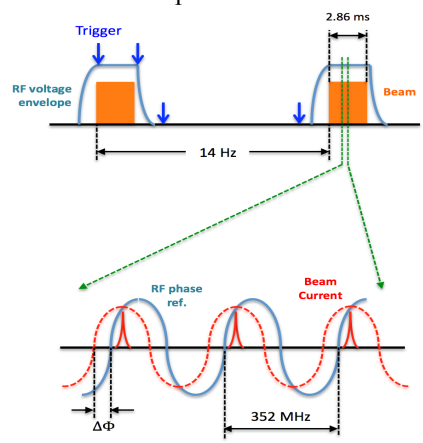

Figure 6: BPM timing and synchronization requirements.

SUMMARY AND NEXT STEP

This paper has outlined the main specifications the ESS beam position and phase monitors. The main parts of the system such as the BPM detector and the electronics have been described. The response of the BPM detector and the electronics has been simulated in MATLAB. Two alternative methods based on sampling in RF/IF have been studied and compared for the detection of the BPM signals with a potential use for the LLRF system as well. The BPM timing and synchronization requirements for the machine trigger, RF phase reference and ADC clock have been summarized. MTCA.4 has been chosen as the main candidate for the high performance electronics at ESS including the BPM system and tests with a prototype platform have been planned for the BPM/LLRF systems.

REFERENCES

[1] D. Lipka et al, Button BPM Developments for the European XFEL, DIPAC2011, Hamburg, Germany.
[2] S. R. Smith, Beam Position Monitor Engineering, SLAC-PUB-7244, July 1996.

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