Status and Implementation of Wideband Feedback System for e-p Instabilities in SNS

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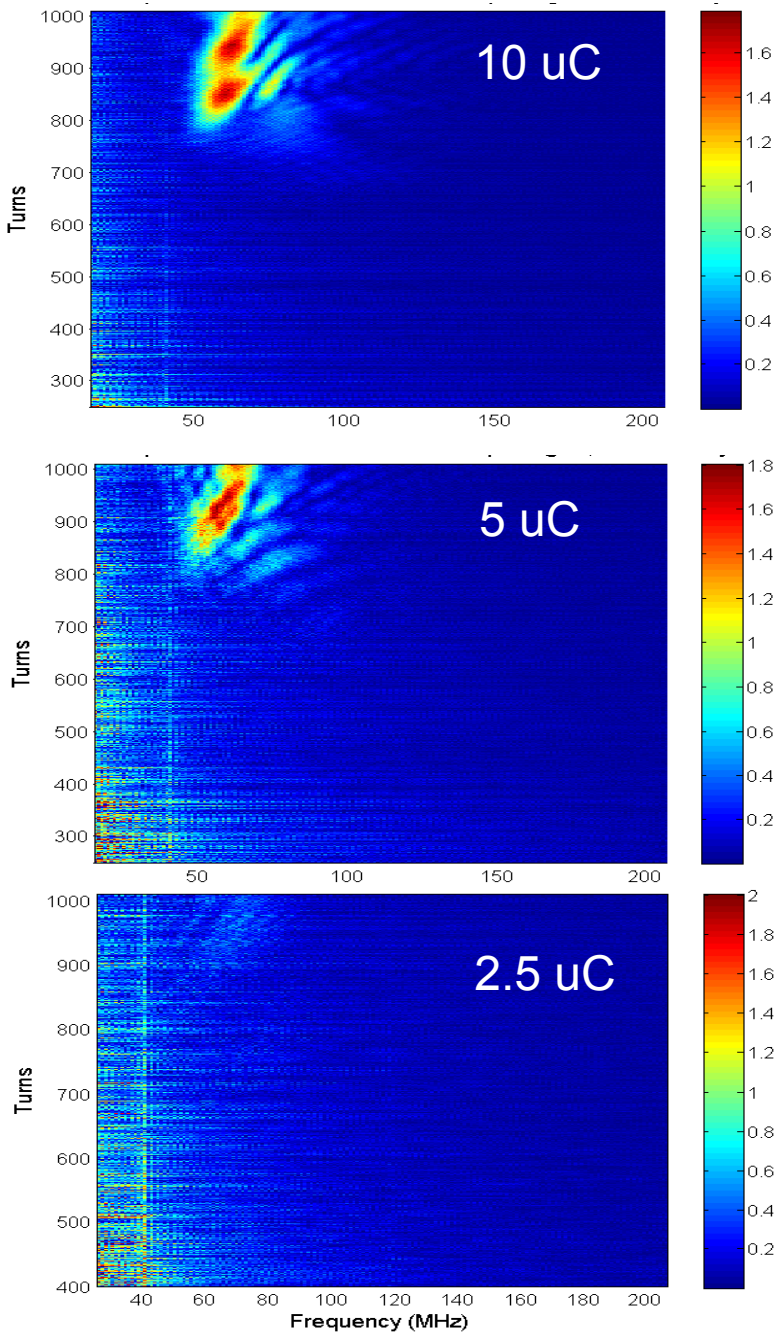
Overview

- **Currently using pickup / kicker designed at BNL with small modification to launch.**
- **Building new matched pickup / kickers.**
- **2 PA 1-300 MHz, 400 Watt. Additional one ordered**
- **Analog system being developed for early deployment***
- **Digital ADC/FPGA/DAC system being developed**

"Experimental Tests of a Prototype System for Active Damping of the E-P Instability at the LANL PSR," Deibele et. al, WEXC01, PAC 2007+ many others

Motivation and Background

April 2008: Beam Intensity Study - Frequency



Vertical instabilities stronger (shown here).

Here Instability does **not** obey theoretical law from Neuffer/Zotter:

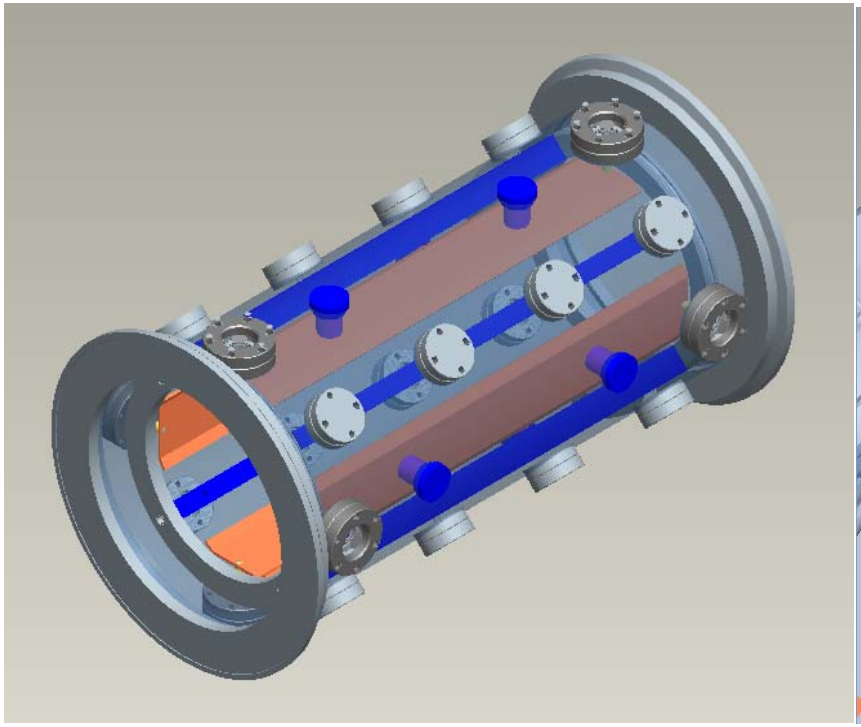
$$f \propto \sqrt{N}$$

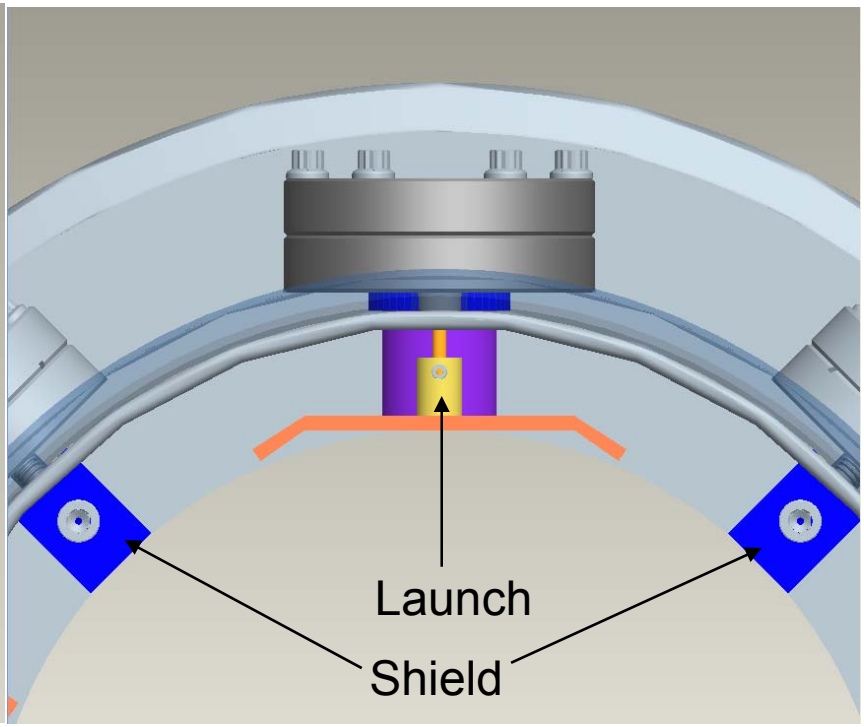
Previous studies for coasting beam only weakly obeyed this law (ECLOUD 2007)

Instability Observations in the Spallation Neutron Source Accumulator Ring
-S. Cousineau et. al.

New Electrode Design

New Electrode design



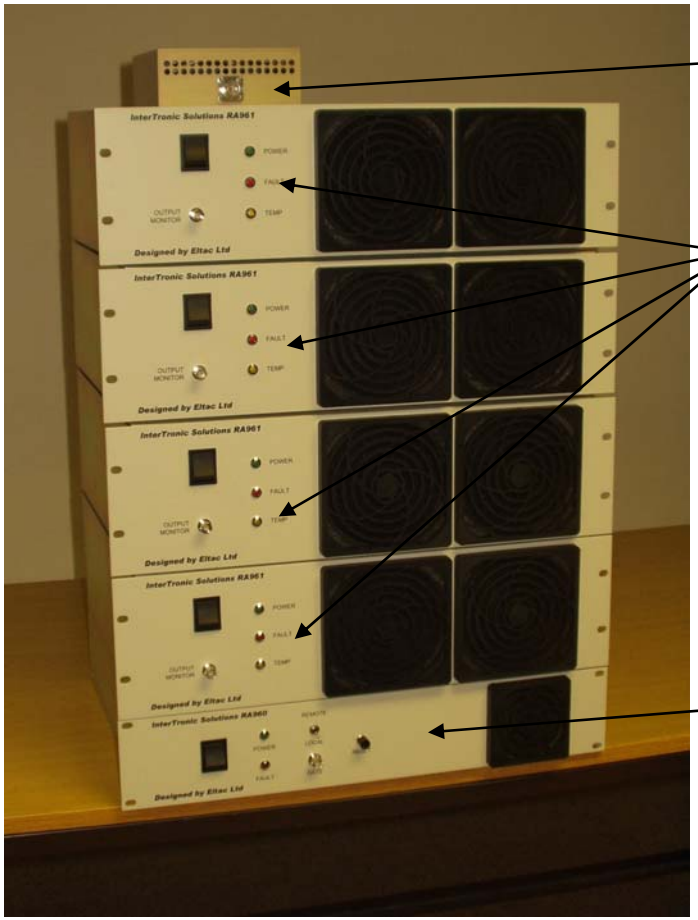


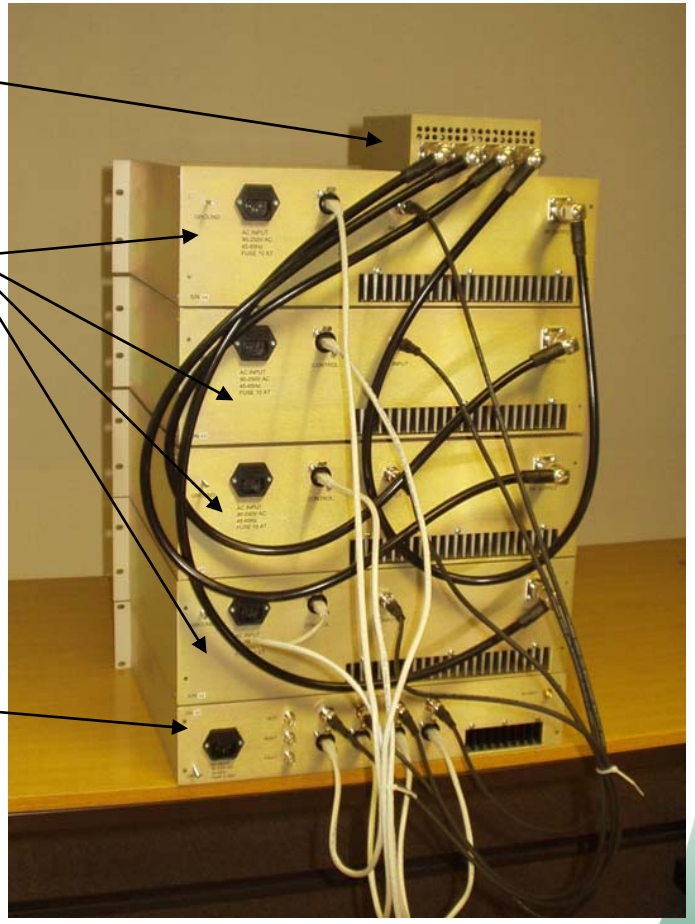
- **Signal from electrode launches to cable with better than -30 dB (calculated)**
- **Profile of electrode with angles simple to manufacture**
- **< -30 dB coupling from mode to mode**
- **Getting bids for funding**
- **TiN coating program beginning with collaboration of NFDD and WVU with Earl Scime**

SNS-NFDD

Power Amplifier

New Power Amplifier, 400W, 1-300 MHz



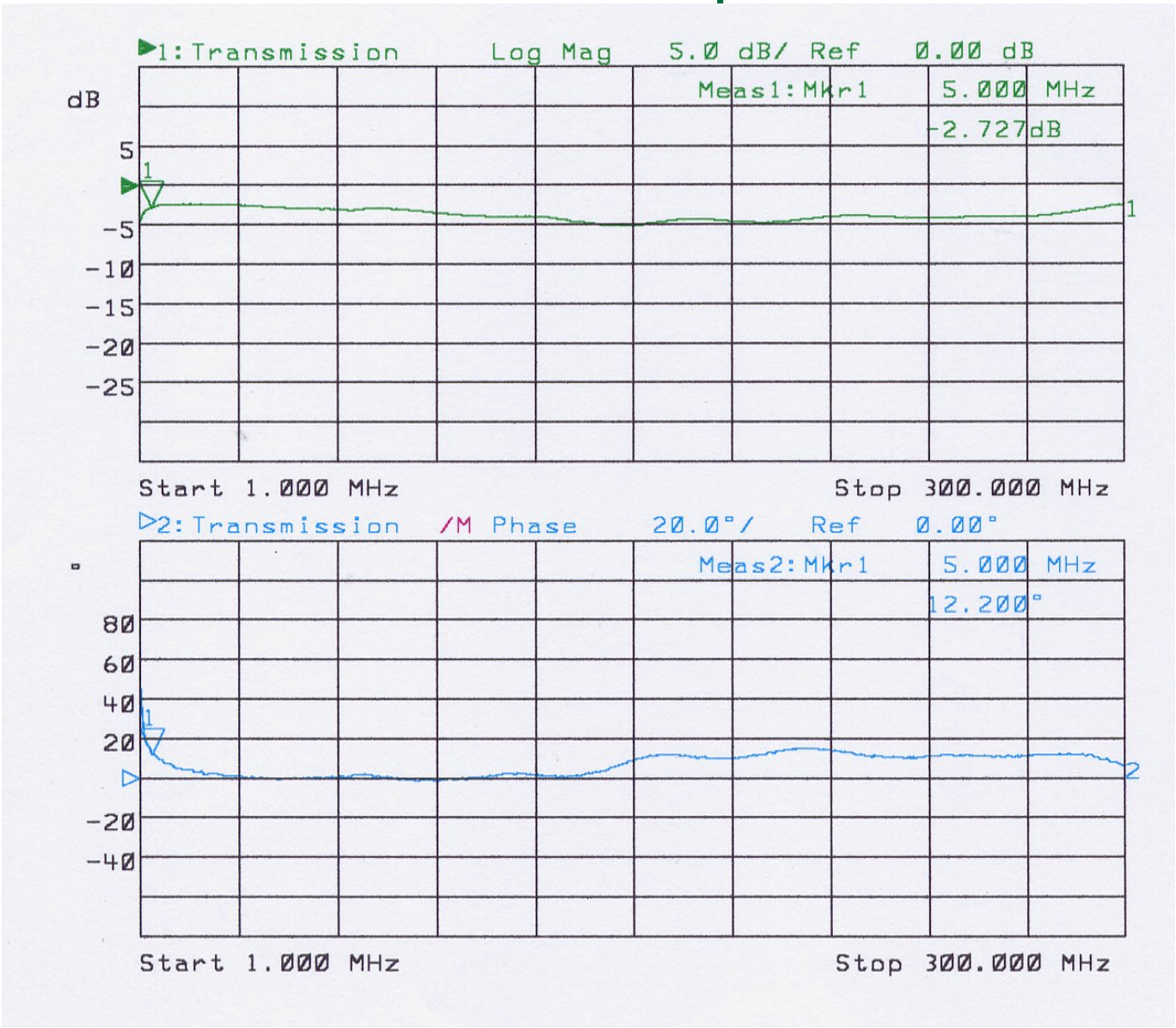


Photos by Intertronic Solutions / Eltac Ltd.

Amplifier Features

- **Complete solid state design.**
- **Gated to pulse the amplifier (reduce power requirement / heat load in rack)**
- **S_{11} < -25 dB**
- **4 stages of parallel 100 Watt amplifiers**
- **Werlatone power combiner on output**
- **Separate MPS control on current drive + temp sensors to each SiC MESFET.**
- **Class A operation**
- **Power supply in each chassis is simple 120V OTS power supply.**

Measurements of Amplifier



Measurements by Intertronic Solutions / Eltac Ltd.

Mixed Signal System Design

FPGA board Setup

- **One 10 bit 2 GS/s ADC/DMUX**
- **One 12 bit 2 GS/s MUX/DAC**
- **One VME/VXS 3.125 Gbit/s serial I/O links – VME rack is simply a power supply**
- **One Front Panel slot for 2.5Gbit/s UDP Ethernet transceivers**
- **Two 1 GB DDR SDRAM**
- **One Xilinx Virtex-II Pro FPGA**

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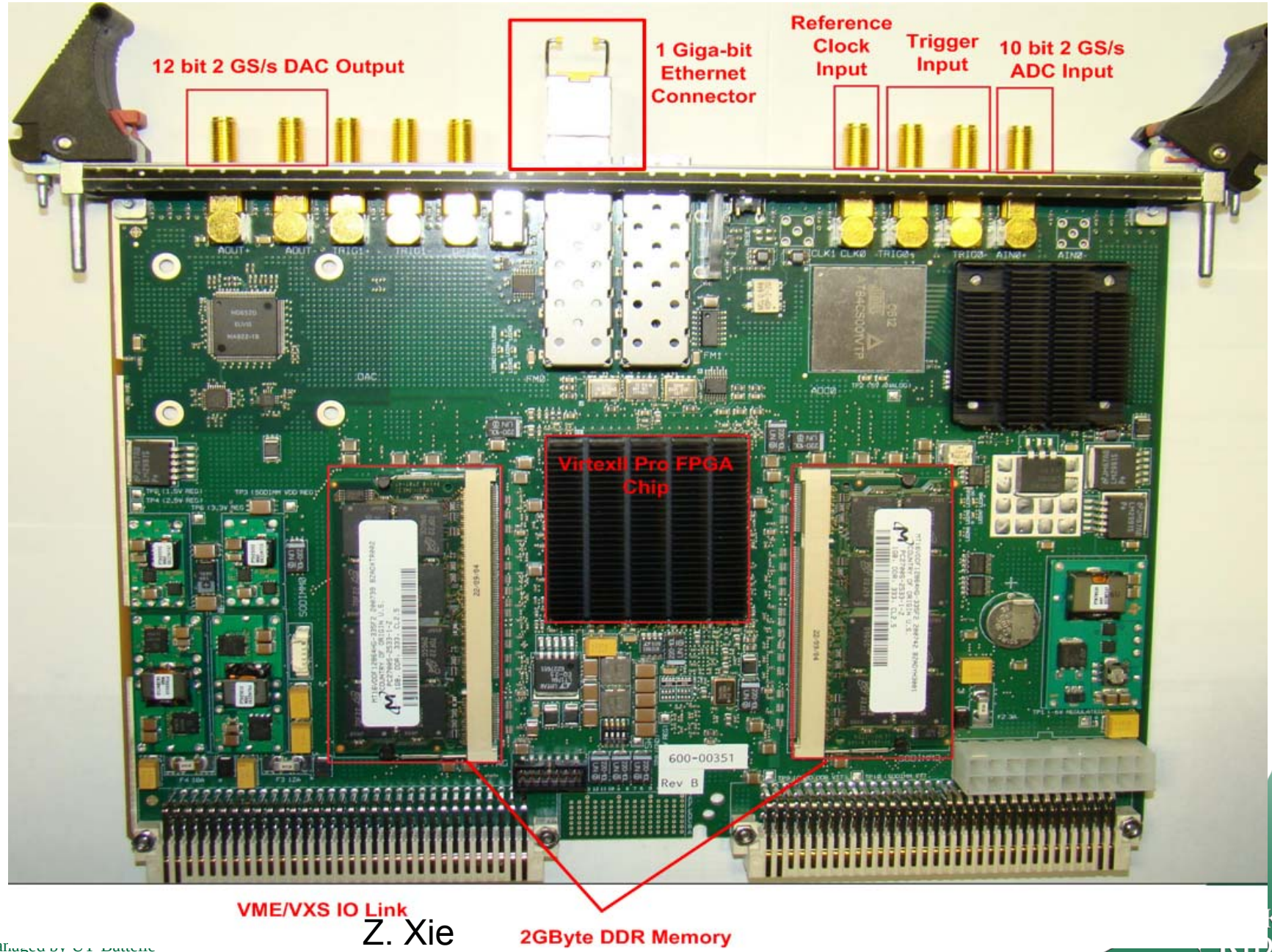
System Overview



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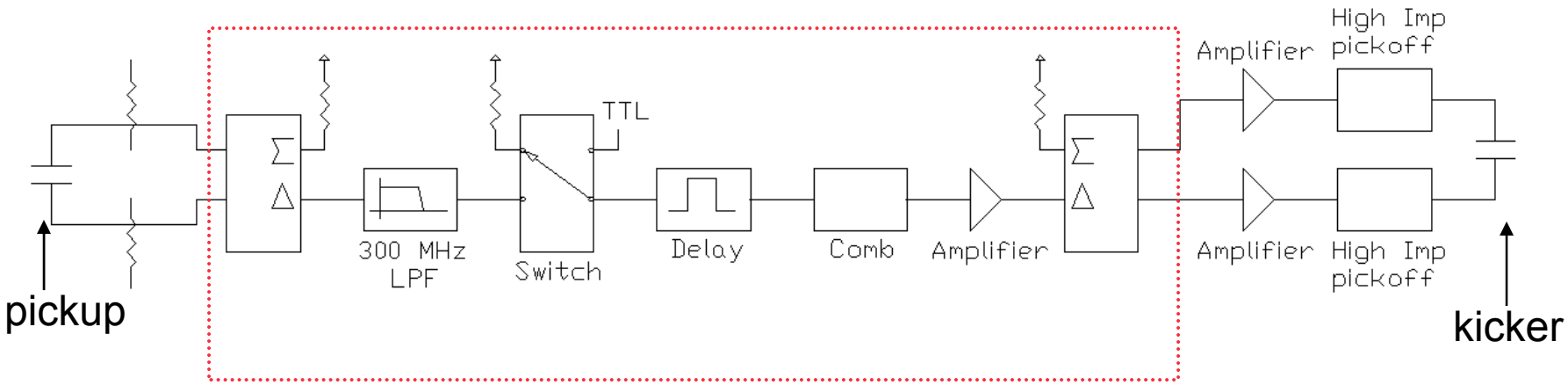
Analog Feedback Damper System



- **Portions of the analog system will be replaced by digital hardware**
- **New functionality and capabilities will be added**

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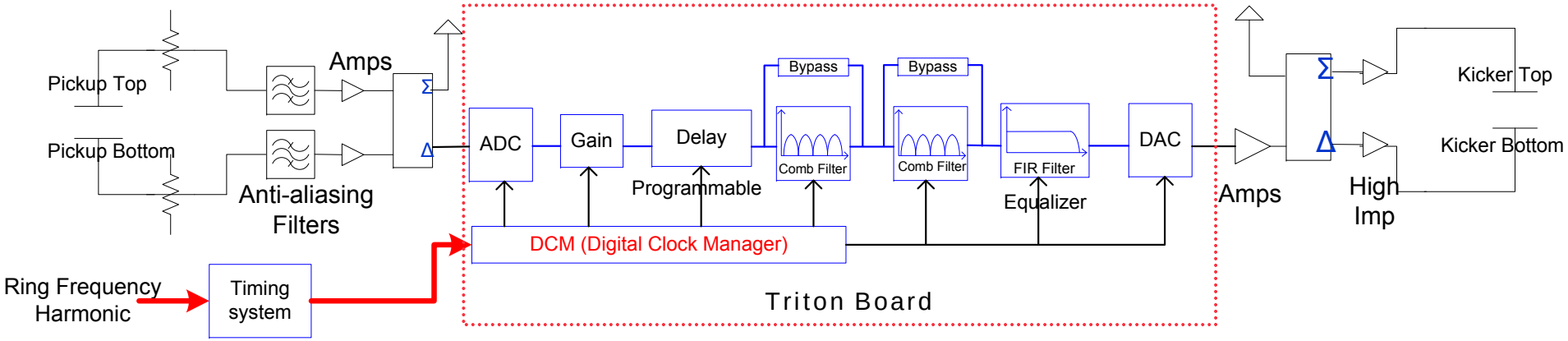
Mixed-Signal Damper System



- **The new system combines analog and digital components**
- **The digital components are clocked at a multiple of the ring frequency (1Mhz)**
  - **A multiple of 1600 is currently planned for the ADC and DAC**
  - **The ring frequency may vary slowly over time by up to 10%**
- **The common clock for the ADC, FPGA, and DAC must have very little skew.**
- **The overall latency from pickup to kicker is expected to be roughly 4 μsec**

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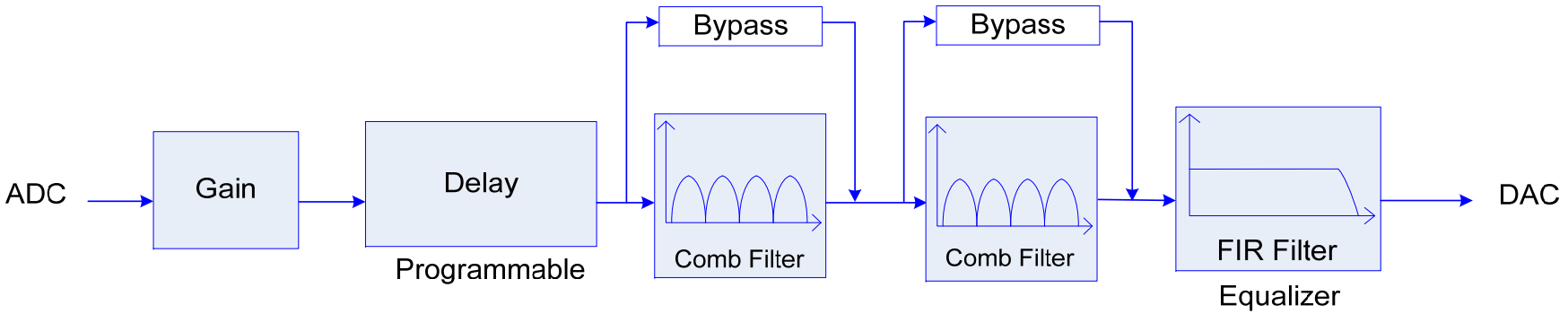
Data Processing on the FPGA



- **Each module is programmable and can be bypassed**
- **Gain multiplier controls overall system gain**
- **Programmable delay controls the overall system delay**
- **Comb filter can be 1 or 2 turns of delay**

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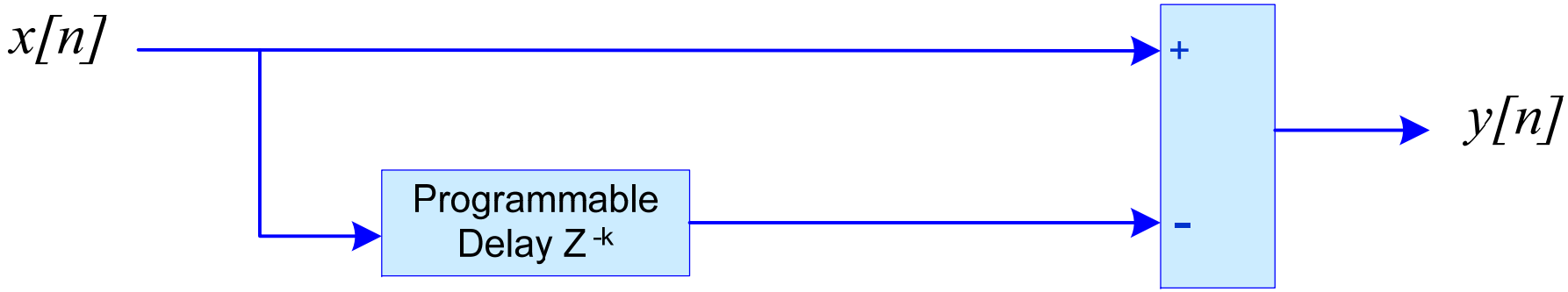
Comb Filters



- **The comb filters damp the ring harmonics leaving betatron sidebands, reducing RF power which would be used to also correct the closed orbit,**
  - **Comb filter output:** $y[n] = x[n] - x[n-k]$
  - **Comb filter frequency response:** $Y(z) = X(z)[1 - z^{-k}]$
  - ***k* is set to an integer that is a multiple of the ring frequency (for 1600MHz clock frequency, k = 1600, which corresponds to ~1 μsec delay)**

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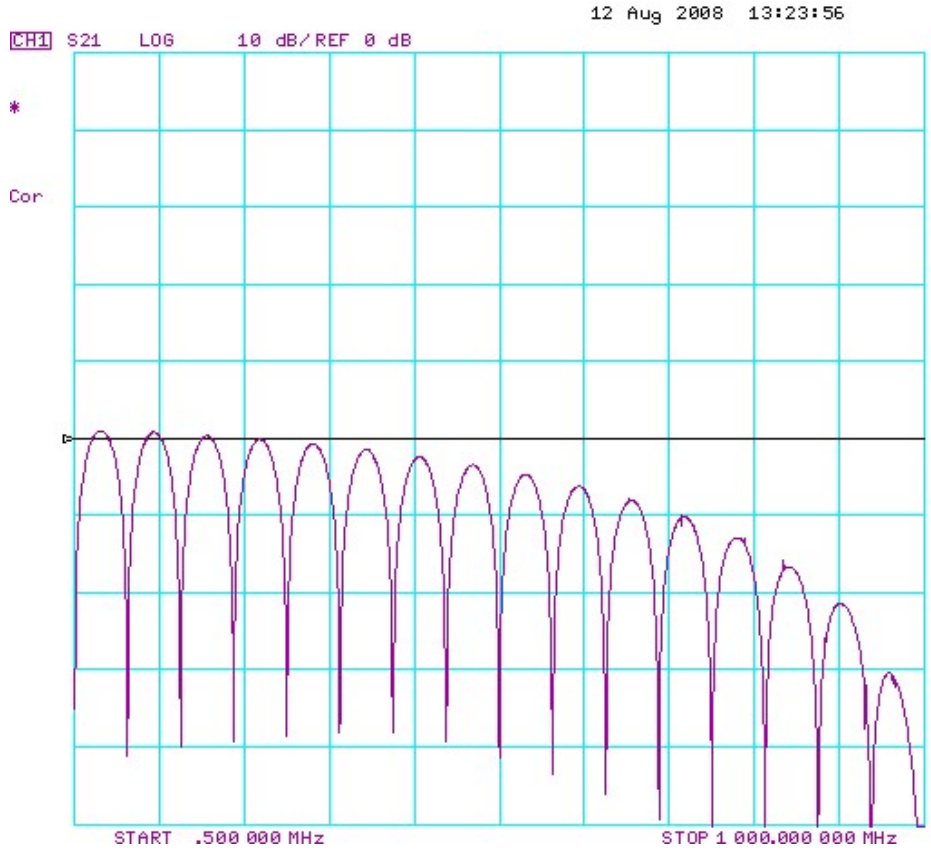
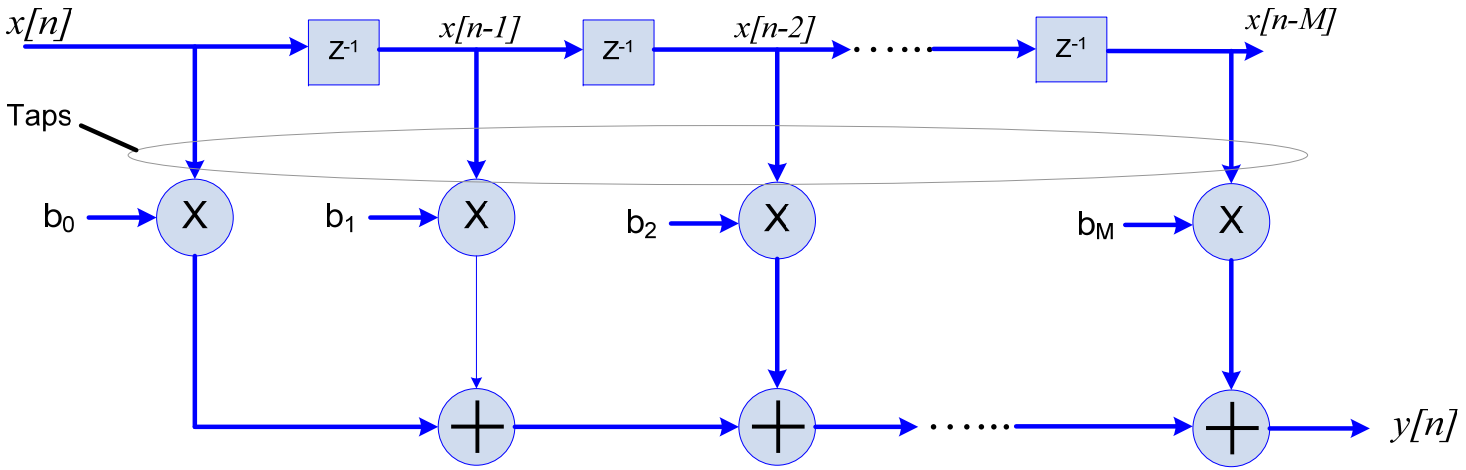
A Comb filter Implementation



S21 Magnitude measurement

S21 Phase measurement

Equalizer (FIR Filter)



- **The FIR Filter computes:** $y[n] = \sum_{k=0}^{M} b_k \cdot x[n-k]$
- **We expect to have a filter with 256 taps. A 16-channel parallel FIR filter which has a total of 256*(3/2)^4=1296 taps may be used.**
- **The FIR filter serves as an equalizer that corrects for dispersion in analog components**
  - **Electrodes have non-uniform gain verses frequency**
  - **Amplifiers have phase dispersion**
  - **Low-pass filters, cables, ADC, and DAC have magnitude and phase dispersion**

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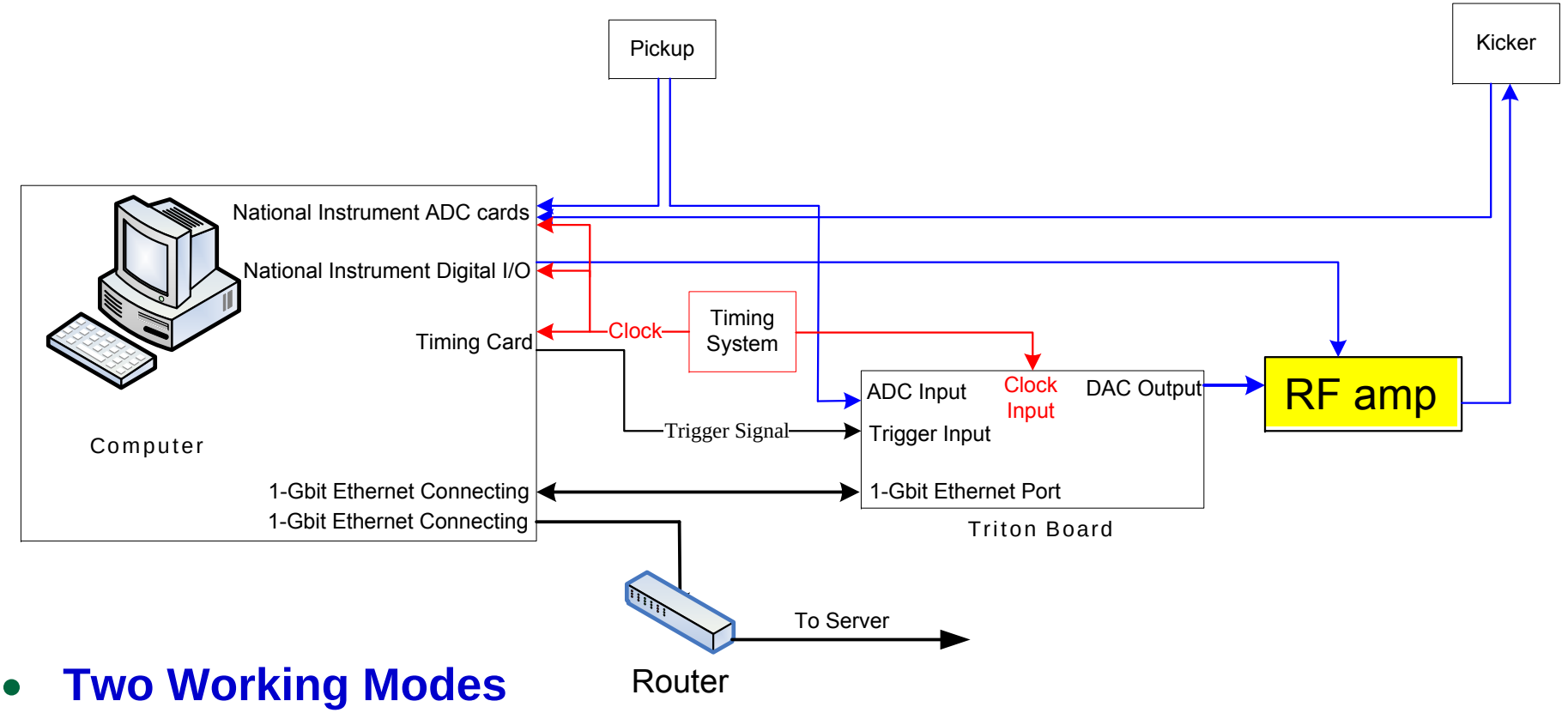
Overall System Setup



- **Two Working Modes**
  - **Dampening Mode**
    - **Actively dampening the instability through Triton Board**
  - **Research Mode**
    - **Capture the instability through National Instrument ADC cards**
    - **Perform adaptive self-learning algorithm**
    - **Reconfigure the Triton board for new parameters**

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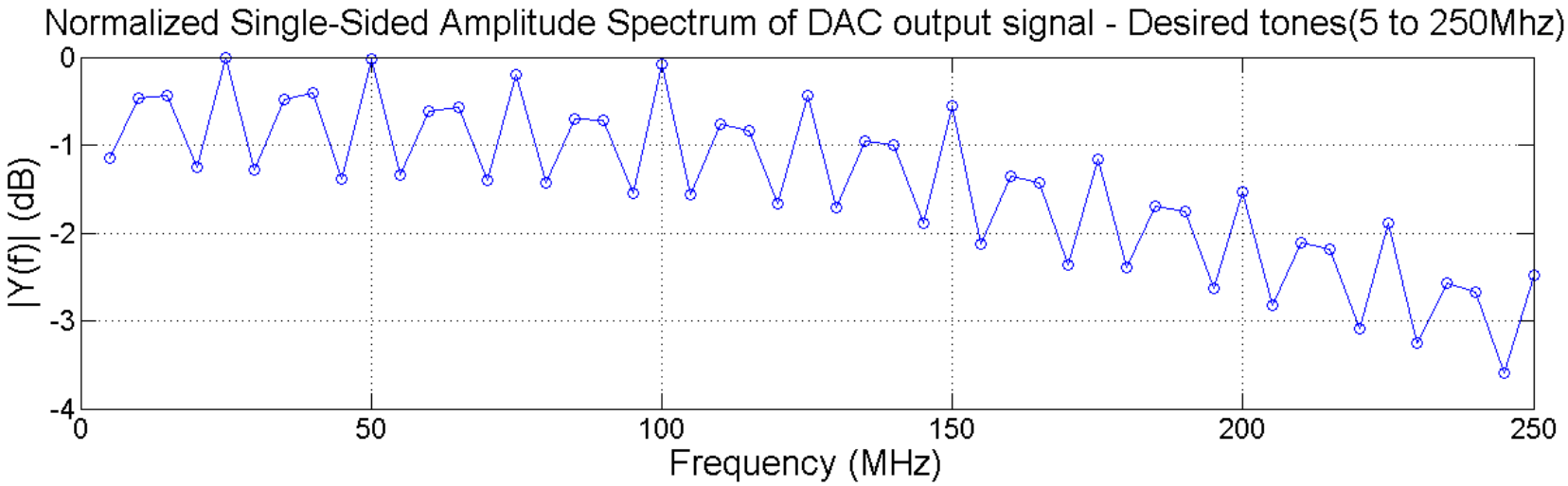
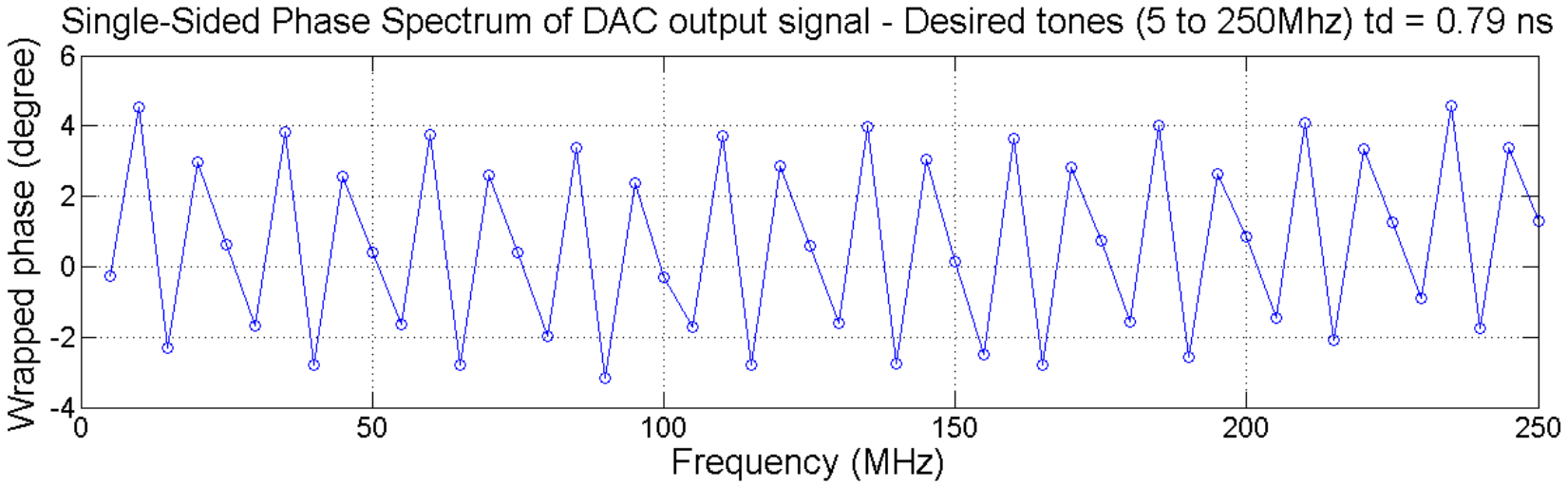
DAC Test Results





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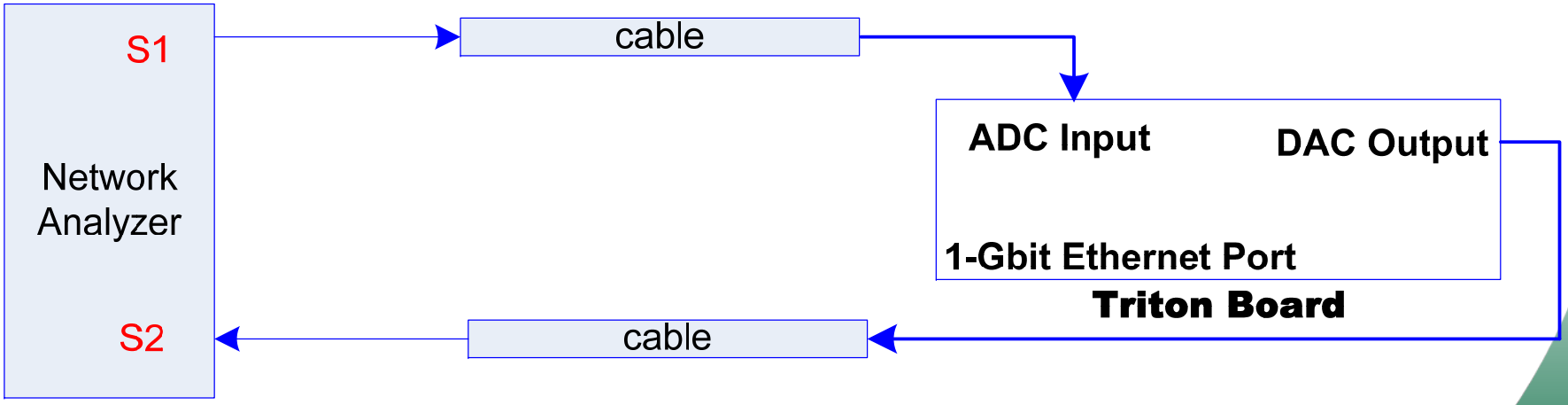
ADC->FPGA->DAC Test

- **Magnitude Dispersion**
  - **Measure magnitude linearity from 5Mhz to 500Mhz**
- **DAC Phase Dispersion**
  - **AC coupled ADC introduces 50 degree of phase dispersion at 1Mhz**
  - **Phase dispersion within 20 degrees from 10Mhz to 250Mhz**



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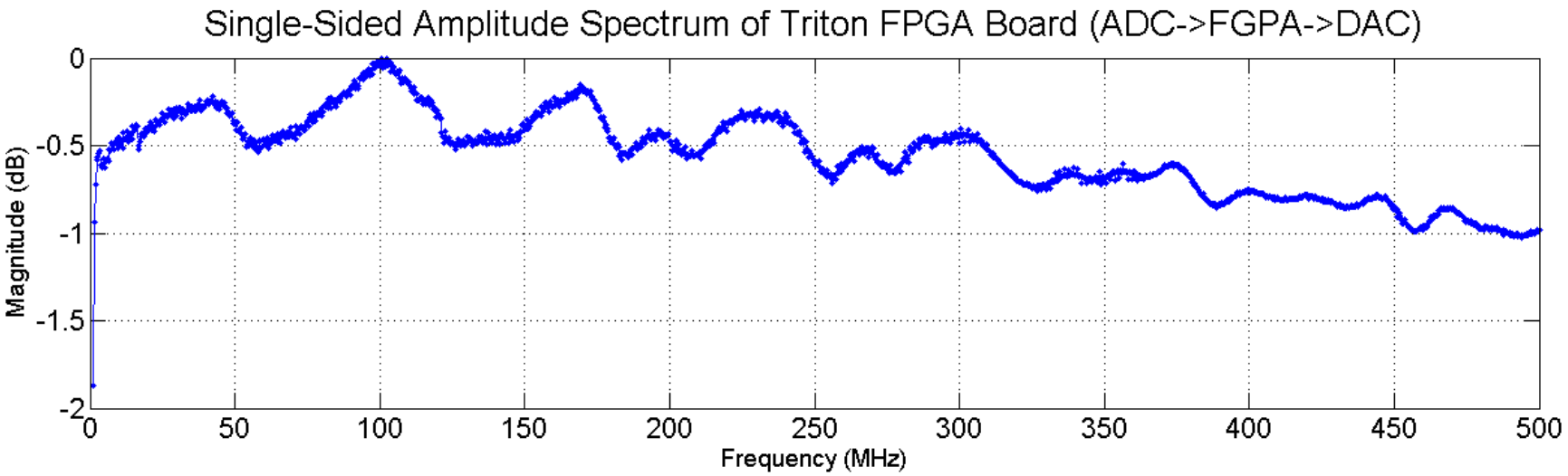
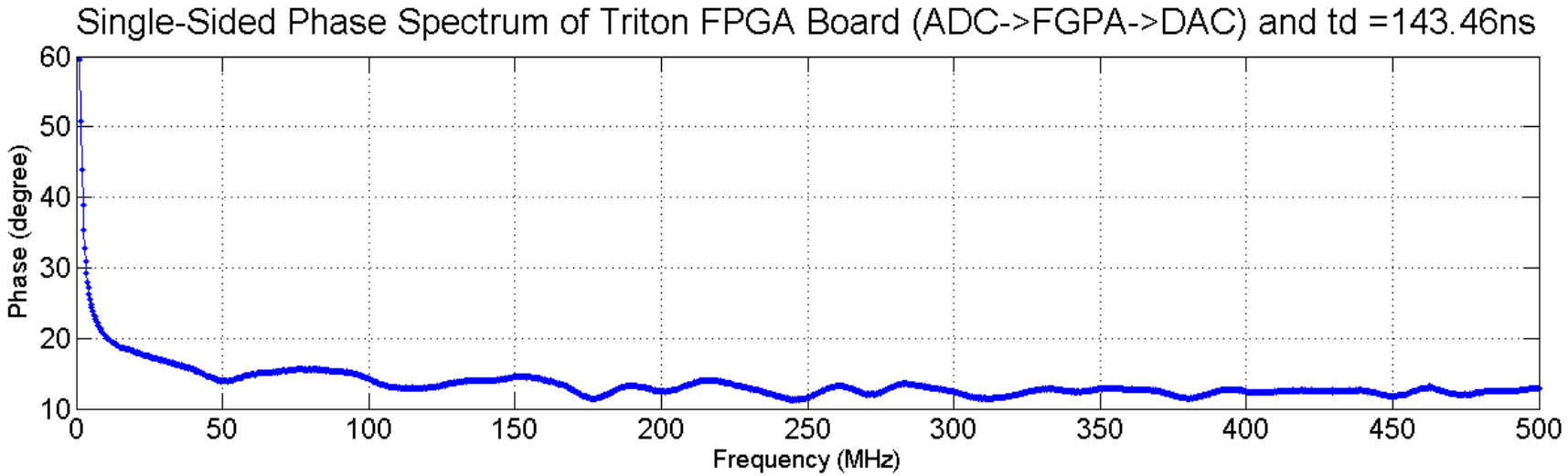
ADC->FPGA->DAC Test





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Outlook

- **Looking to have analog system complete and installed in the next 2-3 months for testing / modeling**
- **Version 0 of the full mixed signal system should be done in 7-8 months**
- **Full mechanical design of new pickup/kicker complete, going out for bid.**
- **Cabling and hardware harmonics of ring clock installed. Controls software needs to be implemented**
- **Racks are getting their AC power installed now.**

Finito