FABRICATION OF SELF-ALIGNED-GATE DIAMOND FIELD-EMITTER-ARRAY TRIODES FOR FREE-ELECTRON LASERS

J. D. Jarvis, H. L. Andrews, C. A. Brau, B. K. Choi, J. Davidson, W.-P. Kang, and Y.-M. Wong,
Vanderbilt University, Nashville, TN, U.S.A.

Abstract

Diamond field-emitter arrays (DFEAs) possess several advantages over photocathodes: ruggedness, no drive laser requirement, and minimal heating. A gated DFEA with micron-scale cathode-gate spacing has the added benefits of direct e-beam modulation and low operating voltages < 100 V. A second gate can be integrated, creating built-in focusing capability. We have developed two types of self-aligning gate fabrication methods. First, pyramidal molds are formed on a SOI (silicon on insulator) substrate then coated with CVD nanodiamond. The bulk layer of silicon is thinned, followed by oxide etching and opening the diamond tip isolating the gate electrode and insulating layer from the cathode. The second method uses additive physical evaporation depositions of insulating and gate electrode layers on top of the DFEAs. Chemical etching of the insulating layer separates and opens cathode tip due to "lift off" type step coverage of the evaporation technique. A 2-mask fabrication process has been used to pattern the gate to optimize active gate area and increase yield. Fabrication techniques and electrical behavior of the gated DFEAs will be discussed.

INTRODUCTION

High brightness cathodes are useful for many applications ranging from scanning electron microscopes, to electron beam driven sources. As free-electron laser technology progresses towards shorter wavelengths and higher powers, the need for cathodes producing high-brightness beams increases. Recent experiments have demonstrated the potential of diamond field-emitter arrays (DFEAs) as cathodes for free-electron lasers [1-3]. Diamond field emitters have several advantages over metallic devices. Since diamond is a covalent solid, temporal stability from clean diamond emitters is superior to that of metals. The high thermal conductivity of diamond mitigates self Joule heating which can lead to explosive vaporization of field emitters. Additionally, diamond emitters are chemically inert and perform well in poor vacuum conditions. While ungated DFEAs are a promising source of high-brightness electron beams, including a self-aligning gate on the emitter allows precise control of emission levels and low operating voltages. A second integrated gate would allow for built-in beam focusing. Two methods of producing DFEAs with self-aligned gates are presented here. The first utilizes an SOI wafer, while the second follows the so-called volcano process.

SOI PROCESS TRIODES

The SOI process triodes start with a SOI wafer, and utilizes the inverse mold process described previously [4,5]. This process differs from the ungated device procedure in that the SOI wafer contains a buried oxide layer which facilitates the creation of a self-aligned gate [6]. The process flow for the SOI process is shown in Fig. 1.

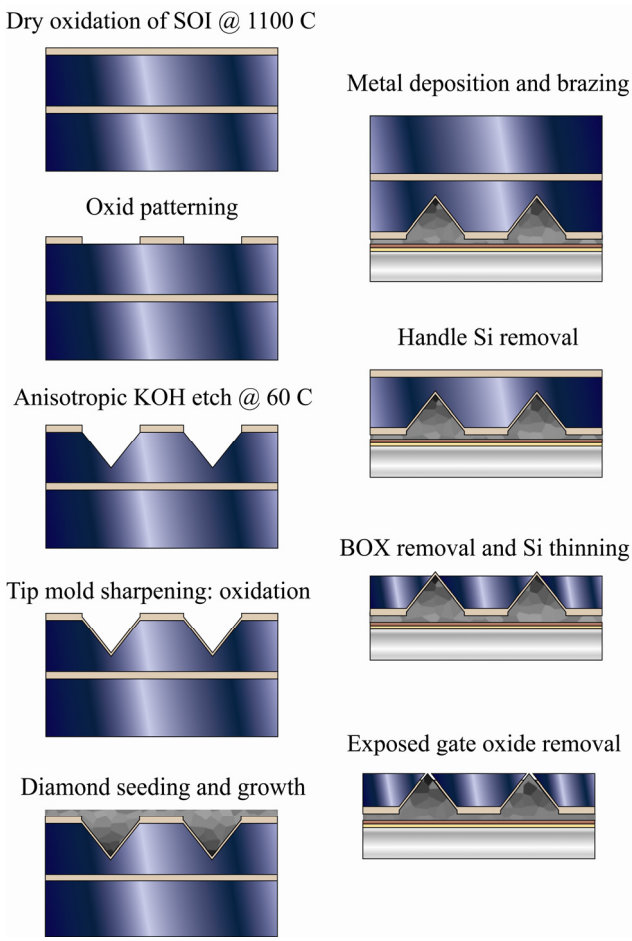

Figure 1: Process flow for the SOI triode DFEA.

The SOI wafer is patterned and pyramidal molds are produced in the surface with an anisotropic KOH etch. The molds are then oxide sharpened and conformally filled with CVD diamond. The device is then brazed to a molybdenum substrate and the handle silicon is removed down to the buried oxide layer. The oxide serves as a precision etch stop and allows the final etching of the gate silicon to be carefully controlled. After exposing the

oxide coated tips the oxide is removed, completing the device. A finished SOI gated device is shown in Fig. 2.

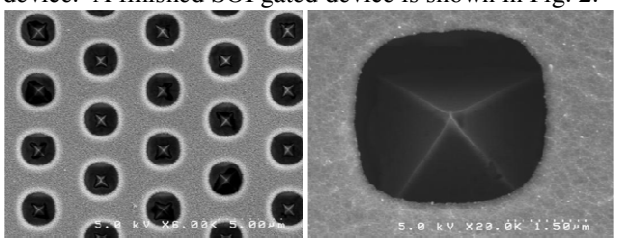

Figure 2: A finished SOI gated device and close-up detail of an emitter.

For SOI devices the tip yield and the tip-to-tip reproducibility is quite good, however issues remain with gate isolation during, and in some cases before, operation. Figure 3 shows the result of the two-mask process that is applied after the gate is completed. This final process allows the removal of excess gate material to reduce the likelihood of gate leakage and to minimize the device capacitance. After this procedure there are 16 independently addressable devices on the same 15x15 mm cathode.

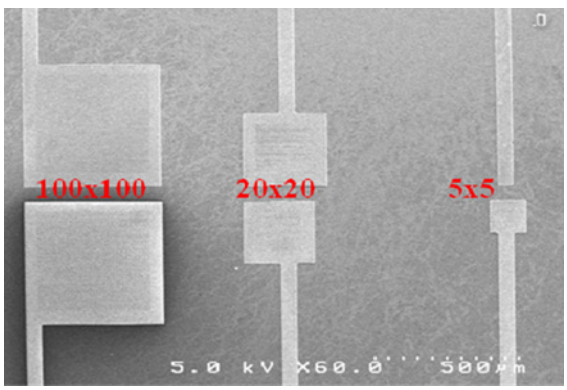

Figure 3: SOI gated device after two-mask processing.

VOLCANO PROCESS TRIODES

The volcano process can be used to add a gate to any ungated DFEA [7]. The process flow is demonstrated in Fig. 4. It begins with a sputter coating of the diamond array with SiO_2. The oxide builds up preferentially on sharp points and edges. The result is a bulbous oxide coating of the very end of the emitter. After oxide deposition a gate metal is deposited from above onto the cathode surface. The ball of oxide at the end of the emitter shields the oxide underneath it from the metal deposition. This allows a subsequent etch of the exposed oxide to remove the caps. A completed volcano device is shown in Fig. 5. From the SEM image of the volcano array it is clear that there are presently tip yield issues. The current tip yield is approximately 20%, however processes are being developed to produce conical molds rather than pyramidal ones. This will remove the bridging between the tip oxide and the pyramid edge oxide that is presently causing the low yields. Preliminary tests of volcano devices have been performed and emission current has been collected, however the gate cannot maintain its isolation under the conditions shown in Fig. 5.

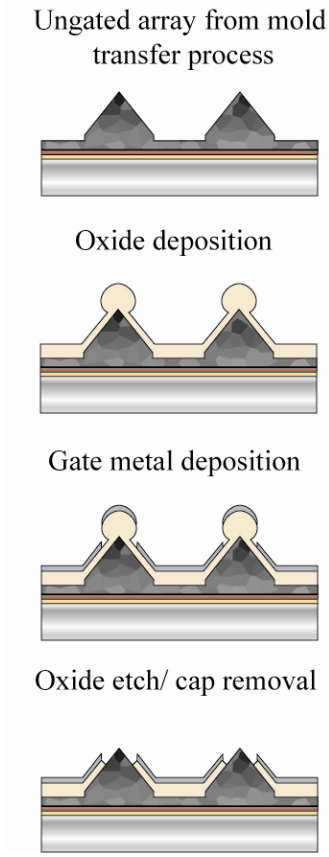

Figure 4: Volcano process flow for gate addition to ungated arrays.

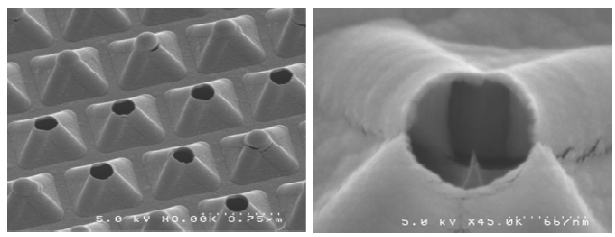

Figure 5: Completed volcano gated array with tip detail.

CONCLUSIONS AND FUTURE WORK

We have demonstrated two processes by which viable gated field emitter arrays can be produced. In the next round of testing a large electric field (~20 V/µm) will be applied between the phosphor collector and the gate electrode, this will have several benefits: the field between the gate and cathode will be much lower, thus preventing breakdown, leakage, and spurious field emission. It is also possible that a high enough external field could be used so that the potential of the gate can be negative relative to the cathode. This would enable some single-gate focusing of the emitted beamlets.

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