BUNCH ARRIVAL MONITOR AT FERMI@ELETTRA

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Abstract

The bunch arrival monitor (BAM) for the IV generation synchrotron light source FERMI@Elettra is presented. It is based on an original idea developed at FLASH/DESY, specifically designed and built in-house for FERMI@Elettra. Each BAM station consists of a front-end module, located in the machine tunnel, and of a back-end unit located in the service area. It makes use of the pulsed optical phase reference along with the stabilized fiber link. The front end converts the bunch arrival times into amplitude variations of the optical phase reference pulses distributed over the link. The analogue signal is generated at the e-beam's passage in a broadband pick-up and is sent to the modulation input of an electro-optical modulator (EOM). The back end acquires, synchronously, the amplitude modulated pulses, using a broadband photodiode and a fast analog-to-digital converter. The digitized data is sent to the machine control system for further processing. The dedicated analog-to-digital conversion, processing and communication board, part of the monitor back end, is also briefly described.

INTRODUCTION

New 4th Generation Light Sources (4GLS) currently in operation, construction or design at several National Laboratories are posing demanding requirements on the associated Timing and Synchronization (T&S) systems, identified as femto-second (fsec) T&S systems. 4GLS are typically Free Electron Lasers (FEL) driven by single pass Linear Accelerators (LINAC). Such demanding requirements on jitter ($<10\text{fsec}_{RMS}$), and drift, originate from the adopted scheme for the generation of the electron beam and the FEL radiation.

The typical bunch length ($\tau_B < 50\text{fsec}_{FWHM}$), achievable in single pass accelerators thanks to the beam longitudinal manipulation techniques, the required beam quality (6-D emittance) and the radiation generation (seeding) and exploitation (time resolved / pump-probe experiments) schemes call for an ultimate jitter of $<10\text{fsec}_{RMS}$. This ultra-low jitter value is typically required either between the electron bunch and the seed laser pulse or between the FEL pulse and the User laser pulse. To achieve this goal, the whole accelerator components need to share a Phase Reference with $<10\text{fsec}_{RMS}$ jitter and drift.

BUNCH ARRIVAL MONITOR

In 4GLS, the time position of the bunch is identified by the combination of the timing pulse (as a reference) and the slope of the electrical signal produced by the bunch passage through the pick up mounted on the beam line. This scheme was first proposed by the Desy group [1]. The pick up signal is fed to an Electro-Optical Modulator (Mach-Zehnder modulator - MZM) and modulates the optical pulses of the optical master oscillator (OMO) as a reference. The timing jitter of the bunch shifts the temporal position of the slope and thus amplitude modulates the optical pulses. Therefore the amplitude variations correlate to the timing jitter of bunches. The BAM system consists of two main parts, the front end installed in the tunnel close to the beam pick up and the back end installed in the service area for the readout of the modulated pulses and further processing.

BAM Front End

The BAM front end does the timing comparison between the reference's optical pulses and the electron bunches in the accelerator. Due to the very high resolution requirement, the BAM front end is mainly an optical system. The time comparison is done by a MZM, which converts the time difference into an amplitude difference. The modulated optical pulses from the MZM are fed to the photodiode in the BAM back end. The front end is shown in Figure 1.
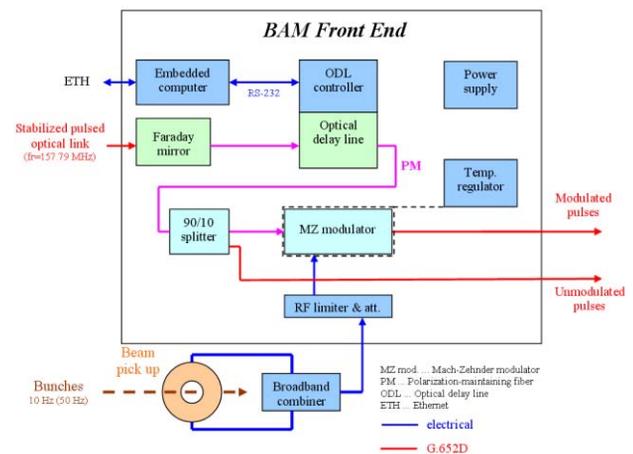
Figure 1: Block diagram of the BAM front end.

The front end has two inputs, the optical pulses from the OMO, distributed via a stabilized link, and the electrical signal from the pick up. The Faraday mirror is part of the stabilized link and needs to be close to the MZM, since short pulses provide better timing resolution. The optical delay line compensates slow drifts of the link and enables the calibration of the system at the beginning of the operation. The splitter passes 90% of the optical power to the MZM, while the 10% is left un-modulated for the ADC clock extraction at the back end. The polarization from the stabilized link needs to be controlled. Optionally, there is a need for a limiter after the pick up for the protection of the MZM's RF input. Since the MZM's transfer characteristic is temperature dependent, the MZM is temperature stabilized by a

regulated heat-pump. The delay line and some diagnostic parameters are remotely controlled via the Ethernet connection.

BAM Back End

The BAM back end is in charge of the readout and processing of the timing comparison made in the BAM front end. The modulated pulses are digitized by a dedicated analog-digital-analog (ADA) board based on the uTCA platform [2]. Beside the ADA the BAM back end includes also the signal-conditioning board (SCB) which extracts the ADC clock signal and provides a low phase-noise phase shifter. Two high-speed photodiodes are required for the opto-electrical conversion. The BAM back end is depicted in Figure 2.
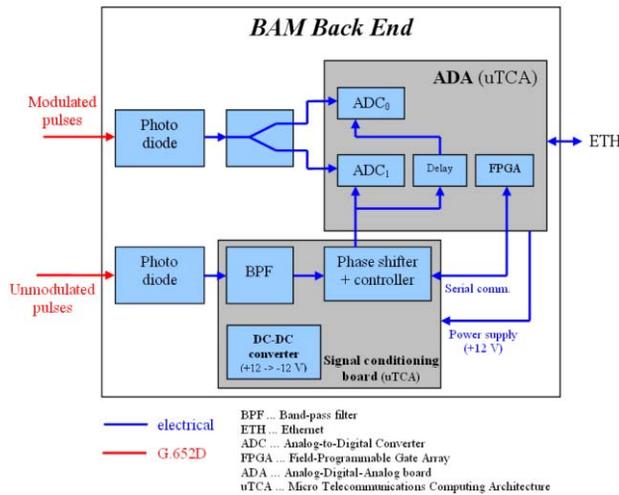
Figure 2: Block diagram of the BAM back end.

Two ADCs are used for the acquisition of the modulated optical pulses, first one for pulses and the second one for the baseline. In this way the noise present on the baseline can be used for the pulse amplitude normalization. The delay between the ADC sampling times is few hundreds of ps. The ADA is described in more detail in a later section. The low phase-noise electrically-adjustable phase shifter is based on a passive IQ modulator and features an automatic gain control for the incoming signal. It is controlled via a serial interface through the FPGA, connected to the Ethernet.

PHASE REFERENCE FOR THE BAM

The BAM stations need a phase reference signal for their operation. It is obtained from the pulsed sub-system of the FERMI optical timing system [3]. Each BAM front end in the machine tunnel has a dedicated stabilized fiber optical link. The scheme of the timing distribution and optical cabling related to the BAM diagnostic is represented in the Figure 3.

The optical master oscillator (OMO) is a soliton fiber laser working with a repetition rate of 157.790 MHz. The optical pulses are distributed to the BAM front ends by the fiber-link stabilization (FLS) units. The link receiver

(RX) is composed of an Erbium-doped fiber amplifier and a Faraday rotator mirror. The latter is integrated into the BAM front end, so the link stabilization is done as close as possible to the point where the optical pulses are effectively used. The modulated (bunch timing) and the un-modulated (OMO clock) pulses are distributed to the back end via (non-stabilized) optical fibers for the data processing (bunch-arrival time and jitter).
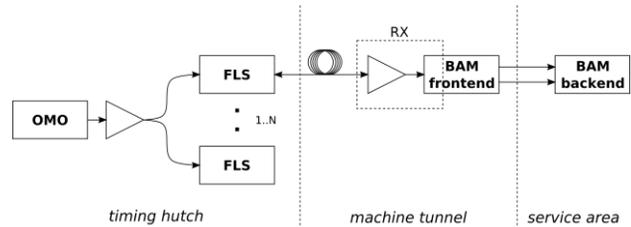
Figure 3: Optical distribution used for the BAM.

The optical pulses, used to sample the pick-up signal generated by the e-beam, are dispersion compensated and have a duration of about 200 fs FWHM at the output of the link. It is important to have short pulses at the input of the modulator but they are stretched before the input of the Mach-Zehnder Modulator because of the extra fiber path. The latter is therefore kept as short as possible.

ACQUISITION AND PROCESSING BOARD

For the BAM and other high-performance systems at FERMI@ELETTRA a dedicated data-processing platform (analog-digital-analog - ADA) has been designed [3]. It is based on the MicroTCA standard and is implemented as an Advanced Mezzanine Card (AMC). The main features of the platform are high-speed signal acquisition, generation, data processing and communication towards the control system. The architecture is based on the Xilinx Virtex-5 FPGA responsible for the data handling of all the external inputs, the processing and the interface to users. The block diagram of the ADA is shown in Figure 4.
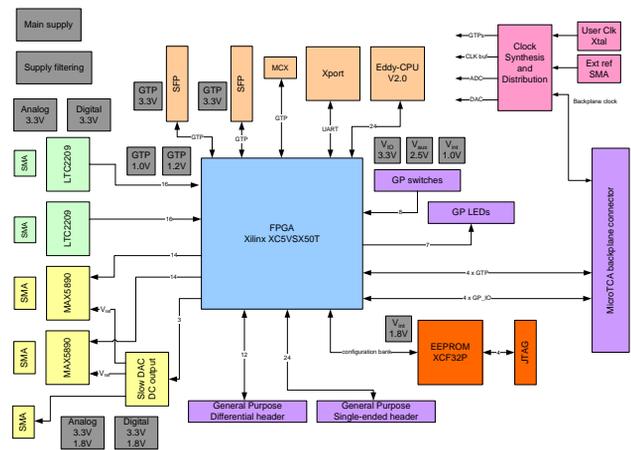
Figure 4: Data-processing platform for the BAM.

The ADA platform is divided in the following subsystems:

1. Power-supply section
2. Clock distribution: a programmable and configurable clock tree provides precise timing to on board devices with the freedom to choose between several internal or external references
3. Configuration section: the logic can be programmed choosing between direct access through an onboard JTAG chain or remotely either via the backplane or the Ethernet through the microcontroller
4. Analog inputs and outputs:
    2 LTC2209 ADC inputs, 160 Msps, 16 bits
    2 MAX5890 DAC outputs, 600 Msps, 14 bits
    1 LTC2602 slow dual DAC output, 16 bits
5. Computational core: Xilinx Virtex-5 SX50T FPGA
6. Remote access:
    Lantronix: 1 Mbps Ethernet link
    Eddy-CPU: 100 Mbps Ethernet link
    Small Form-factor Pluggable (SFP) ser-des: 1Gbps custom link
    uTCA Backplane via Gigabit Transceiver Pairs (GTPs): 4 x 1Gbps custom protocol links
    uTCA Backplane via standard IOs: 4 x 200Mbps custom protocol links
7. General purpose inputs and outputs: 24 single ended and 12 differential lines

The ADA supports various fully-configurable and programmable clock possibilities. The ADC and DAC stages can be independently driven by external clock sources through SMA inputs on the front panel. Since the BAM acquisition is critical the latter clock option is used. The ultra-low phase-noise clock is provided by the un-modulated optical pulsed link to the back end via the signal-conditioning board. In addition, the FPGA can be clocked off of the same external clock either from the DAC or ADC inputs, as well as being timed independently from one of the onboard clock sources. Alternatively the whole board can be timed by high-accuracy (tens of pico-seconds range) frequency synthesizers starting from a low frequency (14 – 37.78 MHz). The selection of the various frequencies and tree setup is accomplished by setting jumpers. The backplane and other data transfer and communication sections (e.g. Gigabit links) are timed independently having other clocking requirements.

PRELIMINARY RESULTS

The e-beam pick up, shown in Figure 5, provides an electrical signal which incorporates the bunch timing (jitter) information. The pick up is a 4-electrode open coax-line type (SMA connectors), having extremely wide bandwidth (few tens of GHz) required for the needed steep slope of the voltage-to-time conversion. Important property of the pick up is also the coupling factor between the beam and the electrodes. The latter must be optimally chosen, not to provide too high nor too low voltages at the output SMA ports. The optimal output voltage needs to

match the Mach-Zehnder modulator drive voltage (i.e. 5 Vpp).

Figure 5: BAM 4-electrode (open coax-line type) pick up.

The signal from the pick up was measured by a real-time high-bandwidth (12 GHz) oscilloscope with only 1 m of coax cable between the pick up and the oscilloscope. The signal was measured at 100 pC charge and is shown in Figure 6. The signal has a typical mono-pulse shape, with the central (the steepest) slope being used for the timing information. The slope's rise time is limited mainly by the oscilloscope's bandwidth. With further increase of the charge (to few hundred pC), suitable amplitude for the Mach-Zehnder modulator will be achieved (few Vpp).
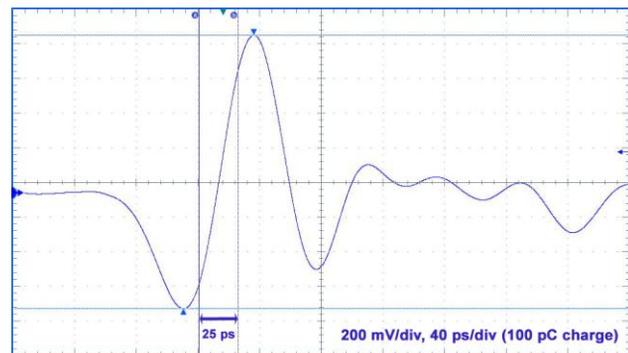
Figure 6: BAM pick-up signal measured on a 12 GHz scope.

The un-modulated optical link from the BAM front end to the back end provides the low phase-noise clock for the ADCs. The signal-conditioning board (SCB) extracts the first harmonic (157.79 MHz) and features a 360-degree electrically-adjustable phase-shift capability. The preliminary OMO-output measurement in the 10 Hz to 10 MHz integration range show about 258 fs of timing jitter. The SCB-output jitter, shown in Figure 7, is about 287 fs. The additive jitter of the SCB is therefore in the order of 130 fs. The noise between the 50 Hz and 10 kHz of the preliminary measurement is coming from the OMO (mainly due to the loose power-supply filtering), while the noise between 10 kHz and 1 MHz is generated in the SCB. With further reduction of the OMO phase noise (better power-supply filtering) the total timing jitter below

200 fs is expected which is adequate for a high-resolution acquisition of the ADCs in the back end.
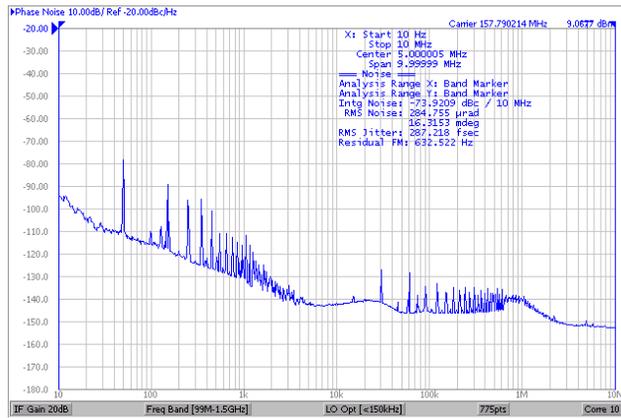
Figure 7: Preliminary phase-noise measurement of the extracted clock for the ADC.

The prototype of the BAM front end has been built. Using some commercial solutions (i.e. optical delay line, Peltier driver) and several custom-made electrical circuits a fully-functional and remotely-controlled standalone unit was assembled. The aluminium box is 250 x 250 x 100 mm in size and includes all blocks shown in Figure 1. It features a temperature-stabilized chamber for the Mach-Zehnder modulator, an embedded computer for the remote control via Ethernet, a diagnostic board for several important parameter readout, a 560 ps optical delay line with controller and some additional circuits. The BAM prototype box (with the Faraday-mirror module removed) is shown in Figure 8.
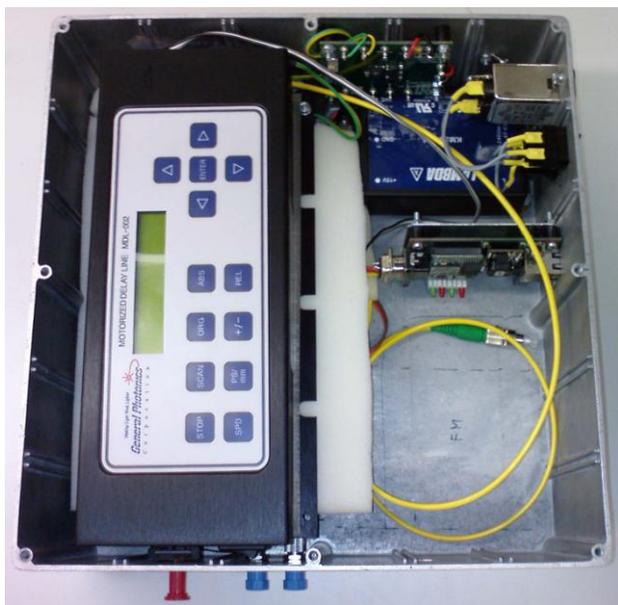
Figure 8: BAM front-end prototype. The Faraday-mirror module of the stabilized link is not installed in the box (lower right area).

The preliminary measurements of the complete BAM system (front end and back end) without the beam have been carried out. Assessment of the optical and electrical power levels throughout the system has been made. The most critical are the optimal Mach-Zehnder RF drive level and the optical power levels at the two photodiodes in the back end. The amplitude noise of the OMO pulses has been evaluated with real-time measurements using the ADA acquisition board. The amplitude RMS noise measured was 0.37 %, which seems a little bit too high, but the input power and voltage levels of various devices and components were not optimally set at this point.

FUTURE WORK

An integration of the complete system (front end and back end) is planned in June/July 2010. The first bunch timing jitter measurements will be performed. The prototype units will be used at first, but will be later replaced with the (first) industrially-manufactured series. The final BAM system with the complete integration into the FERMI@Elettra control system will be done in autumn.

CONCLUSION

The bunch-arrival-time monitor developments have been described. Up to now working front end and back end prototype units have been manufactured and tested. The measurements of the pick-up signal show a slope of about 50 mV/ps (at 100 pC charge), which is limited by the measurement equipment. Normally, the machine will operate at several hundreds of pC charge, so the slope will be appropriately steeper. Although the first acquisition measurements show relatively large OMO's amplitude noise, optimization of levels throughout the system will greatly improve the readout resolution.

ACKNOWLEDGMENT

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