A New Approach in Simulating RF Linacs Using a General, Linear Real–Time Signal Processor*

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Abstract

Strict requirements on the tolerances of the amplitude and phase of the radio frequency (RF) cavity field are necessary to advance the field of accelerator technology. Due to these stringent requirements upon modern accelerators, a new approach of modeling and simulating is essential in developing and understanding their characteristics. This paper describes the implementation of a general, linear model of an RF cavity which is used to develop a real–time signal processor. This device fully emulates the response of an RF cavity upon receiving characteristic parameters (Q_0, ω_0, $\Delta\omega$, R_S, Z_0).

Simulating an RF cavity with a real–time signal processor is beneficial to an accelerator designer because the device allows one to answer fundamental questions on the response of the cavity to a particular stimulus without operating the accelerator. In particular, the complex interactions between the RF power and the control systems, the beam and cavity fields can simply be observed in a real–time domain. The signal processor can also be used upon initialization of the accelerator as a diagnostic device and as a dummy load for determining the closed–loop error of the control system. In essence, the signal processor is capable of providing information that allows an operator to determine whether the control systems and peripheral devices are operating properly without going through the tedious procedure of running the beam through a cavity.

I. INTRODUCTION

Utilizing a baseband complex envelope analogy of an RF cavity system [1–3], a hardware realization (i.e., real–time signal processor) is developed. This processor has the ability to simulate the effect of cavity detuning, beam loading and finite Q. A brief overview of the relevant theory is presented. This paper focuses on the implementation of a theoretical model to create a real–time signal processor and concludes with a direct comparison of the results from the mathematical simulations and the hardware simulations.

II. MATHEMATICAL REALIZATION OF AN RF CAVITY

This section outlines the procedure used to develop a model for an RF cavity which implements the complex envelope isomorphism, initially developed in reference [1]. This approach of modeling a RF cavity deviates from the standard approach of using amplitude and phase analysis by encoding the relevant information into two linear, general low–pass functions: in–phase (I) and quadrature (Q). In essence, the complex envelope analogy reduces a band–pass system into low–pass functions [2].

*Work supported and funded by the United States Department of Defense, Army Strategic Defense Command, under the auspices of the United States Department of Energy.

0-7803-0135-8/91$01.00 ©IEEE

A single–mode resonant cavity system is composed of four components (see figure 1): an RF source, a transport component, an RF cavity and a beam loading component.

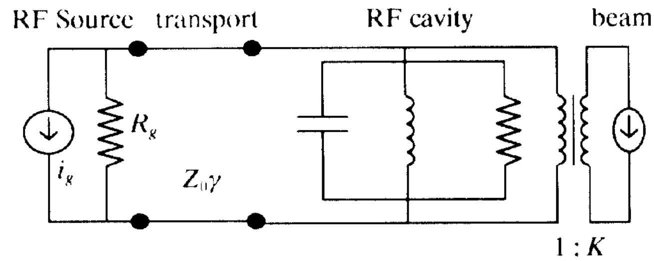


Figure 1. Simplified equivalent circuit of an RF cavity system.

Applying fundamental principles of circuit theory to figure 1, a set of characteristic equations that describe the microwave junctions of the RF cavity system (i.e., forward voltage and reflected voltage) are derived and are graphically illustrated in figure 2. The resonant cavity system block diagram also describes the effects of beam coupling and input coupling. Note that all of the inputs and outputs consist of an in–phase and a quadrature component; hence, the block diagram is more complex than illustrated in figure 2.

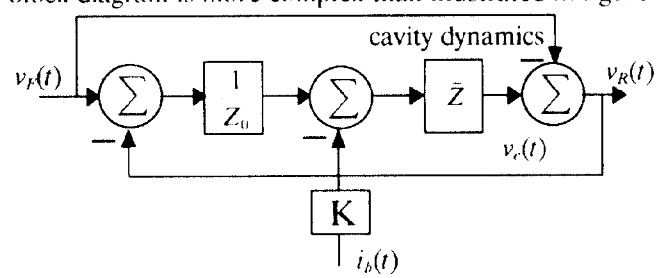
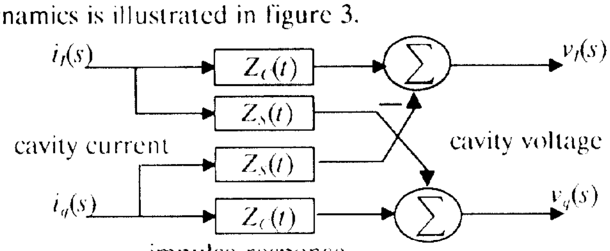


Figure 2. Block diagram of an RF cavity system.

The cavity dynamics are the mathematical realization of the complex convolution integral between a narrow–band RF signal and an RF cavity realized as a bandpass device [3]. From the principles of convolution, a block diagram of cavity dynamics is illustrated in figure 3.



$i_I(t) \equiv$ in–phase component of cavity current

$i_q(t) \equiv$ quadrature component of cavity current

$v_I(t) \equiv$ in–phase component of cavity voltage

$v_q(t) \equiv$ quadrature component of cavity voltage

Figure 3. Butterfly realization of the baseband complex envelope model.

The impulse transimpedance response with ω_0 detuned from the drive frequency is defined in equation (1).

$$Z_C(t) = \frac{R_S}{\tau}\left[e^{-\frac{t}{\tau}}\right]\left(\cos\Delta\omega t - \frac{1}{2Q_0}\sin\Delta\omega t\right)$$

$$Z_S(t) = \frac{R_S}{\tau}\left[e^{-\frac{t}{\tau}}\right]\left(\sin\Delta\omega t + \frac{1}{2Q_0}\cos\Delta\omega t\right) \tag{1}$$

where,

$\tau \equiv$ cavity damping time constant (sec)

$R_S \equiv$ cavity shunt resistance (ohms)

$Q_0 \equiv$ cavity unloaded quality factor

$\Delta\omega = \omega_0 - \omega_d \equiv$ cavity detuning frequency (rad/sec)

$\omega_d \equiv$ cavity drive frequency (rad/sec)

$\omega_0 \equiv$ cavity resonant frequency (rad/sec).

The impulse transimpedance response in the Laplace domain is

$$Z_C(s) = \left[\frac{R}{\tau}\right]\left[\frac{s + a_C}{s^2 + b_1 s + b_2}\right]$$

and

$$Z_S(s) = \left[\frac{R}{2\tau Q_0}\right]\left[\frac{s + a_S}{s^2 + b_1 s + b_2}\right] \tag{2}$$

where,

$$a_S = \left(\frac{1}{\tau} + 2\Delta\omega Q_0\right) \qquad b_1 = \left(\frac{2}{\tau}\right)$$

$$a_C = \left(\frac{1}{\tau} - \frac{\Delta\omega}{2Q_0}\right) \qquad b_2 = \left(\frac{1}{\tau^2} + \Delta\omega^2\right).$$

The complex baseband cavity model requires that the input signals are linear, time-invariant equations and the existence of their Laplace transforms. Thus, the model can accurately simulate the effects of cavity detuning and finite Q without being limited to a small signal regime.

III. DESIGN OF A REAL-TIME SIGNAL PROCESSOR

A. Implementing the Cavity Model

Implementation of the resonant cavity model is obtained through the use of control theory. Control theory provides a practical realization of the model from a set of equations that describe the response of a system.

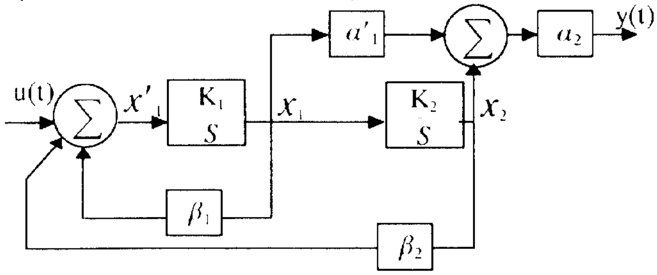


Figure 4. Block diagram of a modified controllable cononical realization.

From basic principles in control theory, equation (2) is realized in a modified controllable cononical form (see figure 4). The transfer function of figure 4 is

$$H(s) = \frac{y(s)}{u(s)} = \frac{\alpha'_1\alpha_2 K_1 s + \alpha_2 K_1 K_2}{s^2 + \beta_1 K_1 s + \beta_2 K_1 K_2}\ . \tag{3}$$

The primary reason for using a modified controllable cononical realization is to utilize the zero offset adjustment circuitry which exists with the multiplication circuitry (i.e., α's and β's coefficients). Zero offset adjustment circuitry is needed because of the inherent offset problem associated with transimpedance amplifiers. Another advantage of implementing a modified controllable cononical realization is to increase the bandwidth of the realization by having a gain coefficient (i.e., K_1 and K_2) associated with each integrator (i.e., s^{-1}).

Note that this realization only represents one transfer function (i.e., $Z_C(s)$ or $Z_S(s)$). Thus, four realizations are needed to create the baseband complex envelope model in figure 3. The controllable cononical form provides the foundation for the hardware realization (i.e., the real-time signal processor).

B. Circuit Description of the Real-time Signal Processor

The packaging format for the real-time signal processor utilizes the VXIbus standard [4]. The specific benefits of conforming to the VXIbus architecture include a concise, standardized, modular format with the accessibility of a parallel processing bus, broadband analog bus, precision clocks and integrated power supplies with a cooling system as standard features of the system architecture. The real-time signal processor is limited to a single-wide module illustrated in figure 5.

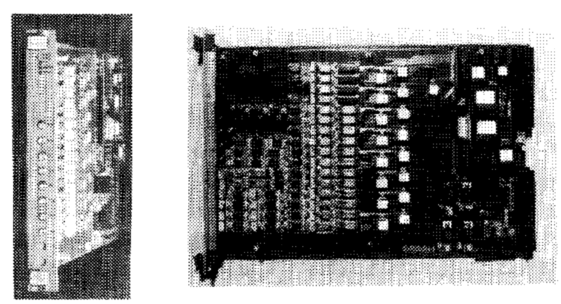


Figure 5. Single-wide real-time signal processor VXI module.

A modular circuit layout minimizes the amount of drafting such that, the VXI processor interface circuitry is created on a separate daughter board with the dimensions of two inches by five inches. The real-time signal processor circuitry is constructed on an eight layer mother board. The layout of the circuitry is in five distinct parts: VXI processor interface, signal conditioning circuitry, digital registers, the multiplying digital to analog circuitry and the analog circuitry. The interface circuitry uses Erasable Programmable Logic Devices (EPLDs) that provide the addressing, timing, data acquisitioning, status and control of the real-time signal processor. Digital multiplication coefficients are down-loaded into separate registers by implementing EPLDs. This allows the ability to remotely control the poles and the zeros of the realization. For example, the data from the output registers of the EPLDs are the digital inputs for the digital-analog (D/A) multipliers which corresponds to the α and β coefficients shown in figure 4. The analog circuitry consists of the summers (i.e., Σ) and the integrators (i.e., s^{-1}).

IV. RESULTS

In the previous sections, a mathematical realization and a practical realization (i.e., real-time signal processor) of a resonant cavity system were developed. This section illustrates the simulations of both the mathematical realization and the hardware realization in a manner which allows direct comparison of the results.

Numerical simulations of the model were achieved by using a control system software package, MATRIX$_X$. The following results simulate an RF cavity with the following assumptions: $Q = 10k$, $R_s = 50\Omega$, $\omega_d = 425MHz$ and $\omega_0 = 425.04MHz$.

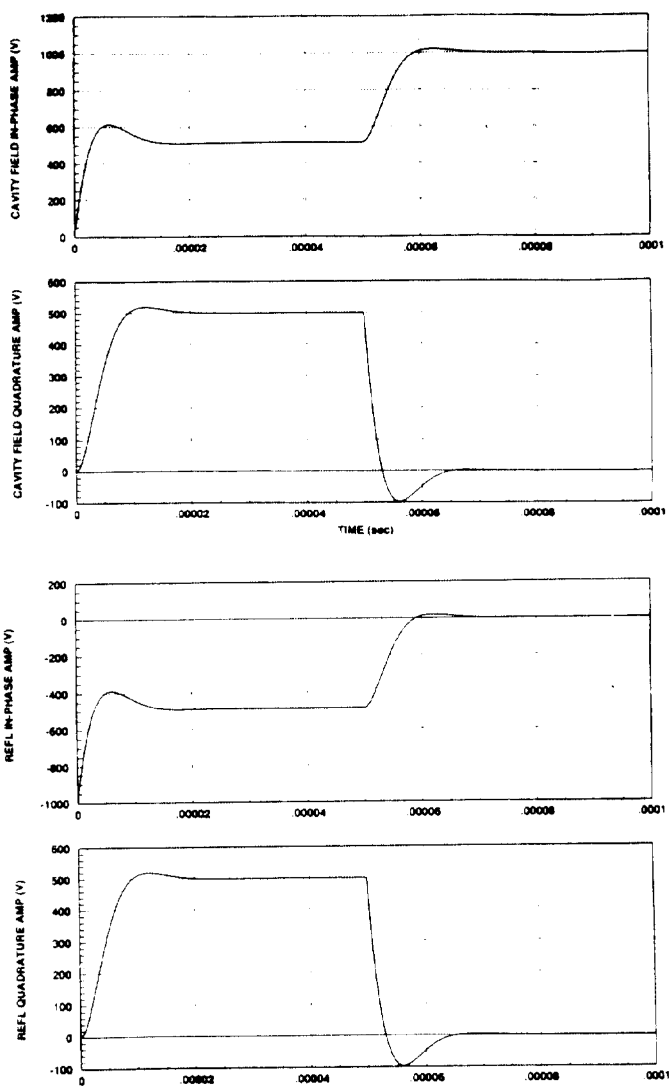


Figure 6. Computer simulations of a cavity operating off resonance with the effects of a beam

The hardware simulations were achieved by loading the appropriate coefficients into the multiplying D/As and simulating the inputs with function generators. The results of the hardware simulations are illustrated in figure 7.

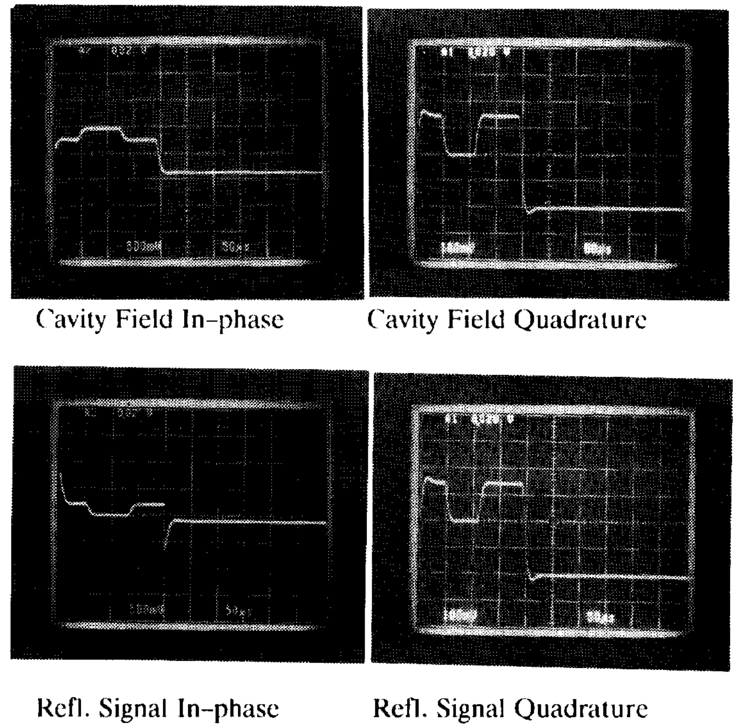


Figure 7. Hardware simulations of a cavity operating off resonance with the effects of a beam

V. CONCLUSION

The development of a real-time signal processor to simulate a resonant cavity system which included the effects of beam coupling and input coupling was successful. The results clearly illustrate that there are direct similarities between computer generated responses and hardware generated responses. This accomplishes a primary goal; however, further analysis needs to be proformed that will provide data on the comparison between the response of an actual accelerator and the response of the real-time signal processor.

VI. ACKNOWLEDGMENTS

The authors wish to extend their appreciation to B. Cheo, P. Denney, E. Natter, A. Regan and C. Ziomek for their discussions of topics contained in this paper. Also, I. Debaca and S. Scarlott are recognized for their technical support.

VII. REFERENCES

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