MULTI-PROCESSOR CONTROL OF THE 100 KeV McMASTER MARK IV SPUTTER ION SOURCE*

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Abstract

An ion source control system has been developed to provide 100 KeV heavy ion injection into the McMaster FN Tandem. The control system is composed of a CMOS RCA1802 microprocessor at deck potential which conveys power supply command/status data from/to a PDP-11/23 via fibre optic link. Approximately 50 fail safe interlock conditions are maintained by the PDP with capabilities to shut down affected power supplies if interlock states warrant. There are commands that allow operator intervention to set supply voltages, source cone position, and interlock bypass. Power supply set point voltages are either maintained to within modifiable regulation windows, or set to track manually controllable shaft encoders. The ion source status is provided to the operator from the PDP via a DEC VT220 monochrome display terminal and printer. There are two possible display modes, both with variable updates rates; one involving power supply voltage/current information and interlock status, and one indicating abnormal stati caused by cascading failed interlocks. An additional serial line on the PDP-11/23 allows user communications, including a "screen dump" of any of the displays, to a remote location through the use of a 1200 baud modem.

Introduction

A computer controlled ion injection source system for McMaster University's tandem accelerator has been developed. The control system is now complete[1] with ion source construction well underway. Within the Accelerator Laboratory, there are already in use several ion sources including sputter, tritium and polarized. The latter source being operated at 50 KV deck potential by manual operator control with lucite rod isolation. The new ion injection source system has been developed with computer control. Operator commands can now be given from the control room on a PDP-11 terminal keyboard. They are then implemented by a microprocessor at ion source deck potential. In planning this system, the following design goals were formulated:

1. Short (2 character keystrokes) but descriptive commands needed for operator control;
2. Computer controlled interlocks to avoid improper operator action and to minimize damage due to component failure;
3. Several display modes to convey source operation and interlock status;
4. The provision of more conventional control knobs in order to continuously vary selected power supply parameters for beam optimization (steering);
5. The inclusion of power supply regulation duties for the control computer;
6. The possibility of remote location communication.

Hardware Description

The design of the hardware system, normally susceptible to larger static voltage discharges, pays particular attention to robustness through the suitable utilization of isolation devices and, on the deck, a CMOS microprocessor with high noise immunity[2] as shown in Figure 1. The detection of 21 analogue signals including power supply currents and voltages, temperatures and vacuum pressures, is accomplished through isolation amplifiers. The 32 digital signal sensors or inputs and the 43 control outputs are buffered between microprocessor and device by optical isolators.
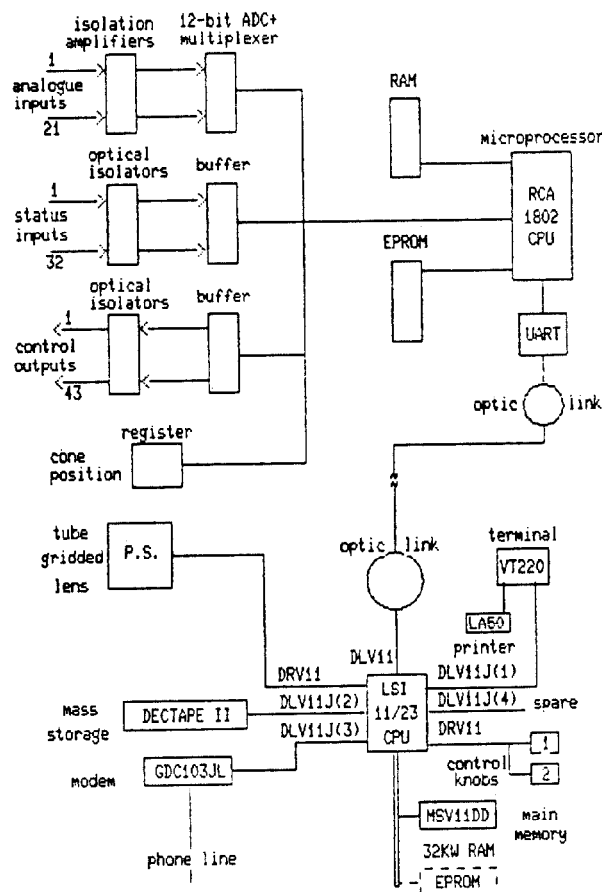

FIGURE 1. Ion Source Control System

Figures 2(a) and (b) show device parameters displayed and interlocks controlled while Table One lists controlled power supplies and the ADC conversion gain being used for monitoring. All power supplies were modified to operate from motor driven variacs. Some supplies also allow fine or vernier control as well as coarse voltage control. The up/down link between the I/O processor at deck potential and the PDP-11/23 at ground potential uses a fibre optic serial line.

The PDP-11/23, initially a LSI-11/2 CPU which proved too slow to regulate power supplies without oscillation (hunting), utilizes four serial lines and two parallel interfaces. As illustrated in Figure 1, the fibre optic link to the RCA1802 is on a separate interface. For reasons outlined in the next section, it is necessary to give priority to the communiction with the RCA1802 over terminal I/O operations by certain positioning of these devices on the PDP-11 backplane. (The four serial line unit (DLV11-J) does not allow internal selectable interrupt priority). The user control knobs utilize shaft angle encoders whose digitized results are placed in one parallel line unit

(DRV11) register for read only operation. The other parallel line unit serves as a read/write register for the tube gridded lens power supply, at ground potential, which has an internal regulation and voltage settable system.

Table One

ION SOURCE POWER SUPPLY COMPLEMENT

Source Power Supply Systems	ADC Reading Resolution
Cs. Boiler (0 to 50Vac)	Voltage - 8 bits
	Current - 8 bits
Ionizer Current (0 to 10Vac)	Voltage - 8 bits
	Current - 8 bits
Suppressor (0 to -3kVdc)	Voltage - 8 bits
	Current - 8 bits
Extraction (0 to -32kVdc)	Voltage - 10bits
	Current - 8 bits
Cs Einzel Lens (0 to -32Vdc)	Voltage - 10bits
	Current - 8 bits
Ground Bias (0 to 5kVdc)	Voltage - 8 bits
	Current - 8 bits
Source Gridded Lens 90 to -10kVdc)	Voltage - 8 bits
	Current - 8 bits
Steerers, X and Y (-1kV to +1kV dc)	Voltage - 8 bits
	Current - 8 bits

and at ground potential:

Deck (0 to -100kVdc)	not connected
Tube Gridded Lens (0 to -32 kVdc)	Commercial internal system

Software Considerations

Program development for both the RCA1802 deck microprocessor and the LSI-11/23 ground potential processor was done on a TSX+ multi-user[3] PDP-11/23. For the RCA1802, a cross assembler was utilized and since the duties of the deck processor were relatively straight forward, object code output was implemented directly into EPROM. The tasks for the control program include interrupt driven input (from the LSI-11/23) and an ASCII dump of ADC 12-bit conversion data (25 microsecond successive approximation type[4]) from the various analog signals with digital binary data for device stati. As simple as the RCA1802 code is, the LSI-11 code proved to be far more complex.

One of the prime considerations in the PDP-11 control program development is speedy and efficient performance. Without this, power supply regulation duties could not adequately be carried out in addition to other tasks such as interlock monitor and control, and terminal display updates and communications with the deck microprocessor (RCA1802). About 90% of programming was done in the MACRO assembly language[5]. A higher level language[6], FORTRAN 77, was utilized for floating point calculations (converting ADC units to voltages, currents and pressures, etc.) and formatted display output subroutines once the screen cursor was correctly positioned. For program development purposes, the program was edited, compiled and linked on the DEC PDP-11/23 multi-user RT11 Operating System, copied to TU58 tapes and transported to the site PDP-11, running RT11 foreground/ background system with DECTAPE II. Although slow to load (2.50 minutes), the program was much more easily modified than would be the case with an EPROM committed program. The code was so structured, however, so as to be amenable to EPROM operation with a small RAM requirement.

Early on, it became apparent that the display screens, using direct cursor addressing, required half of the processing time in the PDP-11. The regeneration of the RT11 operating system incoparating high speed ring buffers and terminal handlers reduced this task to under a quarter of total time requirements. Although

all input/output was handled with suitably prioritized interrupt completion routines, the hardware priority in serial line operation still had to be given to communications with the deck control processor. This necessitated a dedicated serial line for the RCA1802 as shown in Figure 1. Two displays were developed, one to indicate operating parameters (see Figure 2(a)) and one to detail interlock configurations (see Figure 2(b)). In both cases, only changed information is written to the screen unless a new display is selected which requires a complete screen rewrite.

```
<PF2> 3                                              01-FEB-85 15:31:53
CONTROL FUNCTION:  STATUS( ) REGULATE(□) CONTROL( )->#1(□)#2(□)
                   GROUND BIAS
CODE POWER SUPPLY  STS  VOLTAGE  CURRENT(mA)   CODE  INTERLOCK    STS
  0  EXTRACTION    OFF   -782      0.59         16  CONE COOLING  OK
  1  EINZL LENS    ON    -594      0.15         17  BODY COOLING  OK
  2  SRC GRID LNS  ON    -235      0.11         18  SUPRSR COOLG  BAD
  3  GROUND BIAS   ON     784      0.0          19  QUICK COOL    ON
  4  ION CURRENT   OFF    0.24     0.9          20  PENNING PRES  OK
  5  CS BOILER     OFF    1.2       31          21  T.C.#1        OK
  6  SUPPRESSOR    ON    -270      0.20         22  T.C.#2        OK
                        X(volt)  Y(volt)        23  T.C.#3        OK
  7  STEERERS      ON    -3.5     -1.2          24  T.C.#4        OK
  8  T. GRID LNS   ON      0       0.00         25  VALVE#1       CLOSE
                        VAC.PRESS.(Torr)        26  VALVE#2       OPEN
 10  PENNING CGE   ON     125                   27  VALVE#3       ?
                        (degree C)              28  VALVE#4       OPEN
 11  BOILER TEMP.         15                    29  VALVE#5       ?
                        POSITION "              30  DIFF. PUMP    OFF
 12  CONE GAS CTL         9.4                   31  ^ FLOW & TEMP OK
                        PSH (thou ")            33  RUFF PUMP     ON
 13  CONE POSITION        987                   34  TI-BALL PUMP  OFF
                                                35  SPRSR 0 START OFF
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FIGURE 2(a). Screen dump of the terminal main display.

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<PF1> 4                                                01-FEB-85 15:39:44
                              INTERLOCKS

NO. DEVICE    STS # INTERLOC STS ENABL I NO. DEVICE   STS # INTERLOC STS ENABL
 0 EXTRN PS   OFF 0 PNG VAC  OK  YES   I 11 QUICK CL  ON  0 SUP<500V  OK  YES
                1 CONE CL    OK  YES   I 12 VALVE #2  OFF 0 T.C. #3   BAD YES
                2 BODY CL    OK  YES   I                 1 T.C. #4   OK  YES
                3 VALVE #2   BAD YES   I 13 VALVE #3  OFF 0 T.C. #2   OK  YES
 1 EINZL LN   ON  0 PNG VAC  OK  YES   I                 1 T.C. #3   BAD YES
 2 S GRD LN   ON  0 PNG VAC  OK  YES   I 14 VALVE #4  OFF 0 T.C. #1   OK  NO
 3 GRND BI    ON  0 PNG VAC  OK  YES   I                 1 T.C. #1   BAD YES
 4 IONIZER    OFF 0 CONE CL  OK  YES   I 15 DIFF PMP  OFF 0 T.C. #2   OK  YES
                1 BODY CL    OK  YES   I                 1 DIFF FLO  OK  YES
                2 SUP>500V   BAD YES   I                 2 DIFF TMP  OK  YES
 5 CS BOILR   OFF 0 QUICK CL BAD YES   I                 3 RUFF PMP  OK  YES
 6 SUPPRESS   ON  0 PNG VAC  OK  YES   I 16 TI-B PMP  OFF 0 T.C. #1   OK  NO
 7 STEERERS   ON  0 PNG VAC  OK  YES   I
10 PNG GAGE   OFF 0 T.C. #3  BAD YES   I
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FIGURE 2(b). Screen dump of the terminal interlock display.

The RCA1802 deck processor, and the PDP-11/23 main processor, intercommunicate via ASCII strings. In order to operate with low timing overhead, only minimal handshaking or error retries are performed. Errors detected include receiver hardware checks involving parity, framing and overrun conditions. As explained below only one type of retry is done. Upon command, the RCA1802 reports the status of the source devices via a 30 byte packet. If the PDP-11 verifies that it has successfully received 30 bytes, processing begins, otherwise a "report" command is reissued from the PDP-11 to the RCA1802. When a control request, such as "extraction voltage up", is necessary, the PDP-11 sends the device code (the RCA1802 memory-mapped location for that device register) and the appropriate control bit pattern for the device command and status register. If the RCA1802 detects a receiver error, no action on the PDP-11 request is taken. The PDP-11 will reissue the request as part of the duties of the next processing loop operation.

One of the more time critical tasks for this system, is the regulation to better than 3 percent of power supply voltages. Some supplies require better regulation than others, so that the PDP-11 program allows user variable regulation "windows" or trigger levels. Beyond these floor and ceiling values, a voltage cannot stray without the PDP-11 issuing a command to the RCA1802 to lower or raise the voltage as required. Another advantage to programmable regulation is the ability to minimize voltage hunting which varies from supply to supply depending on variac motor speed, fine or coarse level control, or differing noise levels on the feedback lines.

Another important duty of the PDP-11 is to perform logic tests to determine if component failures are present and to take corrective action by closing values, or power supply shutdown. If a situation warrants, any interlock may be 'bypassed' or made 'active' via operator command. In bypass mode, abnormal conditions are marked on the main display via reverse video writing while, in active mode, flashing reverse video is utilized, designated supplies are deactiviated and bells ring when an abnormal condition is detected.

The lowest priority task of the PDP-11 system is to process user keyboard input. Commands include the ability to turn supplies ON or OFF, set voltage levels, both by user input value or by control knob attachment and rotation, change valve positions, change interlock conditions and select displays. These operations are accomplished by 2 character keystrokes, the first being a special function key and the latter being a numeric device code as shown on the display. If special function key n (PFn) is not depressed, then the ASCII string which follows for up to 80 characters is simply reproduced on the command line for logging purposes during remote screen dumps or printer outputs. Table Two summarizes the user input commands. When any command is successfully completed, the display will reflect some change.

Table Two

USER INPUT COMMANDS

Special Function Keys	Operation Performed
(PF1) code STATUS	Change status or device "code" to "status"
(PF2) code VOLTS	Change present voltage for device "code" to "volts"
(PF3) code 1 or 2	Connect device "code" to a control knob number "1 or 2"
(PF4)	Change to interlock display
^T(cntrl T)	Enable remote communication(Talk) mode
^E(cntrl E)	Exit remote communication mode
^D(cntrl D)	Perform screen dump in ASCII string form to remote location.

For example, Figure 2(a) shows an asterisk at the left of device 3 which has been preset to a regulation voltage (note the asterisk in the regulate column at line 2) via the command (PF2). It also shows an interlock violation -- the Quick Cool which affects three power supplies: Ionizer current, Cs Boiler, and suppressor, all flagged in reverse video as well. If the quick cool interlock is active (enabled) as shown in Figure 2(b) then this reverse video on the main display would be flashing, bells would be ringing, and the three affected power supplies would be shutdown via computer command. If the interlock was bypassed (not enabled) then no bells or supply shutdowns, only steady reverse video would be present. If a user keystroke is in error, then a "?" appears in place of the user echoed characters which indicate no operation was performed.

A special mode, invoked by the CNTRL T simultaneous keypress, allows input/output to be performed using one of the PDP-11 serial lines. This includes a screen dump of either of the two possible displays which is sent sequentially as 24 lines of 80 characters each. When connected to a modem, an "on-call" technician with any dumb terminal can type to the last line on the screen with up to 80 characters. Any user keyboard input in this mode is echoed on the top line of the screen as well as sent as output through the modem to the remote terminal. When ready, a CNTRL D keypress sends the currently displayed screen contents to the remote terminal for evaluation. The CNTRL E command

will exit the talk communication mode. Note that under this mode, all control operations are unaffected being performed with a higher priority.

Control System Operation

A full test of all supplies and switch simulated interlock failures has resulted in the following performance figures. The DEC VT220 terminal, operating at 9.6K baud performs a complete screen rewrite in under one second. Screen updates, performed at every 10 processing loop passes, occur at better than every second of elapsed time. Under full load, constituted by all supplies regulating at preset voltages and the system in remote talk mode, the processing loop requires about 20 percent increase in time for completion, that is, moving from 50 milliseconds to 60 milliseconds. Supplies can be regulated to within 0.5 percent. This compares favourably with the regulation obtained in the tube gridded lens supply which contains internal regulation electronics. Use was initially made of a slower main processor, the LSI-11/2 CPU which revealed that regulation could not be obtained to better than 2% without severe hunting effects. The PDP-11/23 control program currently occupies 14K 16-bit words out of a possible 28K words, leaving 14K words for expansion.

Conclusions

The computer control systems developed at McMaster for the Heavy Ion Injection Source has performed adequately in power supply control, interlock monitoring, and providing a palatable user command and status interface. "Luxury facilities" such as hardcopy logging output and remote location communication are implemented without undue effect on program performance. The modular construction of the program allows ready inclusion of more devices and interlocks. Program size is one-half of total memory available, allowing much free space for expansion of the program with additional devices and features.

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