The CEA colliding beam project requires trigger signals relative to the e and e' circuitry to clock beam positions in the accelerator. These triggers are required for proper timing of multicycle injection, steering of the beam into the bypass, triggering of beam monitoring and excitation devices. The synchronizer was built to provide these triggers.

Introduction:

The required timing information is derived by dividing the RF accelerating frequency (475 MHz) by the harmonic number. The normal harmonic number for the CEA is 360, but when the beam is switched to circulate through the bypass the harmonic number becomes 364 due to the increased beam orbit path length. The switching of the division ratio from 360 to 364 is triggered by the ultraflectors which steer the beam into the bypass.

The 475 MHz RF accelerating frequency is divided by 360 in ratios of 2, 9, 5 & 4. The output of the divide by five stage provides a two phase 5.2 MHz clock. This is used to clock a two phase, eight stage shift register, and the output of the divide by four (1.3 MHz) is fed to the SET input of the first stage of the shift register; this generates an eight phase clock at 1.3 MHz (475/160) i.e., the output of each stage differs in time from the preceding stage by 1/8 of the 1.3 MHz period. By selection of one of the eight clock pulses and use of a 100 nanosecond variable delay line, a trigger adjustable over the orbital period is generated. To divide by 364 when the beam circulates through the bypass the equivalent of four cycles of the 475 MHz input are gated off for each 1.3 MHz output pulse.

Synchronizer:

The 475 MHz input is too high a frequency to use with presently available integrated circuit logic. So a snap recovery diode (SRD) divider is used for the input divide by two stage. Figure 1. This stage works as a subharmonic oscillator powered by and phase locked to the input drive signal. The divider has a six db conversion loss and can drive the following MECL III, logic stage in the two cycle gate directly with RF input power ranging from 25 to 250 milliwatts. The device has a bandwidth of over 20% using fixed lengths of coax line for resonant circuits. This large bandwidth eliminates the need for any tuning adjustments. The output of the SRD divider drives a MECL gate (M1A) used as a buffer. This buffer then drives a MECL flip flop, F1, and a delay circuit consisting of three cascaded MECL gates (M2A, B & C). The output of F1 clocks a two stage shift register consisting of F2 and F3, the outputs of which are AND'ed together by M1B. When the 1.3 MHz input to the D input of F2 goes true the next pulse from F1 sets F2's Q output true; making M1B's output false. While M1B's output is false, M2D does not pass any pulses from the delay circuit to the input of the divider by nine stage. The next pulse from F2 causes F3's Q output to go false making M1B's output true again. This pulse from M1B is exactly two cycles wide (at 237 MHz or four cycles wide at 475 MHz) and is synchronized to the 237 MHz pulse train. When the 1.3 MHz input to F2 goes false, the output of F2 goes false before F3's output goes true. This keeps M1B's output true and no gate pulse is generated by the trailing edge of the 1.3 MHz pulse. The above assumes that the inhibit input level is true. If it is false (beam not in bypass) M1B's output will always be false. This gating of the pulse train to the dividers requires four extra input pulses to complete a division cycle by the divider. Therefore, effectively increasing the division ratio by four to 364.

The delay circuit, M2A, B & C, is used to compensate for variations in delay through the two cycle gate versus supply voltage and temperature.

The divide by nine, five and four were also made with MECL logic flip-flops and gates. They are synchronous type dividers to minimize the delay thru the divider chain.

One of the eight outputs of the shift register is selected by an eight input multiplexer. The selected output is used to "clock" a three stage shift register (Figure 1) used as a pulse synchronizer. This circuit is essentially the same as the one used in the two cycle gate except for the input flip-flop which is used to prevent jitter should the input pulse occur at the same time as the "clock" pulse. By this method random triggers can be synchronized to the beam orbital position for use in timing devices which require precise timing relative to the beam. The pulse synchronizer is wired so that only one output pulse is generated by the leading edge of each random input pulse.

If the synchronized trigger must occur between the available eight steps, a 100 nanosecond variable delay line is inserted in the output line of the pulse synchronizer. The use of the eight steps and 100 nanosecond delay line allows much finer timing adjustment and better risetime than that obtainable from a single step and one microsecond variable delay line.

To produce a variable phase 1.3 MHz output trigger for beam monitoring devices the pulse synchronizer shift register is "unplugged" and a jumper installed between the "clock" and the output buffer.
The measured jitter of pulses within this 1.3 MHz pulse train is less than 50 nanoseconds, allowing use in triggering a sampling scope to observe the 475 MHz bunch structure of stored beams.

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The 1.3 MHz output is also used to drive harmonically related beam excitation devices such as the RF quadrupole and 362nd harmonic cavity.

References


The above photo shows two bunches in the accelerator, using a four loop RF beam monitor as the pickup device. The picture was made by triggering a sampling oscilloscope (Tektronix 661) with the 1.3 MHz signal from the synchronizer. The time base was 500ps/cm and 10mv/cm with a .5 mA stored beam.

![Synchronizer Block Diagram](image-url)