PCM DATA TRANSMISSION SYSTEM USING SPLIT PHASE CODE*

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Summary

The LAMPF control system specifies transmission of both data and timing signals between the control room and the local control points throughout the machine for data collection and equipment control information. A balanced system is used to reduce noise pickup. The transmitter receives a timing pulse train and the digital data in a "non return to zero" (NRZ) format. The two signals are combined to form a split phase code and transformer coupled to the transmission line. The receiver uses a minimum energy content circuit (integrator) preceding the decoder to reduce noise sensitivity. The number of timing pulses in the incoming pulse train is known as is the time duration of the transmission. This information is used to further reduce the probability of error.

LAMPF Data System Characteristics

The LAMPF control system is based on a central digital computer for control of the machine. At each of the local data points, analog signals are converted to digital format by an analog to digital converter, and transmitted to the computer. Digital control signals are transmitted back to the local control points and converted into analog or binary (ON-OFF) signals to control the various equipments that make up the accelerator control system. The distances over which the signals must be transmitted (3000 ft. maximum) and the reliability necessary to avoid spurious commands, require careful attention to the characteristics of the transmission system. The large number of channels involved require fairly high over-all transmission rates.

Transmission System

A balanced transmission system has been selected to reduce the noise picked up on the lines. The level of the signals at the transmitting end is approximately 20 volts, peak to peak. Restrictions have been placed on the waveform and pulse train characteristics which will be acceptable to the receiver.

The number of timing pulses and the length of the word transmitted in either direction from the control room to the local operating point are known. Therefore, the receiver can be designed to discriminate against signals which do not "fit".

The input signals are the timing pulse string and the data information. The data is in the form of an NRZ code; a "1" is represented by one of the two possible levels and a "0" by the other. The transition takes place at the beginning of each bit cell. This information is fed into an encoder which combines the two signals into a split-phase code. The split-phase code used here divides each one of the bit cells into two parts. An input "1" is converted to a "10" and an input "0" to "01". The split-phase, or bi-phase, code always has a zero crossing at the center of the bit cell and the direction of this crossing is indicative of the bit value.

The first bit transmitted is always zero to set up the decoder at the receiving end. Both the timing information and data word have been combined into a single signal to reduce the number of transmission lines required between the computer and each of the data locations to one line in each direction.

Encoder - Transmitter

Fig. 1 is a simplified schematic of the Encoder-Transmitter. Sketches show the waveforms at various points in the circuit. The input inverters are self-explanatory. The "AND" function requires all three of the inputs high (positive) for a low output. (The transmit enable is driven high at the beginning of the transmission.) The "OR" function uses the same logic elements as the "AND" function but operates in a different mode. If any one input is low, the output will be high. In the absence of a transmit enable, the output of the "AND" gates will be low ("OR gate outputs high), as indicated by the waveforms and no voltage will be applied to the output transformer on either winding.

The "transmit" and "timing" inputs are driven high at time T_O. (The timing input to Gates 1 and 3 high.) If the data is low, the input to Gate 2 and 3 will be high because of the action of the inverter. Since 3 is the only one which will now have all three inputs high, the low coupled from the output of Gate 3 to Gate 6 causes the output of Gate 6 to go high. The power driver then switches 15 volts to the lower end of the transformer to drive the output of the transformer low, as indicated by the waveforms.

The timing signal then goes low. The inputs from the timing signal to Gates 2 and 4 will be high, due to the action of the inverter. The zero has remained low. Gate 2 then has all three inputs high; output, low. This low output couples through Gate 5 and causes the power driver (7) to drive the upper end of the transformer winding high. At the same time, the lower end is returned to zero. Since the center tap is grounded, the output is driven positive.

The signal placed on the lines by the transformer swings alternately, plus and minus 15 volts, with the direction of the transition in the center of the bit cell determined by the data bit. Because the timing and data signal may be slightly skewed with respect to each other, a narrow notch may appear in the top or bottom of the transmitted waveform when the transition is made from a "0" to a "1" or a "1" to a "0", as shown by the waveforms. Over long transmission distances, this notch may be smeared out and cannot be depended upon in the decoding network to provide a signal to indicate the end or beginning of a new bit cell.

Receiver - Decoder

A schematic of the receiver-decoder is shown in Fig. 2. Only those components which are necessary for the understanding of the system have been included in the figure. Waveforms are shown to assist in the understanding of the operation of this circuit.

The integrated circuits use DTL logic. The gates are designed such that when both inputs are high (positive), the output will be close to zero. If either input is low, the output will be high. The one-shot and JK F/F's trigger when the input goes low. The state to which they transfer will be determined by the inputs to the JK. For A and B F/F's, the inputs have been tied to the positive voltage. This causes them to change state for each negative-going trigger signal. F/F C output is determined by the polarity on the "S" and "C" inputs. If the C input is high (S low) when the toggle occurs, the data output will be high. If S is high (C low), the output will be low. Because these two outputs are connected to opposite ends of the transformer, they will alternate, depending on which polarity is present at the output of T1 when the trigger signal occurs.

The incoming pulse train is coupled into T1 and again split into two signals 180° out of phase with each other. Each signal is then fed to an integrating detector. The signal comes in through Terminal A ("TYP No. 1" block) to the junction of L1, CR1 and R1. A positive signal back-biases CR1 and charges C1 through R1. The rate at which C1 will charge is determined by R1, and delays the transistor turn on time. One of the inputs to "OR" gate F will be pulled low (output high) when the transistor turns on.

At the conclusion of the pulse, the output of the transformer is reversed. Diodes CR1 and CR2 conduct to discharge C1 and prevent the transistor base from being driven more than a few tenths of a volt negative. At the same time, one base is being driven negative, the base of the transistor in the other integrating circuit will be going positive because of the 180° phase relationship on the output of the transformer. The effect of these two circuits is to cause each bit cell to be divided into two separate cells with a bit in each one. These bits occur at a rate which is twice the fundamental frequency of the incoming waveform. However, when a "0" is followed by a "1", or a "1" by a "0", the incoming pulse does not change during the first half of the bit cell.

The output of Gate F will be low with no signal present. This low signal is coupled into Gate H and triggers a one-shot flip-flop (F/F) if a signal is received through the transformer of sufficient amplitude and duration to turn on one of the transistors in the integrating circuit. The output of the one-shot removes the clamps placed on each one of the F/F's "A, B and C". As long as this clamp is present, the data and timing outputs are forced low.

When a positive transition of Gate G output occurs, the trigger to F/F will be driven negative. On the first transition only, the charge on capacitor C2 holds the clamps on each one of the F/F's during the transition to prevent triggering any of the F/F's. This allows the timing and data sequence to start in the proper sequence. The first bit will always be read as a "0".

A negative transition on the output of G toggles F/F B to drive the "Q" output positive. The second time the output of G is driven positive, the timing F/F will be toggled since the holding voltage on the F/F's is zero by this time. Operating F/F A on the leading edge and F/F B on the trailing edge of the output of Gate G shifts the timing relative to the data to permit strobing into registers.

The second bit, a "1" in the diagram, is "read" by F/F C one quarter of the bit cell late to allow the "S" and "C" inputs to settle properly (as are all succeeding bits).

As long as the bits succeeding one another are the same, i.e. "0" follows "0" or "1" follows "1", the circuit operates as described above. However, when a "0" follows "1" or a "1" a "0", the required transition to control the integrating circuits and gate F does not occur. Therefore, F/F D has been added to simulate this effect. The output of this one-shot F/F has been adjusted to match the timing signal pulse width.

F/F D is triggered when the timing signal goes negative. At the conclusion of the timing interval, when the timing signal would normally go positive, the F/F returns to its quiescent state and a pulse is applied to one input of Gate G to simulate the transition from one state to the other. If the transformer output changed polarity, this pulse is not necessary. However, if the reversal were not made, the simulated signal then causes the F/F's to function as described above. The value for C3 and R4 have been chosen to provide a pulse of sufficient width to Gate G to delay the toggle of the timing F/F long enough to maintain proper data-timing pulse positions. F/F B is triggered by the negative-going signal from Gate G. This occurs when either the Q output of F/F D goes positive or the Gate F output goes positive. These transitions must occur within ± 10% of each other in time.

F/F E has the duration of the pulse adjusted to allow sufficient time to receive the word coming in. When this F/F returns to the quiescent state, the count of timing pulses received is compared with the number that should have been received including a parity bit. If this comparison is not valid, the information is assumed to contain an error. A portion of the output of the Gate J is fed back to H to prevent spurious triggering toward the end of F/F E timing interval.

Signals can be fed into Gate J which will result from decoding the function portion of the incoming word. If the function is not a valid one, the information may be rejected.

Operating Range

The decoder must be adjusted to match the characteristics on the incoming signal. R1 may be adjusted in both integrating networks to provide an optimum integrating time such that the transistor will be turned on at a quarter of the bit cell time interval. The output of the F/F E may be adjusted to correspond either to the total word length or to the length of the function code of the incoming word.

These two circuits have been adjusted over a relatively wide range. The lower bit rate limit is determined by the transformer. The system was operated at a bit rate of 770 Kbps. No tests were run to determine the upper limit. As the bit rate is changed, no adjustments were made in the transmitter; however, the slew or offset between timing and data became more important as bit rate was increased.

In the receiver, changes in bit rate necessitated changes in the integrator time constant; the value of L1; the C3-R4 time constant and the value of C2 in the bench model. Essentially no tests were run on the prototype with variable bit rates.

The signal coming in through the transformer alternates between ± V. However, the final transition returns to zero. It has been found that this causes a problem with the reset of the last integration. In order to assure proper operation, an inductor L1 has been added in parallel with the input circuit to force the final transition to return to zero as rapidly as is necessary.

Tests conducted on the system have proven to be entirely satisfactory and at the present time, a system is in operation. A simulated noise signal approximately equal to the data signal amplitude was induced on the line without causing a malfunction of the system.

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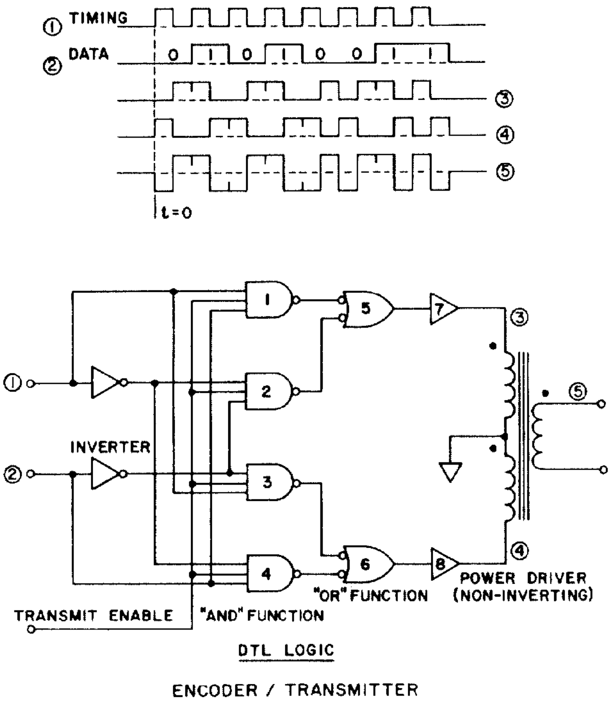

Figure 1.

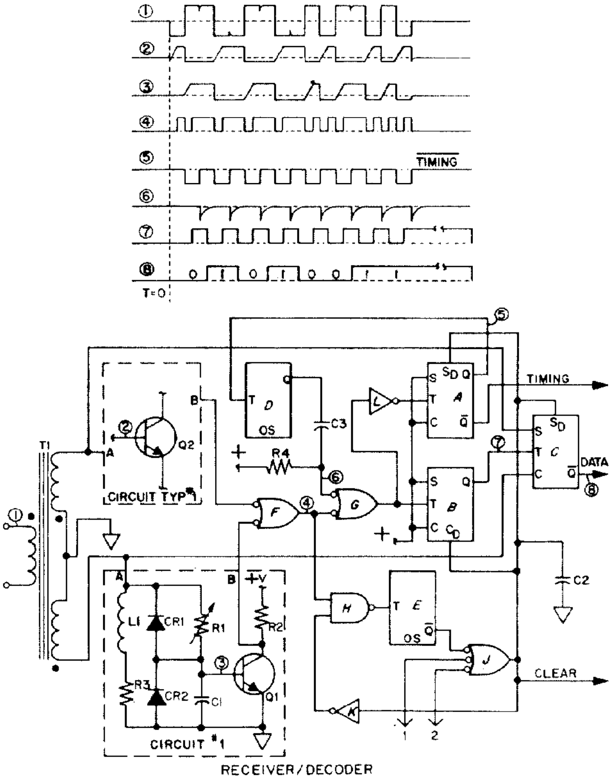

Figure 2.